INTEGRATED CIRCUITS

DATA HANDBOOK

Advanced CMOS logis
ACL

BOOK IC07 1990

Philips Components

PHILIPS

ADVANCED CMOS LOGIC ACL

Signetics reserves the right to make changes, without notice, in the products, including circuits, standard cells, and/or software, described or contained herein in order to improve design and/or performance. Signetics assumes no responsibility or liability for the use of any of these products, conveys no license or title under any patent, copyright, or mask work right to these products, and makes no representations or warranties that these products are free from patent, copyright, or mask work right infringement, unless otherwise specified. Applications that are described herein for any of these products are for illustrative purposes only. Signetics makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

LIFE SUPPORT APPLICATIONS

Signetics' Products are not designed for use in life support appliances, devices, or systems where malfunction of a Signetics Product can reasonably be expected to result in a personal injury. Signetics' customers using or selling Signetics' Products for use in such applications do so at their own risk and agree to fully indemnify Signetics for any damages resulting in such improper use or sale.

Signetics registers eligible circuits under
the Semiconductor Chip Protection Act.

Preface

Signetics would like to thank you for your interest in our ACL product family. Utilizing a 1μm CMOS process, Signetics' ACL has joined the lowest power-delay product family in the market today. This, coupled with its standard setting, low-noise, system reliable pinout, makes it an obvious favorite among system designers.

In addition to ACL, Signetics Standard Products Group offers the industry's broadest line of commercially available logic products. These products span a wide speed/power spectrum from 100K/10K ECL, to FAST to 74HC/HCT and other industry standard families such as: the CMOS 4000B series, 74, 74LS, 74S, 8T, and 8200 Logic. Information regarding these products lines is also available from your nearest Signetics Sales Office, sales representative, or authorized distributor.

Standard Products Group

Product Status

DEFINITIONS		
Data Sheet Identification	**Product Status**	**Definition**
Objective Specification	**Formative or In Design**	This data sheet contains the design target or goal specifications for product development. Specifications may change in any manner without notice.
Preliminary Specification	**Preproduction Product**	This data sheet contains a preliminary data and supplementary data will be published at a later date. Signetics reserves the right to make changes at any time without notice in order to improve design and supply the best possible products.
Product Specification	**Full Production**	This data sheet contains Final Specifications. Signetics reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.

Section 1
Introduction

INDEX

Introduction

INTRODUCTION

There is little doubt that CMOS is closing in on bipolar technology as the mainstay of integrated commodity logic. Advancing technology is rapidly eliminating the old trade-offs between speed and power dissipation (see Figure 1), and problems peculiar to CMOS such as latch-up and ESD sensitivity have already been solved. However, until now, CMOS logic ICs have been unable to match the high speed and the high current output of TTL technologies which is essential for operation in the bus or transmission line environment of the fastest logic systems.

The introduction of the Advanced CMOS Logic (ACL) family of ICs removes this hurdle. Signetics fabricates ACL in a 1-micron twin-well CMOS process with recessed local oxidation and a titanium disilicide layer on the gate, source and drain areas to reduce the contact and interconnect resistance. This, together with oxidation of the gate sidewalls for reduced capacitance, leads to increased drive and speed that equals that of the fastest bipolar TTL logic. With an average propagation delay of 5ns (150MHz operation) and 24mA sink/source capability, ACL supplements the HE4000B and HCMOC IC ranges to allow designers to implement the outstanding CMOS benefits of wide and symmetrical noise margins, high reliability, and reduced power dissipation across the whole speed spectrum of logic circuitry.

The inevitable fast edges associated with the exceptionally high speed of ACL required one final hurdle to be removed: the problem, which also exists for fast-switching bipolar logic, can reduce system noise margins, cause loss of stored data and reduce system speed. We have solved it for ACL by discarding the traditional corner supply pinning arrangement and simultaneously adopting a flowthrough architecture wherein the supply pins are at the center of each side of the package (where the internal inductance is minimum), all the input pins are on one side, all the output pins are on the other, and control pins are at the corners. Although this solution means that ACL is not pin-compatible with the comparable TTL and HCMOS functions, as an engineering-driven company, we felt that the considerations of improving system reliability, simplifying pcb design and reducing board area should take precedence.

All types within our ACL family have outputs that are both CMOS and TTL-compatible and are available for operating temperature ranges of -40°C to +85°C (commercial/industrial: 74AC/ACT prefix) or -55°C to +125°C (military: 54AC/ACT prefix). They come in two versions:

- Fully buffered 54/74AC types with CMOS-compatible input switching levels (typically $V_{cc}/2$) and a supply voltage range of 3V to 5.5V for all-CMOS systems
- Fully buffered 54/74ACT types with TTL-compatible input switching levels (typically 1.5V) and a supply voltage range of 5V±10% for interfacing with TTL systems

Since the low power dissipation of our ACL ICs makes them ideal for circuitry on densely packed boards in small enclosures, we didn't overlook the need to make them compatible with surface mounting technology which is being increasingly used for automated assembly of electronic equipment to achieve significant reduction of its size and weight. Production quantities of *all* our ACL ICs are available in DIP packages and in SO (small outline) packages. The dimensions of the latter were originally developed by us and now form the basis of JEDEC standard publication 95 (also published in IEC standard document 191-2, family A76).

ACL ICs are completely latch-up free and have complete protection against electrostatic discharge (ESD) at their inputs.

ACL IN A NUTSHELL

ACL has all the well-known attributes of our HCMOS family combined with faster operation and increased drive capability. Here are 14 reasons why Signetics is head and shoulders above the rest:

- A comprehensive type range from simple gates to shift registers and counters
- All types available in 74AC versions (CMOS input levels) and 74ACT versions (TTL input levels)
- All types available in SO (small outline) packages as well as in DIP, so you can use surface-mount techniques to increase pcb packing density. The 14 and 16-pin SO packages are the narrower 150mil (3.8mm) versions and are available on 16mm tape on 13 inch diameters reels (2500 ICs). The 16, 20, 24 and 28-pin SO packages are 300mil (7.6mm) wide and are available on 24mm tape with 1000 ICs on a 13 inch reel. The body width of all the DIP packages (14 to 28 pins) is 300mil (7.6mm).
- Completely latch-up free and fully ESD protected up to ±2kV (human body model) at all inputs and outputs.
- Low power dissipation. Typical quiescent current per package is only a few nanoamps for gates, flip-flops and MSI. Typical counter operating current with a 5V supply is 250µA at 1MHz and increases linearly with frequency.
- 24mA sink/source current. For incident wave switching 74AC/ACT types can provide ±75mA (for driving a 50Ω load).
- ACL input current is only 1µA in the High or Low state. This is essentially zero compared with the input current of TTL technologies. The fan-out to other CMOS ICs is therefore only limited by load capacitance considerations and not by DC loads.
- More than three times the noise immunity of TTL. Input switching levels are between 30% and 70% of V_{cc} for 74AC types and between 0.8V and 2V for 74ACT types. The output swing for all ACL ICs is from 0.1V to V_{cc}-0.1V with a load of 50µA (fifty ACL inputs), and from 0.5V to V_{cc}-0.8V with a load of ±24mA.
- The input switching threshold level is subject to a variation of only ±60mV

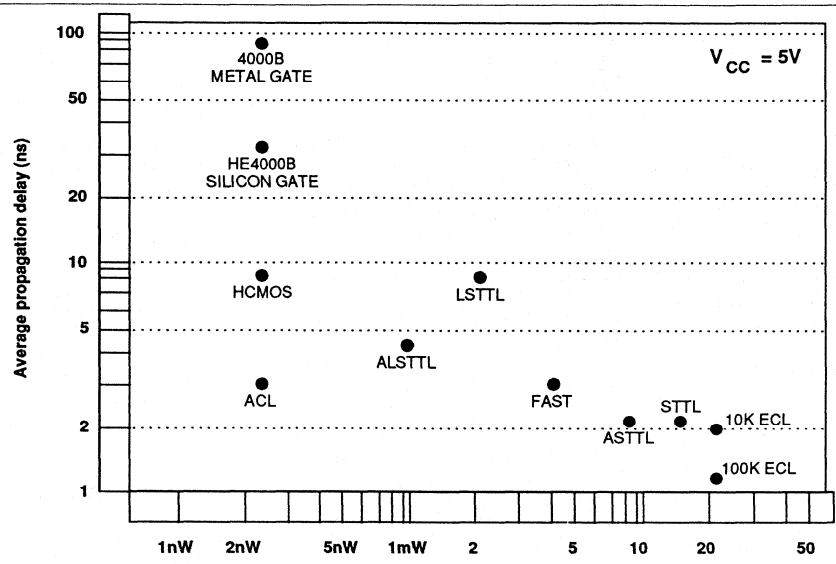


Figure 1. The Logic Family Speed/Power Sectrum

over the entire temperature range, much less than the ±300mV specified for advanced TTL families.

- Wide supply voltage range. AC versions are specified with a supply from 3V to 5.5V (the internal logic state is maintained down to 2V). Battery back-up is no problem and automotive applications are possible. TTl-compatible ACT versions are specified with a supply of 5V ± 10%.
- With a 5V supply, average propagation delay for a gate is 5ns for either High-to-Low or Low-to-High transitions into a capacitive load of 50pF. On-chip propagation delay for gates is only 0.5ns. Typical operating frequency is up to 150MHz at 25°C and f_{MAX} is simply specified with a 50% duty factor.
- Outputs have edge control circuits to reduce the effective dv/dt, thereby further reducing switching noise. The output buffers are standardized to allow symmetrical output current sourcing and sinking for equal output rise and fall times. This results in simplified design combined with optimum speed and AC performance.
- Center supply pins and flowthrough architecture to minimize ground and supply rail glitches during simultaneous switching of outputs, and to simplify board layout.
- All ACL critical inputs have a new patented dynamic hysteresis to make them less susceptible to slow input edges. (A critical input is considered an input which controls more than one output.)
- Extensive customer support is available.
- Signetics ACL ICs are alternate-source by TI.

A CLOSER LOOK AT ACL

Supply Voltage

ACL circuits with the type number prefix 74AC operate from a supply voltage range of 3V to 5.5V which meets the new industry JEDEC standard No. 8 which specifies 3.3V ±0.3V for regulated power supply systems. The internal logic of 74AC circuits will, however, maintain its state with a supply voltage as low as 2V. This facilitates the use of a lithium battery as a back-up supply. ACL circuits with the type number prefix 74ACT operate from a supply voltage of 5V ±10% which is consistent with the supply voltage for the TTL logic circuits with which they are intended to interface.

Power Dissipation

One of the most important requirements for any logic system is low power dissipation because it minimizes system cost, allows higher packing density, and results in improved reliability because of lower operating temperature.

The typical quiescent power dissipation of an ACL gate (2.5nW) is more than six orders of magnitude less than that of bipolar TTL functions. This is because, unlike TTL circuits, CMOS circuits dissipate only negligible power due to leakage currents when they are not switching. The maximum quiescent current per ACL package for SSI (40μA) is less than 1% of that of an equivalent TTL package with 50% of the gates in the High state. The typical dynamic power dissipation of ACL gates is also very low. With 50pF load and a 5V supply, it is 0.18mW at 100kHz rising to only 18mW at 10MHz, two-thirds of which is dissipated in the load capacitance. This is considerably lower than that of the fastest TTL circuits, particularly at lower frequencies where their high quiescent current predominates over their dynamic current.

The power cross-over frequency where ACL and TTL dissipate the same power is

about 10MHz for a gate, and more than 20MHz for a flip-flop. However, in a practical logic system, only a few of the logic elements operate at the maximum clock frequency, so the average operating frequency is much lower, giving ACL ICs an even greater advantage over advanced TTL. In a more complex system comprising a divider chain of six flip-flops, the power cross-over frequency no longer exists. At 30MHz, ACL still dissipates only one sixth of the equivalent advanced TTL dissipation. If the divider chain is lengthened, or the system complexity increased, the power saving increases even more.

Propagation Delay

The on-chip propagation for a single ACL gate is only 0.5ns. For an entire ACL package with a 50pF load, it is 5ns average for High-to-Low or Low-to-High transitions. Moreover, propagation delay is specified over the entire operating temperature range and at two system supply voltages (3.3V ± 0.3V and 5V ± 0.5V). For user convenience, we also specify the minimum propagation delay. The specified limits are comparable to those for the most advanced TTL logic. The AC characteristics of ACL are improved by standardized output buffers which allow equal rise and fall times. The typical switching frequency limit for ACL is 150MHz at 25°C and is specified with a 50% duty factor so you don't have to tweak the pulse widths as you do with TTL. Due to the high drive current capability of the low impedance ACL outputs, propagation delay variation as a function of load capacitance is much less than that of most other logic ICs.

Noise Immunity

The input switching levels for 74AC ICs are always between 30% and 70% of V_{cc}. Output swing is from 0.1V to V_{cc}-0.1V with a load of 50μA (50 CMOS inputs). For 74AC circuits driving 50 CMOS inputs, the low- and high-level noise immunity with a 4.5V supply is, therefor, 28% of V_{cc}. It is even greater for a higher supply voltage, 74ACT ICs match the Low-level noise immunity of TTL at higher operating temperatures (up to 85°C) and exceed it at 70°C. The High-level noise immunity is three times that of TTL. ACL ICs are, therefore, ideally suited for use in electrically noisy environments such as those encountered in industry, telephony and automotive applications.

Drive Capability

Although the ACL family has the low input current which is a characteristic of CMOS circuits, it is capable of providing output current of up to 24mA without sacrifice of noise immunity or switching speed. Moreover, unlike the fastest TTL circuits, all ACL ICs have standardized output buffers which allow symmetrical output current sinking and sourcing to obtain equal rise and fall times. This simplifies design and results in optimum speed and AC performance.

The drive current specified for ACL is valid over the entire operating temperature range and, since the input current for ACL circuits is only 1μA in the High or Low state, the fan-out when driving other CMOS circuits is only limited by load capacitance considerations and not by the available drive power. However, in the fastest logic systems, ACL will probably be working in a transmission line environment where its low output resistance (20Ω max.) is of particular significance for reducing a system's susceptibility to crosstalk and induced noise, and for guaranteeing incident wave switching to optimize system speed. For example, to guarantee incident wave switching over the commercial temperature range, the sink/source capability of ACL is 75mA at V_o=1.65V which allows terminated lines with a characteristic impedance down to 50Ω to be driven at the maximum supply voltage.

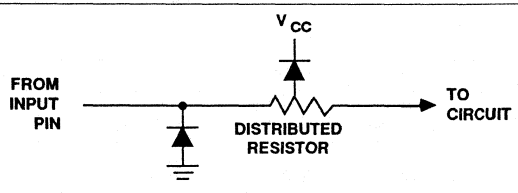
ESD Protection

The ACL input network shown in Figure 2(a) incorporates reverse-biased diodes between the positive rail, input pins and ground in order to clamp the input voltage to provide ESD protection and limit the amplitude of any ringing. These diodes have typical forward voltage drops of 0.9V and reverse breakdown voltages of 18V. ACL inputs can withstand ESD of greater than ±2kV from the 'human body model' (1.5k Ω, 100pF, 13ns pulse rise time) shown in Figure 2(b). This meets MIL-STD-883B, Method 3015.

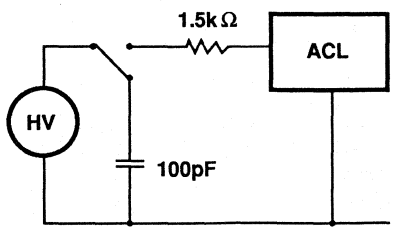
Large inherent diodes formed by the drain surfaces of ACL output transistors provide protection and allow discharges up to 2kV to be sustained without damage to outputs.

ACL Is Latch-up Free

Latch-up can be reduced by the use of extensive guard rings, but at the expense of increased chip area. In our ACL family, we've completely eliminated latch-up by growing the high-resistivity p- epitaxial layer on a very low-resistivity p- layer and



(a) ACL Input Protection Network



(b) 'Human Body Model' Test Arrangement

Figure 2. The Inputs of ACL ICs Are Fully Protected Against ESD.

thereby prevents parasitic bipolar transistors from being forward biased. This, plus proprietary layout rules and process parameters that even further reduce the gain of the parasitic bipolar transistors, means that our ACL ICs are completely latch-up free.

We've subjected our ACL ICs to latch-up tests with ratings far exceeding those specified by JEDEC. In no case did latch-up occur. For example, input/outputs can withstand currents as high as 100mA DC or 450mA pulsed. V_{cc} breakdown for ACL ICs doesn't occur until a supply current of 6.8mA; this requires a supply voltage of more than 21V. After breakdown, the supply voltage always snaps back to a level far greater than the maximum operating supply voltage. So, latch-up will not occur in the event of severe supply over voltage.

74ACT - FOR INTERFACING WITH TTL

Since the entire type range of ACL ICs is also available in 74ACT versions, it is easy to drive ACL from ALS-TTL, AS-TTL or FAST-TTL outputs without using power consuming pull-up resistors at the bipolar logic outputs to maintain adequate noise margins.

All the advantages previously described for 74AC ICs naturally also apply to the 74ACT versions. The only differences are that the propagation delay is slightly longer and the nominal supply voltage and the input structure of the 74ACT types have been modified to match TTL characteristics. The modified input structure not only adapts to TTL input switching levels, but also reduces power consumption when a minimum TTL High output level of 2.4V is applied to a 74ACT input.

For TTL compatibility, the supply voltages for 74ACT ICs is 5V ±10%. Unlike 74AC ICs which have an input switching threshold of 50% of V_{cc}, the input switching threshold of 74ACT types is 1.5V and the inputs switch between the same levels as TTL ($V_{IL\,max}$=0.8V, $V_{IH\,min}$=2V). The temperature sensitivity of the input switching threshold, however, is only ±60mV over the entire temperature range, so the noise margins also remain very stable over the temperature range. With a 4.5V supply and an output current of 50µA (50 ACL inputs), a 74ACT output swings between 0.1V and V_{cc}-0.1V. With the maximum output current of 24mA, it swings between 0.5V and V_{cc}-0.8V. So, for a 74ACT IC with a 4.5V supply driving fifty ACL inputs, the noise margins are 53% of V_{cc} (High) and 15.5% of V_{cc} (Low). For a similar LSTTL IC, they would be only 15% of V_{cc}(High and 8% of V_{cc} (Low). Even when a 74ACT IC is delivering 24mA, the noise margins are 42% of V_{cc} (High) and 6.6% of V_{cc} (Low).

ADVANCED TECHNOLOGY MAKES IT POSSIBLE

The 10-mask ACL construction is a result of our continuing development program to enhance the proven polycrystalline silicon (polysilicon) gate CMOS process. It incorporates several technological innovations for increasing packing density, speed, and reliability.

The twin-well p/n structure and double-layer metal interconnects allow a high packing density which will also facilitate development of future MSI/LSI circuitry.

Three main features contribute to the exceptionally high speed of ACL. Firstly, the effective length of the transistor gate is only 1µm, resulting in an on-chip propagation delay of only 0.5ns. Secondly, there is a self-aligning titanium disilicide (salicide) layer on the source gate and drain to reduce series resistance and to reduce contact resistance between the 2-layer metal interconnects and the junctions. Thirdly, oxidation of the sidewalls of the gate minimizes the gate/source and gate/drain capacitances.

Reliability is assured by using copper-doped aluminum on tungsten intercon-

SAFE DRIVING-INTERFACE REQUIREMENTS

Safe driving-interface requirements		TO					
		HC/AC 5V supply	HCT/ACT 5V supply	HE4000B 5V supply	HE4000B 6-15 V supply	TTL* 5V supply	ECL 10K
FROM	HC/AC 5V supply	direct	direct	direct	4104	direct	10124
	HCT/ACT 5V supply	direct	direct	direct	4104	direct	10124
	HE4000B 5V supply	direct	direct	direct	4104	direct	10124
	HE4000B 6-15V supply	4049 or 4050	4049 or 4050	4049 or 4050	direct	4049 or 4050	transistor
	TTL* 5V supply	pull-up resistor	direct	pull-up resistor	4104	direct	10124
	ECL 10K	10125	10125	10125	transistor	10124	direct

* Includes LS, S, STD, FAST, ALS and AS

NOTES:
direct = without interface components
4104 = Low-to-High level shifters from the HE4000B family
10124 = TTL to ECL translator from the ECL 10K and 100K families
10125 = ECL to TTL translator from the ECL 10K and 100K families
4049/4050 = High-to-Low level shifters from the HE4000B family

nects to achieve high resistance to electromigration. A very thin titanium layer below the tungsten promotes adhesion to the underlying oxide. Furthermore, a p- epitaxial layer on a low-resistivity p+ substrate results in a high degree of latch-up immunity.

NEW PINOUTS FOR ACL ADD RELIABILITY AND SIMPLIFY DESIGN

The fast rise and fall times associated with high speed logic can lead to noise problems when one or more outputs of an IC switch from one logic state to another. As shown in Figure 3 this discharges the load capacitances through the internal supply pin inductance, thereby causing a transient that lifts up the on-chip ground and reduces the effective supply voltage to the chip. The problems are particularly severe in CMOS logic in which the outputs can switch almost from one supply rail to the other. Referred to as simultaneous switching noise, the transient appears on any unswitched output(s) of the switching IC and has a peak amplitude directly proportional to the number of outputs simultaneously switched and to the internal inductance associated with the IC supply connections. This lifting up of the GND and consequent reduction of V_{cc} levels degrades system reliability by reducing noise margins, reducing speed, causing loss of stored data and causing false switching.

It is a common misconception that supply decoupling capacitors located adjacent to each IC will eliminate simultaneous output switching transients. The output capacitance discharge noise is related to the absolute inductance of the supply connection between the chip in the IC and the external supply groundplane. Since multilayer boards provide excellent supply and groundplanes, improvement can only be achieved by manufacturers taking measures to reduce the supply lead inductances within the IC. Supply line decoupling should be similar to that used for TTL systems operating at comparable speed.

In the early days of integrated logic, IC manufacturers were forced to position the supply pins at diagonally opposite corners of the package because of layout restrictions imposed by single-sided print-boards which were in universal use at that time. However, in today's world of double-sided and multilayer print-boards and much faster logic, placing the supply pins at diagonally opposite corners of the package where the long bonding wires and lead frame segments have the maximum inductance can no longer be considered to be good engineering practice because it's the worst possible positioning from the point of view of simultaneous switching noise. So, for our ACL ICs, we've decided that optimum reliability is far more important than pin compatibility with TTL, and we've relocated the GND and V_{cc} pins; 16-pin ICs with 3 or 4 outputs have two GND pins and two V_{cc} pins; 20, 24 and 28-pin ICs with 3 or more outputs have four GND pins and two V_{cc} pins.

Tests performed on our octal ACL ICs with the new pinning reveal that, when seven outputs are simultaneously switched from High to Low, the amplitude of simultaneous switching noise stays well below the Low input switching level and is only about 35% of that for an IC with corner GND and V_{cc} pins.

We've also rationalized the positioning of the I/O and control pinning of ACL ICs as shown in Figure 4. All the inputs surround the V_{cc} pin(s) on the side of the package with the highest pin numbers, and all the outputs surround the GND pin(s) on the other side of the package. The control pins are strategically placed at the corners of the package. This ACL flow-through architecture, which is used for all ACL ICs in both DIP and SO packages, reduces the total inductance of outputs (bonding wire plus lead frame and output pin) between the chip and the pcb tracks. It also facilitates positioning of decoupling components, simplifies pcb design and fault-finding, and decreases the area of pcb required.

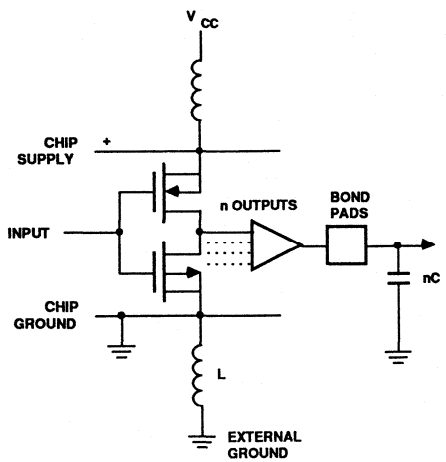


Figure 3

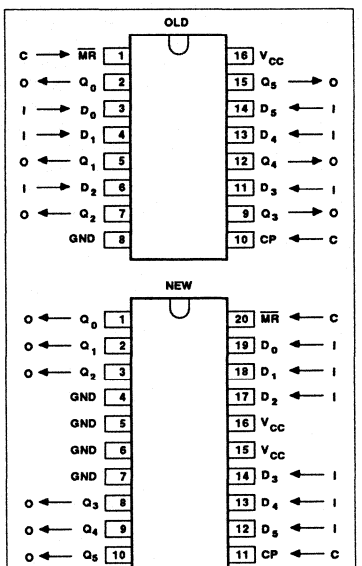


Figure 4 Flow-through Architecture of 74AC11174

Alphanumeric Index

Alphanumeric Index

† See Section 4 for this device's pin configuration.

For more information on these devices contact your local sales organization; see addresses on back cover.

Alphanumeric Index

† See Section 4 for this device's pin configuration.
For more information on these devices contact your local sales organization; see addresses on back cover.

Functional Index

ACL 74AC/ACT11XXX FAMILY

Type numbers have a suffix which signifies the type of package:
N = Plastic DIP; D = Plastic Surface Mount Device

† See Section 4 for this device's pin configuration.

For more information on these devices contact your local sales organization; see addresses on back cover.

Functional Index

† See Section 4 for this device's pin configuration.
For more information on these devices contact your local sales organization; see addresses on back cover.

Functional Index

† See Section 4 for this device's pin configuration.

For more information on these devices contact your local sales organization; see addresses on back cover.

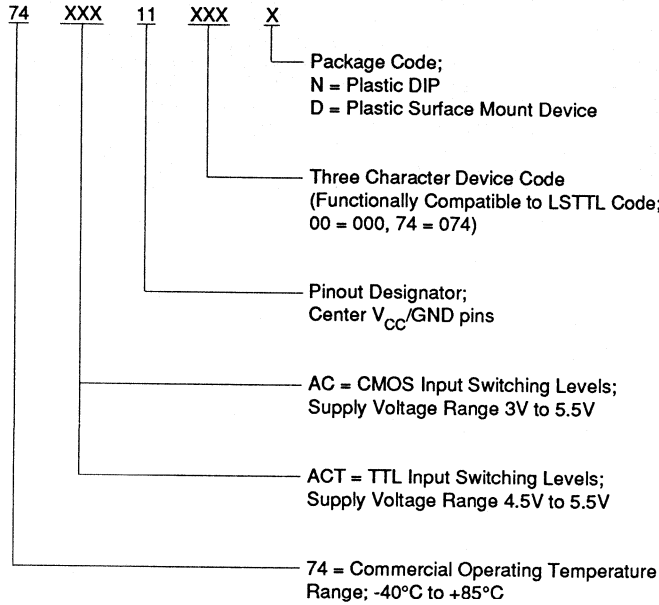
Functional Index

† See Section 4 for this device's pin configuration.
For more information on these devices contact your local sales organization; see addresses on back cover.

Functional Index

Ordering Information

TYPE NUMBER DESIGNATIONS



Section 2
Quality And Reliability

Quality And Reliability

QUALITY ASSURANCE PROGRAMS

Signetics Quality Program

In 1979, Signetics recognized that quality was becoming a major competitive issue, not only in the semiconductor business, but also in other industries. Increases in the volume of products imported from the Far East (steel, automobiles, and consumer electronics) sent strong signals that new competitive forces were at work.

Signetics quickly began to investigate a variety of quality programs. The company realized that quality improvement would require a contribution from *all* employees. Management commitment and participation, however, was recognized as the primary prerequisite for this program to work successfully. Resources required for the resolution of defects were under management control.

In 1980, Signetics developed a program which focused on quality management. Rearranging previous quality control philosophies, Signetics developed a decentralized, distributed quality organization and simultaneously installed a quality improvement process based on the 14-Step improvement program advocated by Phil Crosby. The process was formally begun company-wide in 1981.

Since then, substantial progress has been made in every aspect of Signetics operations. From incoming raw material conformance to improvements in administrative clerical errors — every department and individual is involved and striving for Zero Defects. Zero Accept sampling plans and Zero Defects warranties are evidence of Signetics ongoing commitment and progress in quality.

Today, Signetics quality improvement process has had a far-reaching impact on all aspects of our business. Signetics provides its customers with products of refined electrical and mechanical quality. And through continual use and modification of the Crosby program, Signetics is providing itself with a well-defined method of managing ongoing improvement efforts.

Signetics Zero Defects Warranty

In recent years, American industry has demanded increased product quality of its IC suppliers in order to meet growing international competitive pressure. As a result of this quality focus, it is becoming clear that what was once thought to be unattainable — Zero Defects — is, in fact, achievable.

Signetics offers a Zero Defects Warranty which states that it will take back an entire lot if a single defective part is found. This precedent setting warranty has effectively ended the IC industry's "war of the AQLs" (Acceptable Quality Levels). The ongoing efforts of IC suppliers to reduce PPM (Parts Per Million) defect levels is now a competitive customer service measure.This intense commitment to quality provides an advantage to today's electronics OEM. That advantage can be summed up in four words: *Reduced Cost of Ownership*

As IC customers look beyond purchase price to the total cost of doing business with a vendor, it is apparent that a quality-conscious supplier, like Signetics, represents a viable cost reduction resource. Consistent high-quality circuits reduce requirements for expensive test equipment and personnel, and allow for smaller inventories, less rework, and fewer field failures

Signetics Statistical Process Control (SPC)

Although application of statistics in our process development and manufacturing activities goes back to the early 1970's, the corporate-wide emphasis on Statistical Process Control (SPC) did not come about until mid-1984.

A natural evolution of our quality process made introduction of SPC and other related programs an inevitable event. SPC was, therefore, introduced under the quality umbrella.

The objective of the SPC program is to introduce a systematic and scientific approach to business and manufacturing activities. This approach utilizes sound statistical theory. Managers are expected to be able to turn data into information, and make decisions solely based on data (not perceptions).

The most critical and challenging aspect of implementing SPC is establishment of a discipline within the operating areas so that decision making is fundamentally based on verifiable data, and actions are documented. The other is realization of the fact that statistical tools merely point out the problems and are not solutions by themselves. The burden of action on the process is still on the implementers' shoulders. In order to implement SPC effectively, three steps are continually followed:

Documenting and understanding the process, using process flow charts and component diagrams.

Establishing data collection systems, and using SPC tools to identify process problems and opportunities for improvement.

Acting on the process, and establishing guidelines to monitor and maintain process control.

Repeating steps 1-3 again.

These fundamentals are the basis of establishing Signetics specifications and operating philosophy with respect to SPC. Signetics believes a solid foundation creates a permanent system and accelerates our quality improvement process.

Signetics Quality Performance

Signetics Quality Improvement Program has influenced our entire production cycle — from the purchase of raw materials to the shipment of finished product. The involvement of all areas of the company has resulted in impressive quality improvements. A traditional quality gauge is final product electrical and visual-me-

chanical defect levels as measured upon first submittal results at Signetics outgoing Quality Assurance gates; Estimated Process Quality (This is the PPM Level at our first outgoing inspection for all accepted and rejected lots.) (Figures I and II). Current product shipments routinely record below 20 PPM (Parts Per Million) electrical defect levels and 150 PPM visual-mechanical defect levels. Since Signetics utilizes zero accept sampling on all finished product inspection, any lot with one or more rejects is 100 percent retested.

The most meaningful measure of our product quality is how we measure up to our customers' expectations. Many customers routinely send us incoming inspection data on our products. One major mainframe manufacturer has reported zero defects in electrical, visual-mechanical, and hermeticity and has reported a 100 percent lot acceptance rate on Signetics Standard Products products for over a year. Due to this type of performance, an increasing number of our customers are eliminating expensive incoming inspection testing and have begun implementation of Signetics Ship-to-Stock program.

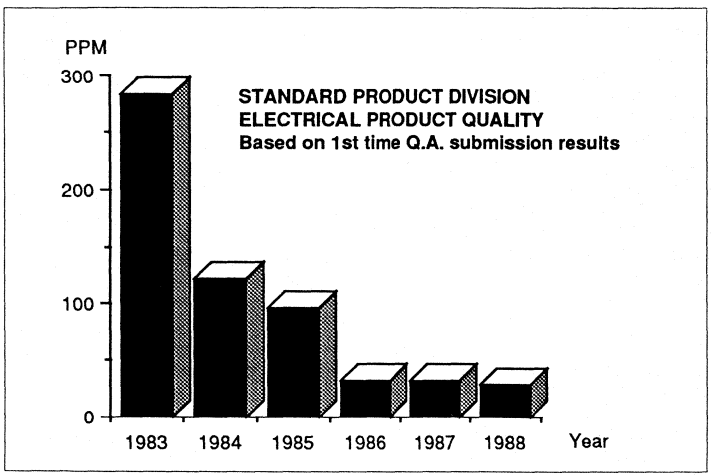


Figure I

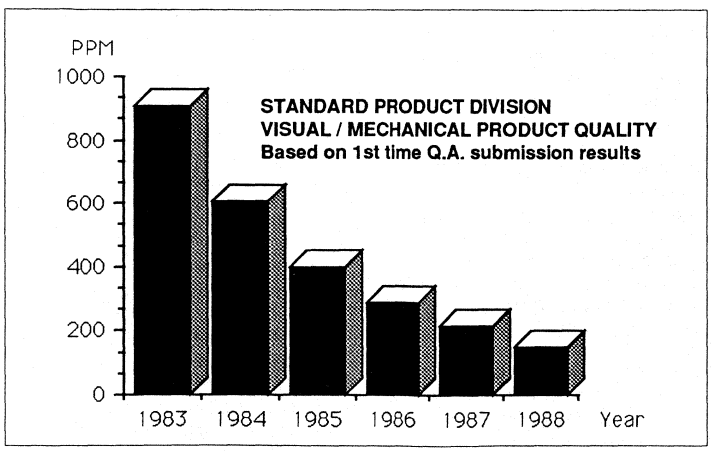


Figure II

Signetics Ship-to-Stock Program

Ship-to-Stock is a formal program developed at the request of our customers to help them reduce their costs by eliminating incoming test and inspection. Through close work with these customers in our quality improvement program, they became confident that our defect rates were so low that the redundancy of incoming inspections and testing was not only expensive, but unnecessary. They also saw that added component handling increased the potential of causing defects.

Ship-to-Stock is a joint program between Signetics and a customer which formally certifies specific parts to go directly into the customer's assembly line or inventory. This program was developed at the request of several major manufacturers after they had worked with us and had a chance to experience the data exchange and joint corrective action occurring as part of our quality improvement program.

Manufacturers using large volumes of ICs, those who are evaluating Just-in-Time delivery programs, or those who want to reduce or avoid high-cost incoming inspection are strongly encouraged to participate in this worthwhile program. Contact your local Signetics sales representative for further assistance and information on how to participate in this program.

Summary

The Signetics Quality Improvement Program has had a far-reaching impact on all aspects of our business. It has, of course, provided our customers with products of improved electrical and mechanical quality and has provided Signetics with a method of managing product reliability improvement to ensure that Signetics products continue to perform as specified.

The corrective action teams that work to eliminate the cause of defects in Signetics products are committed to producing highly reliable integrated circuits and, as demonstrated by our continually improved product reliability performance, we are well on the way to achieving our objective, *Zero Defects*.

RELIABILITY ASSURANCE PROGRAMS

Focus on Product Reliability

During the period from 1981 to 1984, continuing improvements in process and material quality had a significant impact on product reliability.

Since 1984, Signetics has intensified its efforts to markedly improve product reliability. Corporate Reliability Engineering, Division and Plant Reliability Units, Philips Research Labs-Sunnyvale, and Manufacturing Engineering work jointly on numerous improvement activities. These focused activities enhance the reliability of Signetics future products by providing improved methods for reliability assessment, increased understanding of failure physics, advanced analytical techniques, and aid in the development of materials and processes.

Reliability Measurement Programs

Signetics has developed comprehensive product and process qualification programs to assure that its customers are receiving highly reliable products for their critical applications. Additionally, ongoing reliability monitoring programs, SURE III and Product Monitor, sample standard production product on a regularly established basis (see Table I below).

Description of Stresses

SHTL — Static High Temperature Life: SHTL stressing applies static DC bias to the device. This has specific merit in detecting ionic contamination problems which require continuous uninterrupted bias to drive contaminants to the silicon surface. The voltage bias must be maintained until the devices are cooled down to room temperature from the elevated life test temperature. DHTL stressing is not as effective in detecting such problems because the bias continuously changes, intermittently generating and healing the problem. For this reason, SHTL has typically been used as the accelerated life stress for Standard Products products.

HTSL — High Temperature Storage Life: This stress exposes the parts to elevated temperatures (150°C-175°C) with no applied bias. For plastic packages, 175°C is the high end of its safe temperature region without accelerating untypical failure mechanisms. This test is intended to accelerate mechanical package-related failure mechanisms such as Gold-Aluminum bond integrity and other process instabilities.

THBS — Temperature-Humidity, Biased, Static: This accelerated temperature and humidity bias stress is performed at 85°C and 85% relative humidity (85°C/85% RH). In general, the worst case bias condition is the one which minimizes the device power dissipation and maximizes the applied voltage. Higher power dissipations tend to lower the humidity level at the chip surface and lessen the corrosion susceptibility.

TMCL — Temperature Cycling, Air-to-Air: The device is cycled between the specified upper and lower temperature without power in an air or nitrogen environment. Normal temperature extremes are -65°C and +150°C with a minimum 10 minute dwell and 5 minute transition per Mil-STD-883C, Method 1010.5, Condition C. This is a good test to measure the overall package to die mechanical compatibility, because the thermal expansion coefficients of the plastic are normally very much higher than those of the die and leadframe. However, for large die the stress may be too severe and induce failures that would not be expected in a real application.

PPOT — Pressure Pot: This stress exposes the devices to saturated steam at elevated temperature and pressure. The standard condition is 20 PSIG which occurs at a temperature of 127°C and 100% RH. The stress is used to test the moisture resistance of plastic encapsulated devices. The plastic encapsulant is not a moisture barrier and will saturate with moisture within 72 hours. Since the

TABLE I RELIABILITY ASSURANCE PROGRAMS

Reliability Function	Typical Stress	Frequency
New Process Qualification	High Temperature Operating Life Temperature-Humidity, Biased, Static High Temperature Storage Life Pressure Pot Temperature Cycle	Each new wafer fab process
New Product Qualification	High Temperature Operating Life Temperature-Humidity, Biased, Static High Temperature Storage Life Pressure Pot Temperature Cycle Electrostatic Discharge Characterization	Each new product family
SURE III	High Temperature Operating Life Temperature-Humidity, Biased, Static High Temperature Storage Life Pressure Pot Temperature Cycle Thermal Shock	Each fab process family, every four weeks
Product Monitor	Pressure Pot Thermal Shock	Each package type and technology family at each assembly plant, every week

chip is not powered up the chip temperature and relative humidity will be the same as the autoclave once equilibrium is reached. Because the steam environment has an unlimited supply of moisture and ample temperature to catalyze thermally activated events, it is effective at detecting corrosion problems, contamination induced leakage problems, and general glassivation stability and integrity. It is also a good test for both package integrity (cracks in the package), and for die cracks (the moisture swells the plastic enough to stress the die — also the moisture causes leakage paths in the crack itself).

TMSK — Thermal Shock, Liquid-to-Liquid: Similar to TMCL, except that, heating and cooling are done by immersing the units in hot and cold inert liquid. Temperature extremes are -65°C to +150°C with a minimum 5 minute dwell and less than 10 second transition per Mil-STD-883C, Method 1011.4, Condition C. Since heat transfer by conduction is generally much faster than by convection, the liquid-based thermal shock causes more rapid temperature changes in the part. Also, as the part is rapidly changing in temperature all its mass will not be in equilibrium and the temperature gradients across the part will produce additional mechanical stress. For chip-out under bond these factors combine to give an acceleration of 1.5X over TMCL. For ball neck break (wire creep) failures, acceleration of 10X has been observed. To date, there is no reasonable explanation for why the relative accelerations in TMCL and TMSK are so variable and dependent on the failure mechanism.

PRODUCT AND PROCESS

Qualifications

Qualification activity is centered around new products and processes and changes in products and processes. The goal is to assure that the products can meet the qualification requirements prior to general release, and on an ongoing basis to demonstrate conformance to those requirements. The nature and extent of reliability stressing required depends on the type of change and the amount of applicable reliability data available.

A full qualification may include Early Failure Rate (EFR), Intrinsic Failure Rate (IFR), and Environmental Endurance Stressing. Such stress plans are reserved for introductions or changes that involve new or untested material or processes and, as such should be subjected to the maximum reliability interrogation. This normally entails a full range of biased and unbiased temperature and humidity stresses along with thermo-mechanical stresses.

For changes that are of limited scope, the full range of qualification stressing may not be warranted. In these instances, the nature and extent of the change is examined and only those stresses which provide a valuable measure of the change, or those which will detect potential weaknesses, are performed.

Signetics Self-Qual Program (SSQP)

Self-Qual is a joint program between Signetics and a customer which formally communicates Signetics qualification activities for a new or changed product, process, or material. The Signetics Self-Qual process provides our customer's engineering groups an opportunity to participate in the development of the qualification plan. During the qualification process, customers may audit the project, and can receive interim updates of qualification progress. Upon completion, formal detailed engineering reports are provided.

The major impact to the customer comes from the reduced workload on the component engineering and qualification groups. These engineering resources generally divide their time between routine qualification activity and problem resolution on critical components. By eliminating the need to perform qualification for some of the basic vendor changes the customer component engineer can spend more of his time resolving the critical product issues. In addition, the total amount of stress hardware needed to perform qualification life tests and other environmental evaluations can be reduced, saving the customer facility costs and reducing operating expense.

Self-Qual is a no-risk proposition for the customer. Each Self-Qual proposal provides a detailed description of what we are changing and why. It includes a detailed plan of what we intend to do to establish the reliability of the products affected. If the customer wishes to have products added to the plan, or select some additional stresses, or prefers alternative stress conditions, Signetics will do everything possible to accommodate those requests. After that, if the customer is still uncomfortable with the recommended change, they are *under no obligation* to accept our data, and they may perform their own qualification program in addition to Signetics.

Customers who are interested in participating in this program should contact their local Signetics sales representative or Signetics Corporate Reliability Engineering department directly.

Sure III Reliability Monitoring Program

In order to implement an improvement program, a standard measure of performance was needed. Signetics uses the results from the SURE III Reliability Monitoring Program as its basic ongoing measure of product reliability performance. This program samples all generic families of products manufactured by Signetics, and utilizes standardized stress methods and test procedures. This system is augmented by new product and process qualification activities and infant mortality monitoring programs.

Signetics adopted a measurement philosophy based on the premise of continual improvement toward our performance standard of zero defects.

We also increased our standard Pressure Pot stress conditions from 15 PSIG/121°C to 20 PSIG/127°C. This reduced stress duration from 168 hours to 72 hours, and increased high volume sampling, which increased sensitivity to low defect levels.

Our standard monitoring program, SURE III, includes the stress conditions as described in Table II:

Product Monitor

In addition to the SURE III program, each Signetics assembly plant performs Pressure Pot (20 PSIG, 127°C, 72 Hours) and Thermal Shock (-65°C to +150°C, 300

Cycles) reliability monitors on a weekly basis for each molded package type by pin count. The purpose of this program is to monitor the consistency of the assembly operations for such attributes as molding quality and die attach and wire bond integrity. These data are reported back to manufacturing operations and corporate and divisional reliability and quality assurance departments by electronic mail each week.

Reliability Evaluations

In addition to the product performance monitors encompassed in the SURE III program, Signetics Corporate and Division Reliability Engineering departments sustain a broad range of evaluation and qualification activities.

Included in the engineering process are:

Evaluation and qualification of new or changed materials, assembly/wafer-fab processes and equipment, product designs, facilities, and subcontractors.

Device or generic group failure rate studies.

Advanced environmental stress development.

Failure mechanism characterization and corrective action/prevention reporting.

The environmental stresses utilized in the engineering programs are similar to those utilized for the SURE III program, however, more highly-accelerated conditions and extended durations typify these engineering projects. Additional stress systems such as biased pressure pot, power-temperature cycling, and cycle-biased temperature-humidity, are often included in some evaluation programs.

Stress Facility Quality

Signetics quality improvement has reached all functional areas of the company, and the reliability stress laboratories are no exception. Corporate Reliability Laboratory (CRL) is one of the many areas where the benefits of the quality improvement process pays repeated dividends.

CRL utilizes stresses which accelerate failure rates hundreds to thousands of times, requiring precision and control to make reliability data meaningful. Stress loading schedules are maintained with absolute regularity and chambers are never off-line beyond scheduled loading plans. Board currents are recorded prior to and at each interval on biased stresses, and monitoring of in-oven currents is conducted daily.

Thermal modeling of both Thermal Shock and Temperature Cycling systems has been accomplished and all loads are carefully weighed to ensure that thermal ramps are consistent.

Pressure Pot and Biased Pressure Pot systems utilize microprocessor controllers, and are accurate to within 0.1 degree centigrade. Saturation is guaranteed via automatic timing circuits, and a host of fail-safe controls ensure that test groups are never damaged.

Electrostatic discharge (ESD) handling precautions are standard procedures in the laboratories, and the occurrences of devices lost, zapped, or over-stressed have become almost non-existent.

TABLE II SURE III RELIABILITY MONITORING PROGRAMS

Reliability Function	Stress Conditions
Static High Temperature Operating Life (SHTL)	$T_J \geq 150°C$, T_A = 125°C to 150°C, Bias condition = Static, VCC = MAX, Duration = 1000 hours
High Temperature Storage Life (HTSL)	T_A = 150°C, Bias condition = None, Duration = 1000 hours
Temperature-Humidity, Biased, Static (THBS)	T_A = 85°C ± 3°C, Humidity = 85% RH ± 5% Bias condition = Static, V_{CC} = MAX, Duration = 1000 hours
Temperature Cycling (TMCL)	T_A = -65°C (+0°C - 10°C) to +150°C (+10°C - 0°C), Air-to-Air, Dwell time = 10 minutes minimum each extreme Bias condition = None, Duration = 1000 cycles for plastic package = 300 cycles for ceramic package
Pressure Pot	T_A =127°C ±2°C, 20 PSIG ±0.5 PSIG (PPOT), 100% saturated steam, Bias condition = None, Duration = 72 hours
Thermal Shock (TMSK)	T_A = -65°C (+0°C - 10°C) to +150°C (+10°C - 0°C), Liquid-to-Liquid, Dwell time = 5 minutes minimum each extreme Bias condition = None

Reliability Improvement Programs

Currently, Signetics is involved in a number of reliability improvement programs intended to enhance product reliability performance. A series of activities are currently addressing failure rate reduction in thermal cycling stresses, particularly on large die. Other reliability improvement programs involve the use of Silicon Nitride and other technologically advanced passivation systems to increase the high humidity resistance of sensitive products.

Reducing early life failures has become a major focus at Signetics. Numerous corrective action teams are in the process of establishing high volume monitors capable of accurately describing parts per million (PPM) level infant failure rates. From data produced via these monitors, improvement in wafer fabrication process and assembly process technologies are developed to minimize integrated circuit defect levels.

Reliability Publications

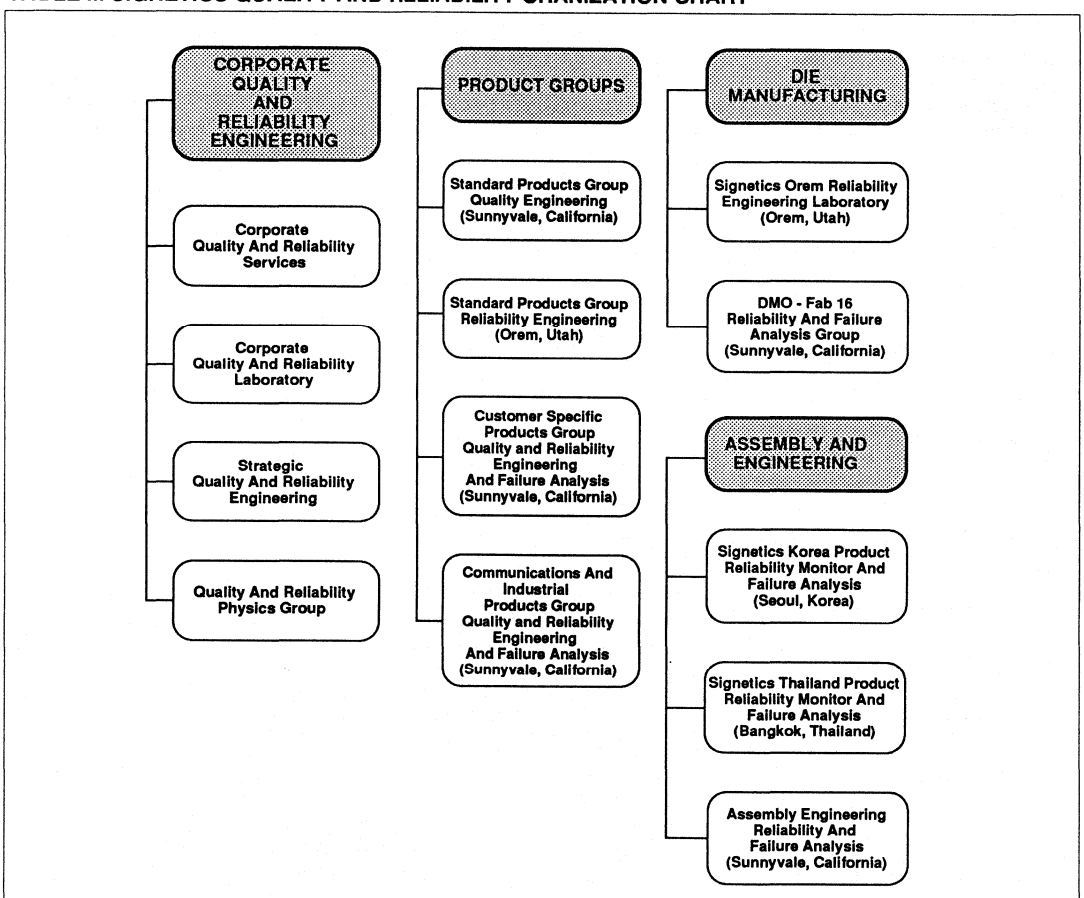
Data from all of these activities is made available to all Signetics customers in a variety of publications:

PRODUCT RELIABILITY SUMMARIES and *QUARTERLY UPDATES*
Yearly, each Product Division's SURE III monitoring data is summarized and published in a Product Reliability Summary. A quarterly update is also published.

SSQP—SIGNETICS SELF-QUAL PROGRAM
In addition to the regular publications of reliability monitor results, a special program for the publication of qualification proposals and final engineering reports has been in place since January of 1984.

SMD RELIABILITY
In support of Signetics leadership in Surface Mount Device (SMD) technology, we have published in-depth studies and evaluations on the reliability of numerous combinations of SMD packages and IC process technologies. These reports

TABLE III SIGNETICS QUALITY AND RELIABILITY ORANIZATION CHART



cover not only the basic product performance, but also evaluate products after exposure to the unique environments created by the various SMD soldering and cleaning processes.

SPECIAL RELIABILITY REPORTS
In addition to our standard reports, special reliability evaluation results are available on a wide variety of Signetics products and processes. Custom reports can be generated to meet specific customer needs and the most accurate failure rate estimates can be prepared for your specific system application and environment.

Data Availability
The previously referenced documents are available to all Signetics customers. Many are available in your local Signetics sales office, or:

Corporate Reliability Services
Reliability Publications Group
Department 9605, Mail Stop #34
Arques Avenue
Box 3409
Sunnyvale, CA 94088-3409

where you can be placed on a standard mailing list for all documentation which meet your specific requirement(s).

The Table III depicts the current organization for Signetics Quality and Reliability Group.

Signetics Manufacturing Facilities
Signetics, as part of a multinational corporation, utilizes manufacturing facilities for wafer fabrication, package assembly, and test in three states and three overseas countries. All wafer fabrication is performed in Signetics operated fabs which report to the Vice President of Die Manufacturing Operations (DMO) in Sunnyvale. Similarly, Signetics Assembly operations in Utah, Korea, and Thailand, report to the Vice President of Assembly Manufacturing Operations (AMO). Assembly subcontractors, Pebei and Anam, are scheduled and controlled through the AMO organization. Assembly subcontractors process all product to Signetics specifications and materials. Signetics has on-site quality assurance personnel at each subcontractor to audit assembly processes and procedures.

All Signetics products are electrically tested in Signetics operated facilities. These facilities report to the manufacturing organization (DMO or AMO) operating the facility at which they are located.

Typical IC Manufacturing Flow
The manufacturing process for Integrated Circuits begins with wafer fabrication. The wafers are then electrically sorted, assembled, and tested prior to customer shipment. Quality assurance inspections are utilized throughout the manufacturing process. Table IV contains a typical manufacturing flow for Signetics ICs.

TABLE IV MANUFACTURING FLOW FOR 1μm CMOS PRODUCT

Facilities	Manufacturing Flow
Wafer Fab	Initial Oxidation N- and P-Well Implant Gate Oxidation Polysilicon Layer Source/Drain Implant Silicide Block Mask Contact Mask Metallization #1 Dielectric Glass Layer Metallization #2 Passivation Layer
Wafer Sort	Wafer Electrical Test Wafer Visual Acceptance
Assembly	Saw Scribe and Break Die Sort Visual Acceptance Encapsulation Topside Symbolization Leadframe Trim and Form Solder Coat Mechanical/Visual Acceptance
Test	Final Electrical Test Burn-In (Optional) Product Assurance Test
Shipping	Pack-Out Outgoing Quality Control Acceptance Shipping

TABLE V PACKAGE CONSTRUCTION

ITEMS	PDIP	SO/PLCC	CERDIP
Lead Frame	Copper, 194 Alloy	Copper, 194 or PMC102	Alloy-42
Lead Finish	Tin/Lead Solder Dip (60/40)	Tin/Lead Solder Dip (60/40) or Solder Plate (80/20)	Tin/Lead Solder Dip (60/40)
Bond Area Finish	Silver Spot	Silver Spot	Silver Spot
Die Attach	Silver filled Polymide or Thermoplastic	Silver Filled Polymide or Thermoplastic	Silver Filled Glass
Bond Wire	Gold, 1.0-1.3 mil Diameter	Gold, 1.0-1.3 mil Diameter	Aluminum, 1.0 mil Diameter
Wire Bonding Die Lead Frame	Thermosonic Ball Stitch	Thermosonic Ball Stitch	Ultrasonic Stitch Stitch
Package Material	Novolac Epoxy	Novolac Epoxy	Ceramic

Table VII Package Code Definition

Pin Count	PDIP	SO	PLCC	CERDIP
8	NE	DE	-	FE
14	NH	DH	-	FH
16	NJ	DJ	-	FJ
18	NK	-	-	FK
20	NL	DL	AL	FL
22	NM	-	-	FM
24	NN	DN	-	FN
28	NQ	-	AQ	FQ
-	-	AA	-	

Section 3
Family Characteristics

INDEX

Family Specifications

GENERAL

These family specifications cover the common electrical ratings and characteristics of the entire 74AC/ACT11XXX family, unless otherwise specified in the individual device data sheet.

INTRODUCTION

The 74AC/ACT11XXX 1µm CMOS Logic family combines the low power advantages of CMOS with the high speed and drive capability of FAST.

The basic family of devices designated as 74AC11XXX will operate at CMOS input logic levels for high noise immunity, negligible quiescent supply and input current. It is operated from a power supply of 3 to 5.5V.

A subset of the family designated as 74ACT11XXX with the same features and functions as the "AC-types" will operate at standard TTL power supply voltage (5V±10%) and logic input levels (0.8 to 2.0V).

HANDLING MOS DEVICES

Inputs and outputs are protected against electrostatic effects in a wide variety of device-handling situations.

However, to be totally safe, it is desirable to take handling precautions into account (also see AN600 "Handling Precautions" in Section 6).

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	TEST CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 to+7.0	V
I_{IK} or V_I	DC input diode current[2]	$V_I < 0$	-20	mA
		$V_I > V_{CC}$	20	
	DC input voltage		-0.5 to V_{CC} +0.5	V
I_{OK} or V_O	DC output diode current[2]	$V_O < 0$	-50	mA
		$V_O > V_{CC}$	50	
	DC output voltage		-0.5 to V_{CC} +0.5	V
I_O	DC output source or sink current per output pin	V_O = 0 to V_{CC}	±50	mA
I_{CC} or I_{GND}	DC V_{CC} current	n = number of outputs (but not less than 100mA)	±(n x 25)	mA
	DC ground current	n = number of outputs (but not less than 100mA)	±(n x 25)	
T_{STG}	Storage temperature		-65 to 150	°C
P_{TOT}	Power dissipation per package Plastic DIP	Above 70°C:derate linearly by 8mW/K	500	mW
	Power dissipation per package Plastic surface mount (SO)	Above 70°C:derate linearly by 6mW/K	400	mW

NOTES:

1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		V_{CC}	74AC11XXX				74ACT11XXX				UNIT
					T_A = +25°C		T_A = -40°C to +85°C		T_A = +25°C		T_A = -40°C to +85°C		
				V	Min	Max	Min	Max	Min	Max	Min	Max	
V_{IH}	High-level input voltage			3.0	2.10		2.10						V
				4.5	3.15		3.15		2.0		2.0		
				5.5	3.85		3.85		2.0		2.0		
V_{IL}	Low-level input voltage			3.0		0.90		0.90					V
				4.5		1.35		1.35		0.8		0.8	
				5.5		1.65		1.65		0.8		0.8	
V_{OH}	High-level output voltage		I_{OH} = -50μA	3.0	2.9		2.9						V
				4.5	4.4		4.4		4.4		4.4		
				5.5	5.4		5.4		5.4		5.4		
			I_{OH} = -4mA	3.0	2.58		2.48						
			I_{OH} = -24mA	4.5	3.94		3.8		3.94		3.8		
				5.5	4.94		4.8		4.94		4.8		
			I_{OH} = -75mA[1]	5.5			3.85				3.85		
V_{OL}	Low-level output voltage		I_{OL} = 50μA	3.0		0.1		0.1					V
				4.5		0.1		0.1		0.1		0.1	
				5.5		0.1		0.1		0.1		0.1	
			I_{OL} = 12mA	3.0		0.36		0.44					
			I_{OL} = 24mA	4.5		0.36		0.44		0.36		0.44	
				5.5		0.36		0.44		0.36		0.44	
			I_{OL} = 75mA[1]	5.5				1.65				1.65	
I_I	Input leakage current	$V_I = V_{CC}$ or GND		5.5		±0.1		±1.0		±0.1		±1.0	μA
I_{OZ}	3-State output off-state current	$V_I = V_{IL}$ or V_{IH}, $V_O = V_{CC}$ or GND		5.5		±0.5		±5.0		±0.5		±5.0	μA
I_{CC}	Quiescent supply current, for SSI	$V_I = V_{CC}$ or GND, $I_O = 0$		5.5		4.0		40		4.0		40	μA
	Quiescent supply current, for MSI	$V_I = V_{CC}$ or GND, $I_O = 0$		5.5		8.0		80		8.0		80	
ΔI_{CC}	Supply current, TTL inputs High[2]	One input at 3.4V, other inputs at V_{CC} or GND		5.5						0.9		1.0	mA

NOTES:
1. Not more than one output should be tested at a time, and the duration of the test should not exceed 10ms.
2. This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0V or V_{CC}.

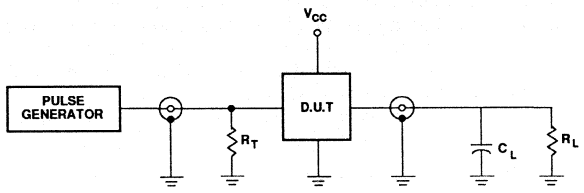
RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	74AC11XXX			74ACT11XXX			UNIT
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	DC supply voltage[1]	3.0	5.0	5.5	4.5	5.0	5.5	V
V_I	Input voltage	0		V_{CC}	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	0		V_{CC}	V
$\Delta t/\Delta v$	Input transition rise or fall rate	0		10	0		10	ns/V
T_A	Operating free-air temperature	-40		+85	-40		+85	°C

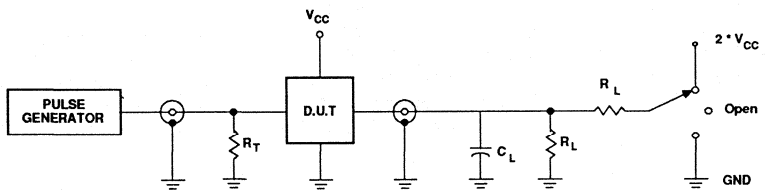
NOTE:

1. No electrical or switching characteristics are specified at V_{CC} < 3V. Operation between 2V and 3V is not recommended, but within that range, a device output will maintain a previously established logic state.

TEST CIRCUIT



Test Circuit



Test Circuit for 3-State Devices

TEST	S1
t_{PLH}/t_{PHL}	Open
$t_{PLZ}t_{PZL}$	2*VCC
t_{PHZ}/t_{PZH}	GND

SWITCH POSITION

DEFINITIONS

C_L = Load capacitance, 50pF; includes jig and probe capacitance

R_L = Load resistor, 500Ω

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators

Input pulses: PRR ≤ 10MHz

$t_r = t_f$ = 3ns

Data Sheet Specification Guide

INTRODUCTION

The 74ACL data sheets have been designed for ease-of-use. A minimum of cross-referencing for more information is needed.

TYPICAL PROPAGATION DELAY AND FREQUENCY

The typical propagation delays listed at the top of the data sheets are the average of t_{PLH} and t_{PHL} for a typical data path through the device with a 50pF load.

For clocked devices, the maximum frequency of operation is also given. The typical operating frequency is the maximum device operating frequency with a 50% duty factor and no constraints on t_R and t_F.

LOGIC SYMBOLS

Two logic symbols are given for each device - the conventional one (Logic Symbol) which explicitly shows the internal logic (except for complex logic) and the IEEE/IEC Logic Symbol.

The IEEE/IEC has been developing a very powerful symbolic language that can show the relationship of each input of a digital logic current to each output without explicitly showing the internal logic.

ABSOLUTE MAXIMUM RATINGS

The Absolute Maximum Ratings table lists the maximum limits to which the device can be subjected without damage. This does not imply that the device will function at these extreme conditions, only that, when these conditions are removed and the device operated within the Recommended Operating Conditions, it will still be functional and its useful life will not have been shortened.

RECOMMENDED OPERATING CONDITIONS

The "Recommended Operating Conditions" table lists the operating ambient temperature and the conditions under which the limits in the "DC Characteristics" and "AC Characteristics" table will be met. The table should not be seen as a set of limits guaranteed by the manufacturer, but as the conditions used to test the devices and guarantee that they will then meet the limits in the DC and AC Characteristics tables.

TEST CIRCUITS

Good high-frequency wiring practices should be used in test circuits. Capacitor leads should be as short as possible to minimize ripples on the output waveform transitions and undershoot. Generous ground metal (preferably a ground plate) should be used for the same reasons. A V_{CC} decoupling capacitor should be provided at the test socket, also with short leads. Input signals should have rise and fall times of 3ns, a signal swing of 0V to V_{CC} for 74AC and 0V to 3V for 74ACT; a 5MHz square wave is recommended for most propagation delay tests. The repetition rate must be increased for testing f_{MAX}. Two pulse generators are usually required for testing such parameters as setup time, hold time and removal time. f_{MAX} is also tested with 3ns input rise and fall times, with a 50% duty factor, but for typical f_{MAX} as high as 150MHz, there are no constraints on rise and fall times.

DC CHARACTERISTICS

The "DC Characteristics" table reflects the DC limits used during testing. The values published are guaranteed.

The threshold values of V_{IH} and V_{IL} are applied to the inputs, the output voltages will be those published in the "DC Characteristics" table. There is a tendency, by some, to use the published V_{IH} and V_{IL} thresholds to test a device for functionality in a "function-table exerciser" mode. This frequently causes problems because of the noise present at the test head of automated test equipment with cables up to 1 meter. Parametric tests, such as those used for the output levels under the V_{IH} and V_{IL} conditions are done fairly slowly, in the order of milliseconds, so that there is no noise at the inputs when the outputs are measured. But in functionality testing, the outputs are measured much faster, so there can be noise on the inputs, before the device has assumed its final and correct output state. Thus, never use V_{IH} and V_{IL} to test the functionality of any ACL device type; instead, use input voltages of V_{CC} (for the High state) and 0V (for the Low state). In no way does this imply that the devices are noise-sensitive in the final system.

In the data sheets, it may appear strange that the typical V_{IL} is higher than the maximum V_{IL}. However, this is because V_{ILMAX} is the maximum V_{IL} (guaranteed) for all devices that will be recognized as a logic Low. However, typically a higher V_{IL} will also be recognized as a logic Low. Conversely, the typical V_{IH} is lower than its minimum guaranteed level.

The quiescent supply current I_{CC} is the leakage current of all the reversed-biased diodes and the OFF-state MOS transistors.

AC CHARACTERISTICS

The "AC Characteristics" table lists the guaranteed limits when a device is tested under the conditions given in the AC Test Circuits and Waveform section.

Definitions of Symbols

DEFINITIONS OF SYMBOLS AND TERMS USED IN ACL DATA SHEETS

Current

Positive current is defined as conventional current flow into a device.

Negative current is defined as conventional current flow out of a device.

I_{CC} Quiescent power supply current; the current flowing into the V_{CC} supply terminal.

ΔI_{CC} Additional quiescent supply current per input pin at a specified input voltage and V_{CC}.

I_{GND} Quiescent power supply current; the current flowing into the GND terminal.

I_I Input leakage current; the current flowing into a device at a specified input voltage and V_{CC}.

I_{IK} Input diode current; the current flowing into a device at a specified input voltage.

I_{IO} Input/output source or sink current; the current flowing into a device at a specified input/output voltage.

I_O Output source or sink current; the current flowing into a device at a specified output voltage.

I_{OK} Output diode current; the current flowing into a device at a specified output voltage.

I_{OZ} OFF-state output current; the leakage current flowing into the output of a 3-State device in the OFF-state, when the output is connected to V_{CC} or GND.

Voltages

All voltages are referenced to GND (ground), which is typically 0V.

GND Supply voltage; for a device with a single negative power supply, the most negative power supply, used as the reference level for other voltages; typically ground.

V_{CC} Supply voltage; the most positive potential on the device.

V_{EE} Supply voltage; one of two (GND and V_{EE}) negative power supplies.

V_H Hysteresis voltage; difference between the trigger levels when applying a positive and a negative-going input signal.

V_{IH} High-level input voltage; the range of input voltages that represents a logic High-level in the system.

V_{IL} Low-level input voltage; the range of input voltages that represents a logic Low-level in the system.

V_{OH} High-level output voltage; the range of voltages at an output terminal with a specified output loading and supply voltage. Device inputs are conditioned to establish a High-level at the output.

V_{OL} Low-level output voltage; the range of voltages at an output terminal with a specified output loading and supply voltage. Device inputs are conditioned to establish a Low-level at the output.

V_{T+} Trigger threshold voltage; positive-going signal.

V_{T-} Trigger threshold voltage; negative-going signal.

Capacitances

C_I Input capacitance; the capacitance measured at a terminal connected to an input of a device.

$C_{I/O}$ Input/Output capacitance; the capacitance measured at a terminal connected to an I/O-pin (e.g. a transceiver).

C_L Output load capacitance; the capacitance connected to an output terminal including jig and probe capacitance.

C_{PD} Power dissipation capacitance; the capacitance used to determine the dynamic power dissipation per logic function when no extra load is provided to the device.

AC Switching Parameters

f_I Input frequency; for combinatorial logic devices the maximum number of inputs and outputs switching in accordance with the device function table. For sequential logic devices the clock frequency using alternate High and Low for data input or using the toggle mode, whichever is applicable.

f_O Output frequency; each output.

f_{MAX} Maximum clock frequency; clock input waveforms should have a 50% duty factor and be such as to cause the outputs to be switching from 10% V_{CC} to 90% V_{CC} in accordance with device function table.

t_H Hold time; the interval immediately following the active transition of the timing pulse (usually the clock pulse) or following the

transition of the control input to its latching level, during which interval the data to be recognized must be maintained at the input to ensure their continued recognition. A negative hold time indicates that the correct logic level may be released prior to the timing pulse and still be recognized.

t_R, t_F Clock input rise and fall times; 10% and 90% values.

t_{PHL} Propagation delay; the time between the specified reference points, normally the 50% points for 74AC devices on the input and output waveforms and the 1.5V points for the 74ACT devices, with the output changing from the defined High-level to the defined Low-level.

t_{PLH} Propagation delay; the time between the specified reference points, normally the 50% points for 74AC devices on the input and output waveforms and the 1.5V point for the 74ACT devices, with the output changing from the defined Low-level to the defined High-level.

t_{PHZ} 3-State output disable time; the time between the specified reference points, normally the 50% points for the 74AC devices and the 1.5V points for the 74ACT devices on the output enable input voltage waveform and a point representing 20% of the output swing on the output voltage waveform of a 3-State device, with the output changing from a High-level (V_{OH}) to a high-impedance OFF-state (Z).

t_{PLZ} 3-State output disable time; the time between the specified reference points, normally the 50% points for the 74AC devices and the 1.5V points for the 74ACT devices on the output enable input voltage waveform and a point representing 20% of the output swing on the output voltage waveform of a 3-State device, with the output changing from a Low-level (V_{OL}) to a high-impedance OFF-state (Z).

t_{PZH} 3-State output enable time; the time between the specified reference points, normally the 50% points for the 74AC devices and 1.5V points for the 74ACT devices on the output enable input voltage waveform and the 50% point on the output voltage waveform of a 3-State device, with the output changing from a high-impedance OFF-state (Z) to a High-level (V_{OH}).

t_{PZL} 3-State output enable time; the time between the specified reference points, normally the 50% points for the 74AC devices and the 1.5V points for the 74ACT devices on the output enable input voltage waveform and the 50% point on the output voltage waveform of a 3-State device with the output changing from a high-impedance OFF-state (Z) to a Low-level (V_{OL}).

t_{REC} Recovery time; the time between the end of and overriding asynchronous input, typically a clear or reset input, and the earliest permissible beginning of a synchronous control input, typically a clock input, normally measured at the 50% points for 74AC devices and the 1.5V points for the 74ACT devices on both input voltage waveforms.

t_S Setup time; the interval immediately preceding the active transition of the timing pulse (usually the clock pulse) or preceding the transition of the control input to its latching level, during which interval data to be recognized must be maintained at the input to ensure their recognition. A negative setup time indicates that the correct logic level may be initiated sometime after the active transition of the timing pulse and still be recognized.

t_{THL} Output transition time; the time between two specified reference points on a waveform, normally 90% and 10% points, that is changing from High-to-Low.

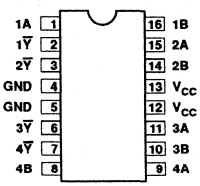
t_{TLH} Output transition time; the time between two specified reference points on a waveform, normally 10% and 90% points, that is changing from Low-to-High.

t_W Pulse width; the time between the 50% amplitude points on the leading and trailing edges of a pulse for 74AC devices and at the 1.5V points for 74ACT devices.

Section 4
ACL Pinouts

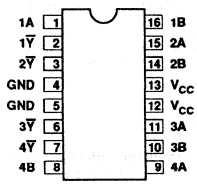
ACL Pinouts

11000



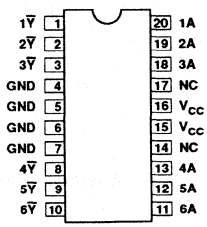
Quad 2-Input NAND Gate

11002



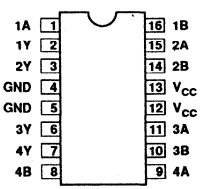
Quad 2-Input NOR Gate

11004



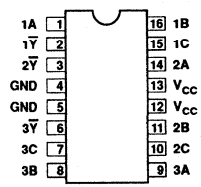
Hex Inverter

11008



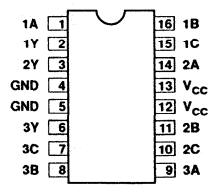
Quad 2-Input AND Gate

11010



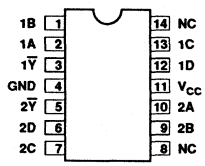
Triple 3-Input NAND Gate

11011



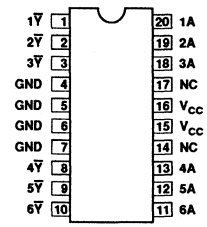
Triple 3-Input AND Gate

11013



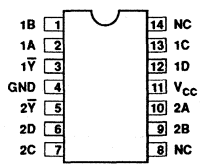
Dual 4-Input NAND Schmitt-Trigger

11014



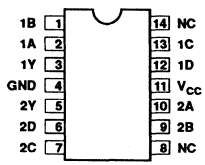
Hex Inverter Schmitt-Trigger

11020



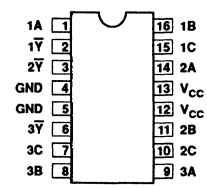
Dual 4-Input NAND Gate

11021



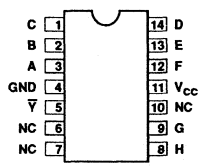
Dual 4-Input AND Gate

11027



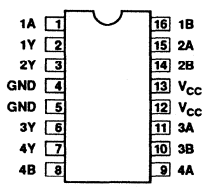
Triple 3-Input NOR Gate

11030



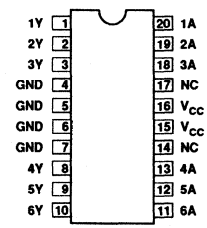
8-Input NAND Gate

11032



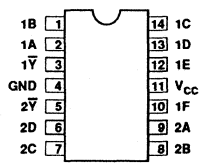
Quad 2-Input OR Gate

11034



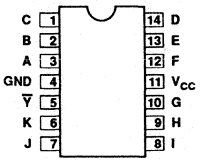
Hex Non-Inverter

11051



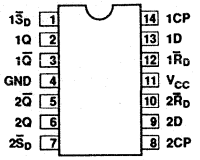
Dual 2-Wide 2-Input, 2-Wide 3-Input AND-OR-Invert Gate

11064



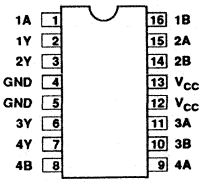
2-2-3-4-Input AND-OR-Invert Gate

11074



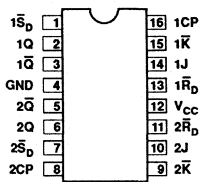
Dual D-Type Flip-Flop with Set and Reset; Positive-Edge Trigger

11086



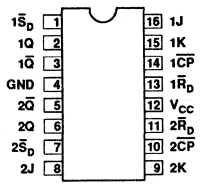
Quad 2-Input Exclusive-OR Gate

11109



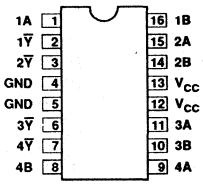
Dual J-K Flip-Flop with Set and Reset; Positive-Edge Trigger

11112



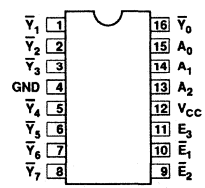
Dual J-K Flip-Flop with Set and Reset; Negative-Edge Trigger

11132



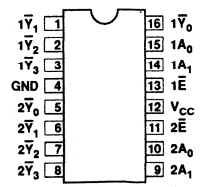
Quad 2-Input NAND Schmitt-Trigger

11138



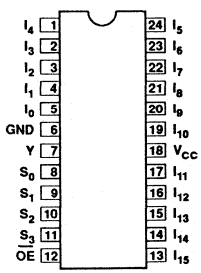
3-to-8 Line Decoder/Demultiplexer; Active-Low

11139



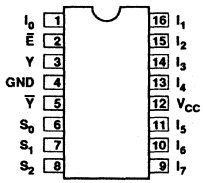
Dual 2-to-4 Line Decoder/Demultiplexer; Active Low

11150



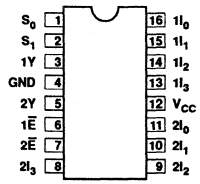
16-Input Multiplexer; 3-State

11151



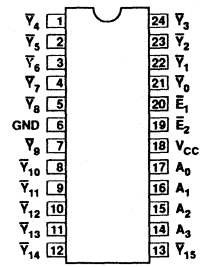
8-Input Multiplexer

11153



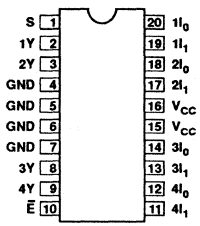
Dual 4-Input Multiplexer

11154



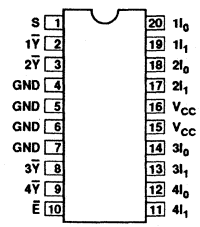
4-to-16 Line Decoder/Demultiplexer; Active-Low

11157



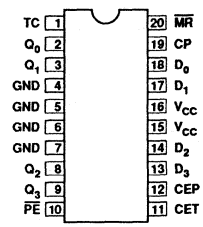
Quad 2-Input Multiplexer

11158



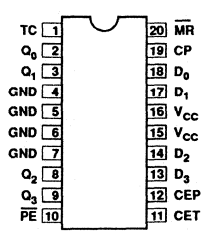
Quad 2-Input Multiplexer; INV

11160



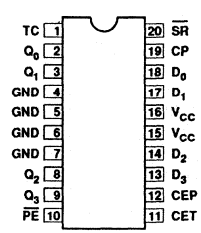
Synchronous Presettable Synchronous BCD Decade Counter; Asynchronous Reset

11161



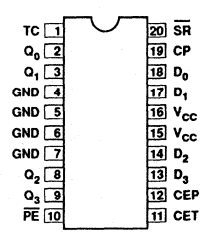
Synchronous Presettable Synchronous 4-Bit Binary Counter; Asynchronous Reset

11162



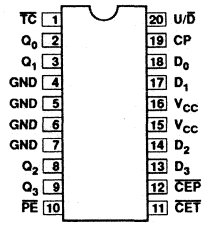
Synchronous Presettable Synchronous BCD Decade Counter; Synchronous Reset

11163



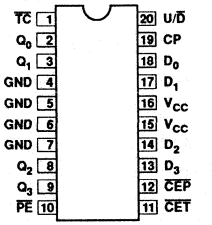
Synchronous Presettable Synchronous 4-Bit Binary Counter; Synchronous Reset

11168



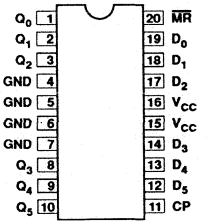
Synchronous Up/Down BCD Decade Counter

11169



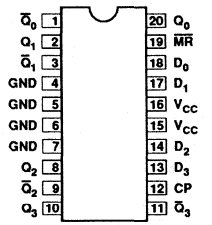
Synchronous Presettable 4-Bit Up/Down Binary Counter

11174



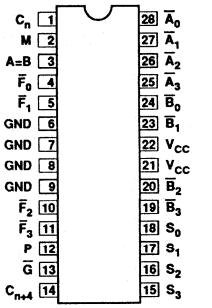
Hex D-Type Flip-Flop with Reset; Positive-Edge Trigger

11175



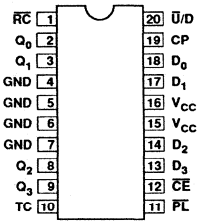
Quad D-Type Flip-Flop with Reset; Positive-Edge Trigger

11181



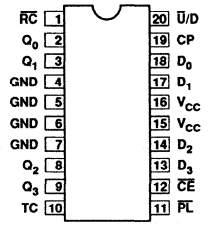
4-Bit Arithmetic Logic Unit

11190



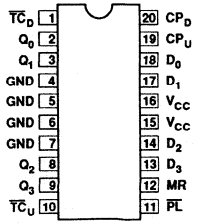
Asynchronous Presettable Synchronous Decade Up/Down Counter with Single Clock

11191



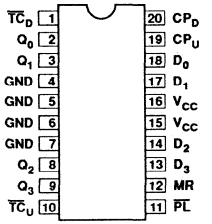
Asynchronous Presettable Synchronous 4-Bit Binary Counter with Single Clock

11192



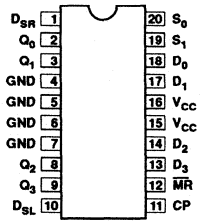
Asynchronous Presettable Synchronous BCD Decade Up/Down Counter with Dual Clock

11193



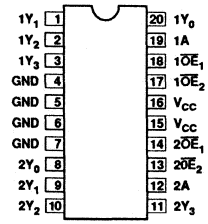
Asynchronous Presettable Synchronous 4-Bit Binary Up/Down Counter with Dual Clock

11194



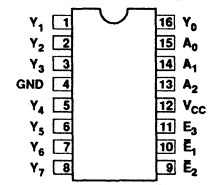
4-Bit Bidirectional Universal Shift Register

11208



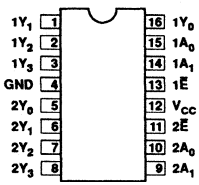
Dual 1-to-4 Clock Line Driver; 3-State

11238



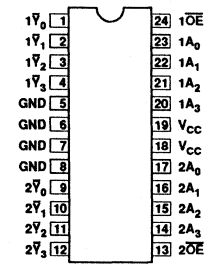
3-to-8 Line Decoder/Demultiplexer; Active High

11239



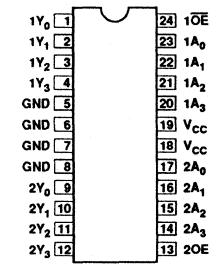
Dual 2-to-4 Line Decoder/Demultiplexer; Active High

11240



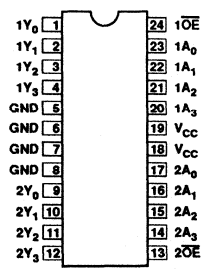
Octal Buffer/Line Driver; 3-State; INV

11241



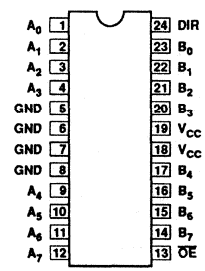
Octal Buffer/Line Driver; 3-State

11244



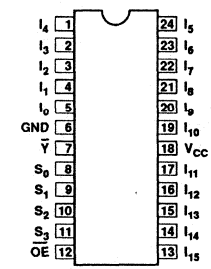
Octal Buffer/Line Driver; 3-State

11245



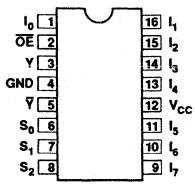
Octal Transceiver with Direction Pin; 3-State

11250



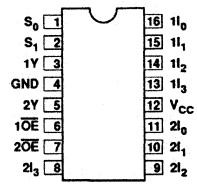
16-Input Multiplexer; 3-State; INV

11251



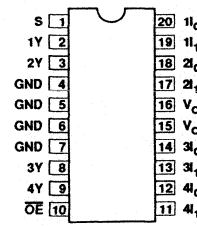
8-Input Multiplexer; 3-State

11253



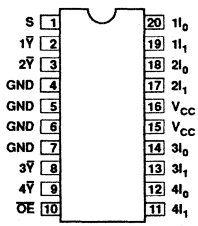
Dual 4-Input Multiplexer; 3-State

11257



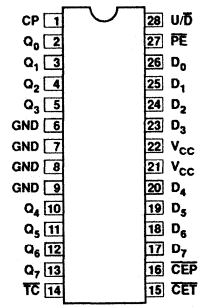
Quad 2-Input Multiplexer; 3-State

11258



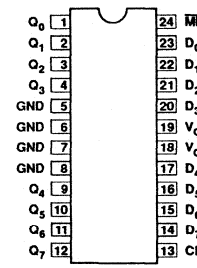
Quad 2-Input Multiplexer; 3-State; INV

11269



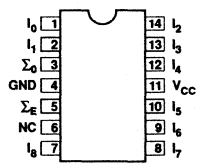
Synchronous Presettable 8-Bit Binary Up/Down Counter

11273



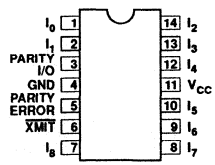
Octal D-Type Flip-Flop with Reset

11280



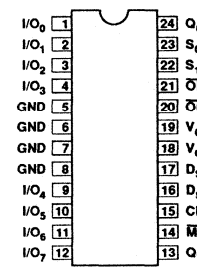
9-Bit Odd/Even Parity Generator/Checker

11286



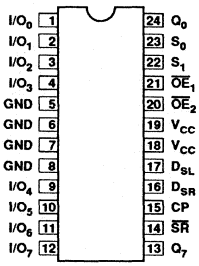
9-Bit Odd/Even Parity Generator/ Checker with Bus Drive I/O Port

11299



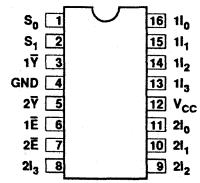
8-Input Universal Shift/Storage Register with Asynchronous Reset and Common I/O Pins

11323



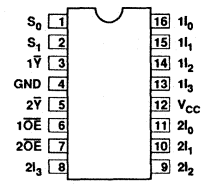
8-Input Universal Shift/Storage Register with Asynchronous Reset and Common I/O Pins

11352



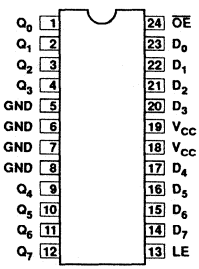
Dual 4-Input Multiplexer; INV

11353



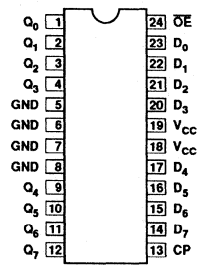
Dual 4-Input Multiplexer; 3-State; INV

11373



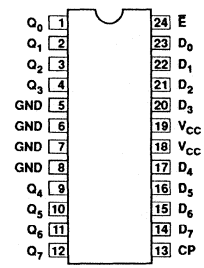
Octal D-Type Transparent Latch; 3-State

11374



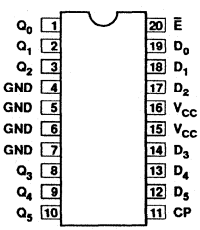
Octal D-Type Flip-Flop; Positive-Edge Trigger; 3-State

11377



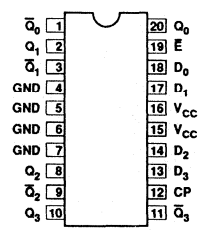
Octal D-Type Flip-Flop with Enable

11378



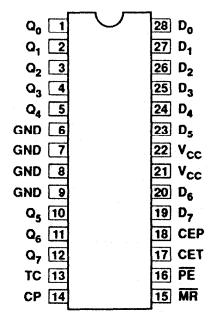
Hex D-Type Flip-Flop with Enable; Positive-Edge Trigger

11379



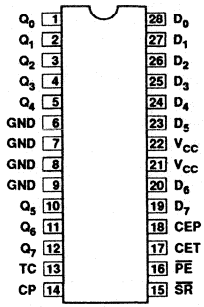
Quad D-Type Flip-Flop with Data Enable

11461



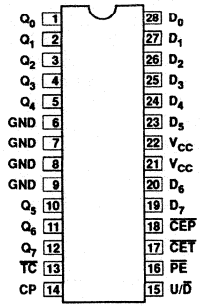
Synchronous Presettable Synchronous 8-Bit Binary Counter; Asynchronous Reset

11463



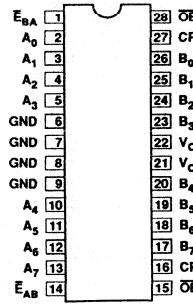
Synchronous Presettable Synchronous 8-Bit Binary Counter; Synchronous Reset

11469



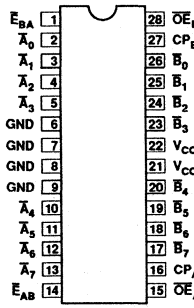
Synchronous Presettable Synchronous 8-Bit Binary Up/Down Counter

11470



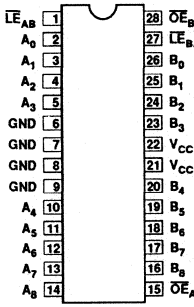
Octal Transceiver/Register with Dual Enable; 3-State

11471



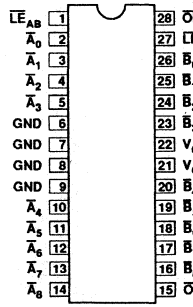
Octal Transceiver/Register with Dual Enable; 3-State; INV

11472



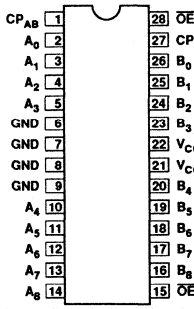
9-Wide Latched Transceiver with Dual Enable; 3-State

11473



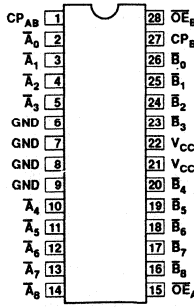
9-Wide Latched Transceiver with Dual Enable; 3-State; INV

11474



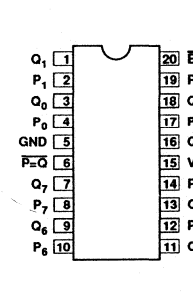
9-Wide Transceiver/Register with Dual Enable; 3-State

11475



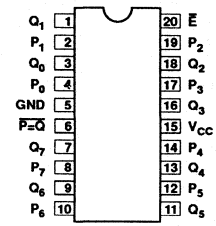
9-Wide Transceiver/Register with Dual Enable; 3-State; INV

11520



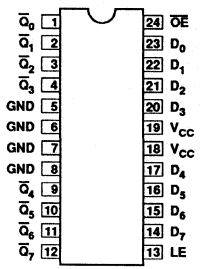
8-Bit Identity Comparator with Input Pull-Up

11521



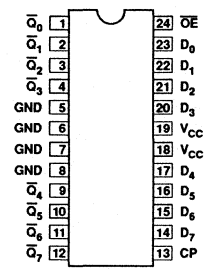
8-Bit Identity Comparator

11533



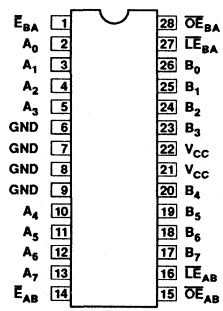
Octal D-Type Transparent Latch; 3-State; INV

11534



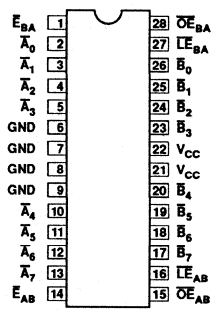
Octal D-Type Flip-Flop; Positive-Edge Trigger; 3-State; INV

11543



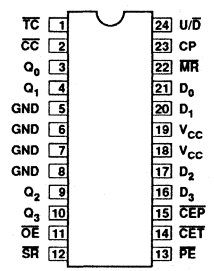
Octal Latched Transceiver with Dual Enable; 3-State

11544



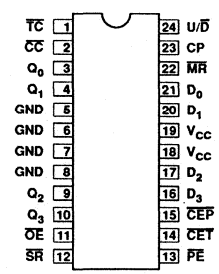
Octal Latched Transceiver with Dual Enable; 3-State; INV

11568



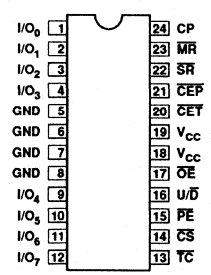
Synchronous Presettable BCD Decade Up/Down Counter with Synchronous and Asynchronous Reset

11569



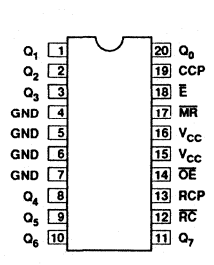
Synchronous Presettable 4-Bit Binary Up/Down Counter with Synchronous and Asynchronous Reset

11579



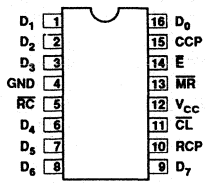
8-Bit Binary Up/Down Counter with Common I/O Pins; Synchronous and Asynchronous Reset; 3-State

11590



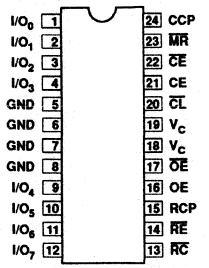
Synchronous 8-Bit Binary Counter with Output Registers; Asynchronous Reset

11592



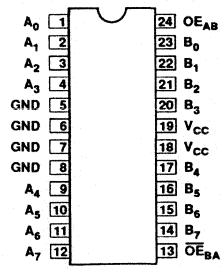
Synchronous 8-Bit Binary Counter with Input Registers; Asynchronous Reset

11593



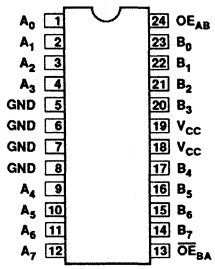
Synchronous 8-Bit Binary Counter with Input Registers; Asynchronous Reset

11620



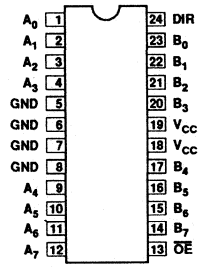
Octal Transceiver with Dual Enable; 3-State; INV

11623



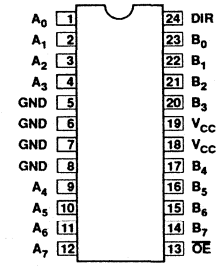
Octal Transceiver with Dual Enable; 3-State

11640



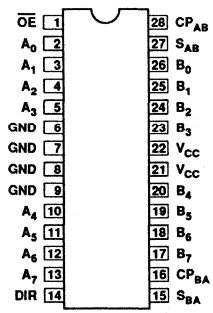
Octal Transceiver with Direction Pin; 3-State; INV

11643



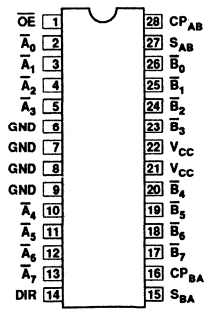
Octal Transceiver; 3-State; True/Inverting

11646



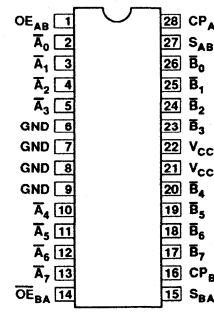
Octal Transceiver/Register with Direction Pin; 3-State

11648



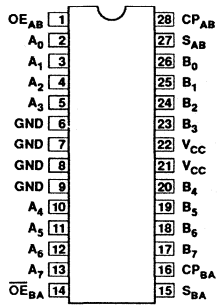
Octal Transceiver/Register with Direction Pin; 3-State; INV

11651



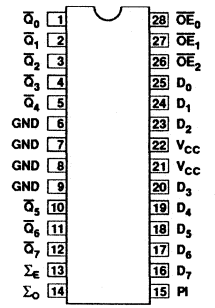
Octal Transceiver/Register with Dual Enable; 3-State; INV

11652



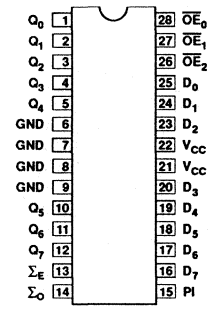
Octal Transceiver/Register with Dual Enable; 3-State

11655



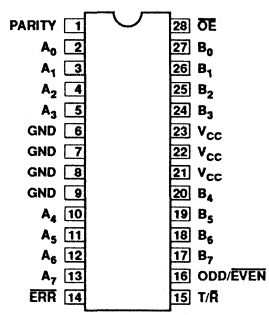
Octal Buffer/Line Driver with 9-Bit Parity Generator/Checker; 3-State; INV

11656



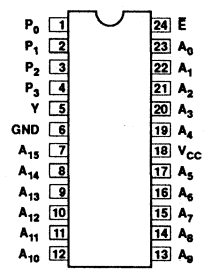
Octal Buffer/Line Driver with 9-Bit Parity Generator/Checker; 3-State

11657



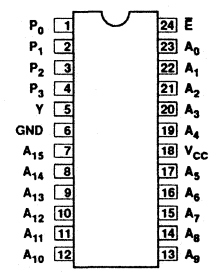
Octal Transceiver with 8-Bit Parity Checker/Generator

11677



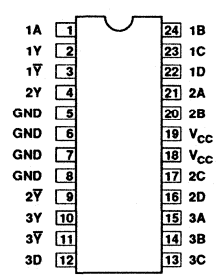
16-Bit Address Comparator with Enable

11678



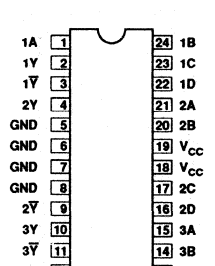
16-Bit Address Comparator with Output Latch

11800



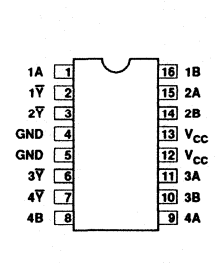
Triple 4-Input AND/NAND Gate

11802



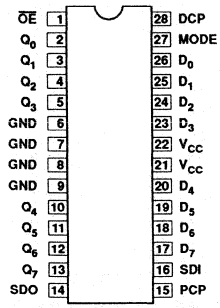
Triple 4-Input OR/NOR Gate

11810



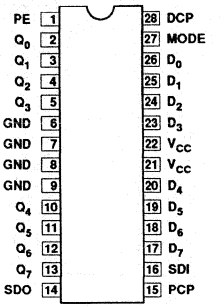
Quad 2-Input Exclusive-NOR Gate

11818



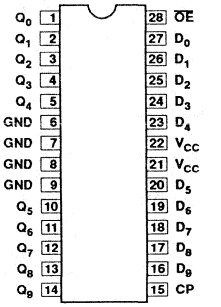
8-Bit Diagnostic/Pipe-Line Register

11819



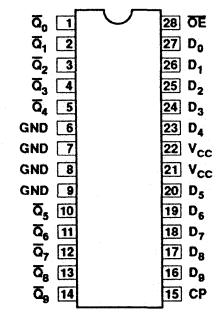
8-Bit Diagnostic/Pipe-Line Register with Parity Even Output

11821



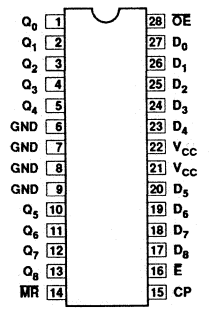
10-Wide D-Type Flip-Flop; Positive-Edge Trigger; 3-State

11822



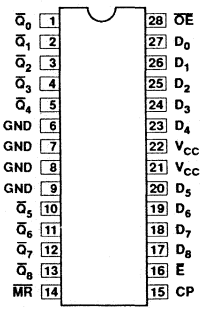
10-Wide D-Type Flip-Flop; Positive-Edge Trigger; 3-State; INV

11823



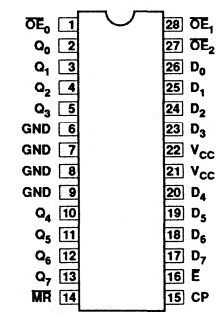
9-Wide D-Type Flip-Flop with Reset and Enable; Positive-Edge Trigger; 3-State

11824



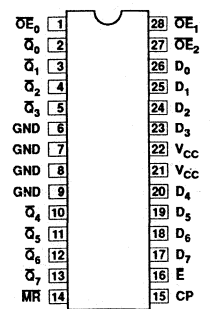
9-Wide D-Type Flip-Flop with Reset and Enable; Positive-Edge Trigger; 3-State; INV

11825



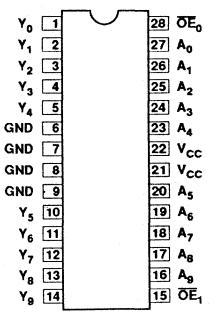
Octal D-Type Flip-Flop with Reset and Enable; Positive-Edge Trigger; 3-State

11826



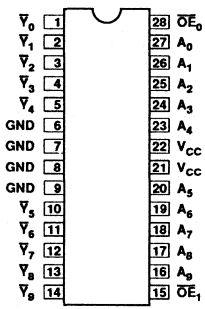
Octal D-Type Flip-Flop with Reset and Enable; Positive-Edge Trigger; 3-State; INV

11827



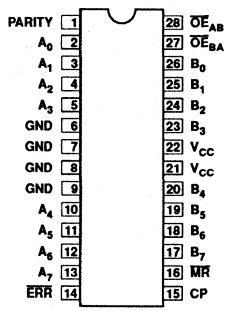
10-Wide Buffer/Line Driver; 3-State

11828



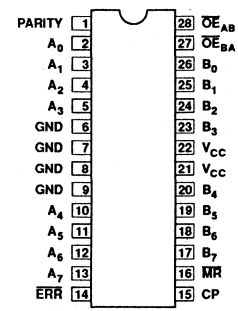
10-Wide Buffer/Line Driver; 3-State; INV

11833



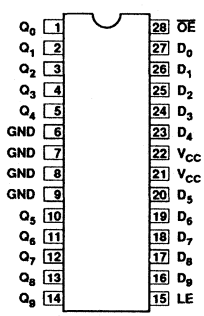
8-Bit Transceiver with 9-Bit Parity Checker/Generator and Error Flip-Flop

11834



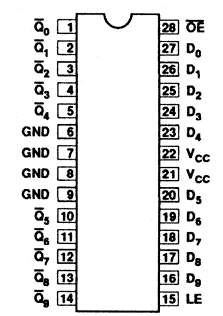
8-Bit Inverting Transceiver with 9-Bit Parity Checker/Generator and Error Flip-Flop

11841



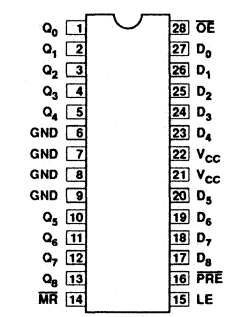
10-Wide D-Type Transparent Latch; 3-State

11842



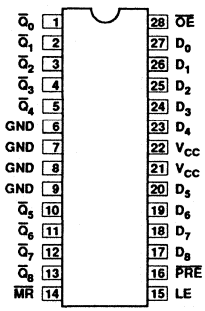
10-Wide D-Type Transparent Latch; 3-State; INV

11843



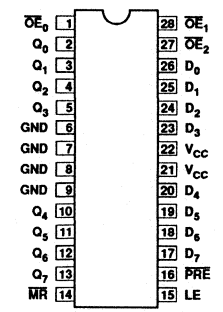
9-Wide D-Type Transparent Latch with Set and Reset; 3-State

11844



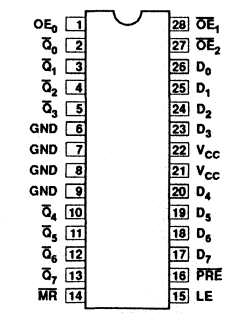
9-Wide D-Type Transparent Latch with Set and Reset; 3-State; INV

11845



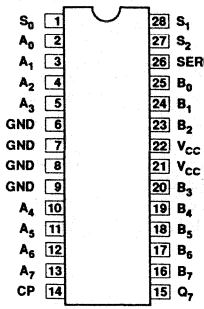
Octal D-Type Transparent Latch with Set and Reset; 3-State

11846



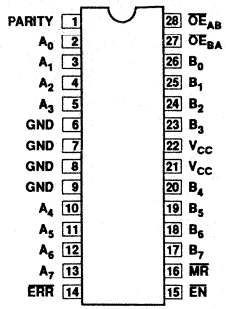
Octal D-Type Transparent Latch with Set and Reset; 3-State; INV

11852



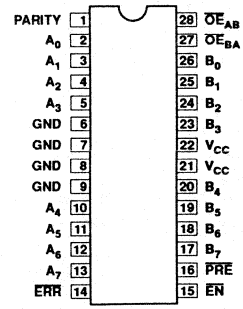
8-Bit Universal Transceiver Port Controller

11853



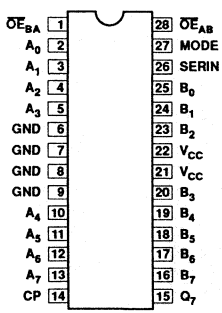
8-Bit Transceiver with 9-Bit Parity Checker/Generator and Error Flag Latch

11854



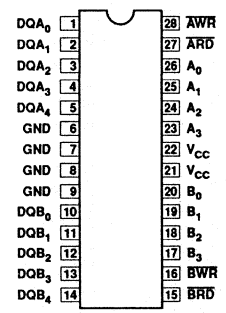
8-Bit Inverting Transceiver with 9-Bit Parity Checker/Generator and Error Flag Latch

11856



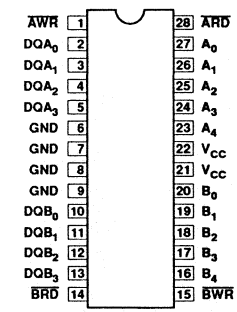
8-Bit Universal Transceiver Port Controller

11858



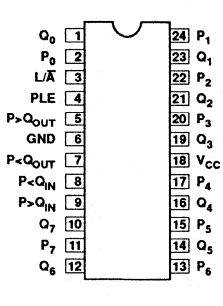
16-Word by 5-Bit Dual Port Register

11859



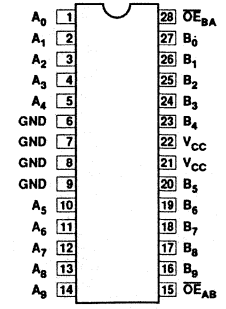
32-Word by 4-Bit Dual Port Register

11860



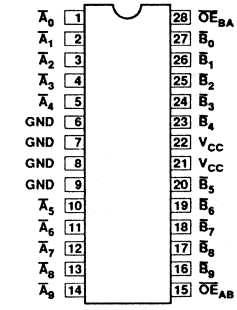
8-Bit Magnitude Comparator

11861



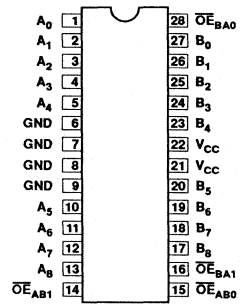
10-Wide Transceiver; 3-State

11862



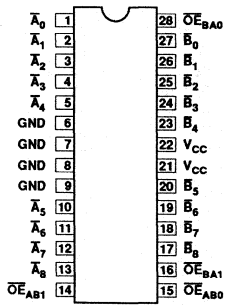
10-Wide Transceiver; 3-State; INV

11863



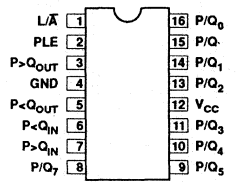
9-Wide Transceiver; 3-State

11864



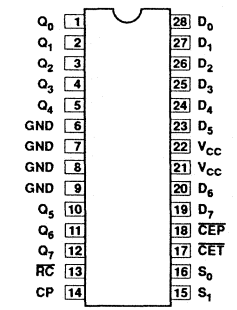
9-Wide Transceiver; 3-State; INV

11865



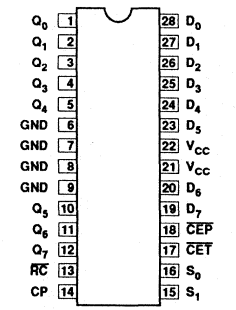
8-Bit Magnitude Comparator

11867



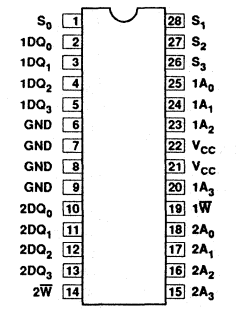
Synchronous Presettable Synchronous 8-Bit Binary Up/Down Counter; Asynchronous Reset

11869



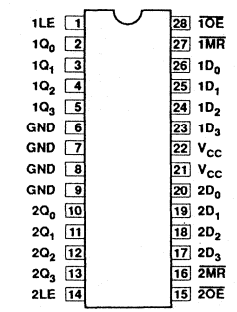
Synchronous Presettable Synchronous 8-Bit Binary Up/Down Counter; Synchronous Reset

11870



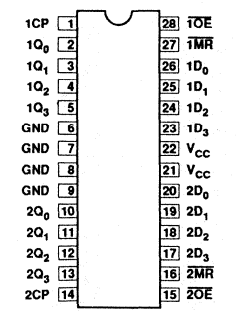
14-Word by 4-Bit Register

11873



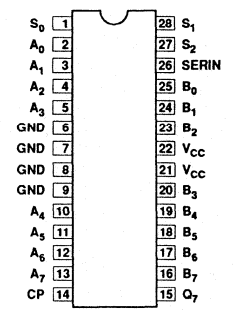
Dual D-Type 4-Bit Transparent Latch with Reset; 3-State

11874



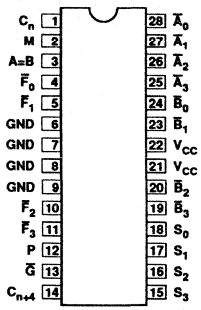
Dual D-Type 4-Bit Flip-Flop Latch with Reset; 3-State

11877



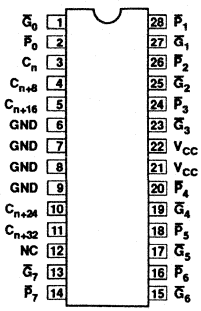
8-Bit Universal Transceiver Port Controller

11881



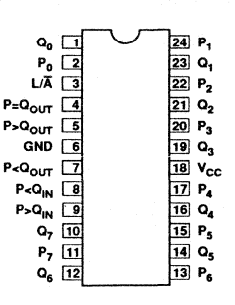
4-Bit Arithmetic Logic Unit with Status Check Register

11882



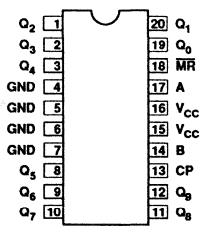
32-Bit Look-Ahead Carry Generator

11885



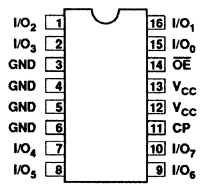
8-Bit Magnitude Comparator

11898



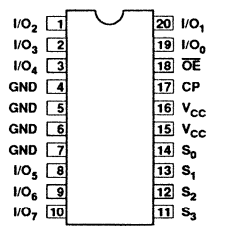
10-Bit Serial-In Parallel-Out Shift Register

11979



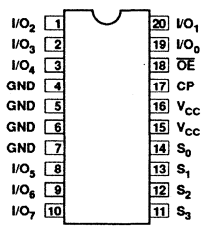
8-Bit Multiplexed I/O Read-Back Register

11980



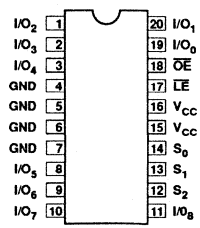
16-Word by 8-Bit Register Multiplexed I/O Read-Back Register

11981



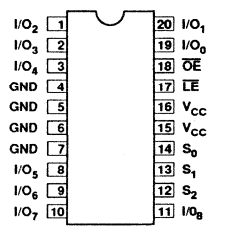
16-Word by 8-Bit Multiplexed I/O Read-Back Register with Address Latch

11987



8-Word by 9-Bit Multiplexed I/O Read-Back Register

11988



8-Word by 9-Bit Multiplexed I/O Read-Back Register with Address Latch

Section 5
ACL Data Sheets

74AC/ACT11000

Quad 2-Input NAND Gate

Product Specification

FEATURES

- **Output capability: ±24 mA**
- **CMOS (AC) and TTL (ACT) voltage level inputs**
- **50Ω incident wave switching**
- **Center-pin V_{CC} and ground configuration to minimize high-speed switching noise**
- **I_{CC} category: SSI**

DESCRIPTION

The 74AC/ACT11000 high-performance CMOS devices combine very high speed and high output drive comparable to the most advanced TTL families.

The 74AC/ACT11000 provides four separate 2-input NAND gate functions.

GENERAL INFORMATION

SYMBOL	PARAMETER	CONDITIONS T_A = 25°C; GND = 0V; V_{CC} = 5.0V	TYPICAL		UNIT
			AC	ACT	
t_{PLH}/t_{PHL}	Propagation delay A, B, to $\overline{Y}$	C_L = 50pF	4.7	6.5	ns
C_{PD}	Power dissipation capacitance per gate[1]	f = 1MHz; C_L = 50pF	33	23	pF
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	3.5	3.5	pF
I_{LATCH}	Latch-up current	Per Jedec JC40.2 Standard 17	500	500	mA

Note:

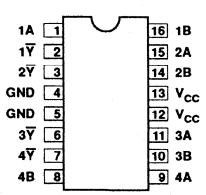
1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_I + \Sigma (C_L \times V_{CC}^2 \times f_O)$ where:
   f_I = input frequency in MHz, C_L = output load capacitance in pF,
   f_O = output frequency in MHz, V_{CC} = supply voltage in V,
   $\Sigma (C_L \times V_{CC}^2 \times f_O)$ = sum of outputs

ORDERING INFORMATION

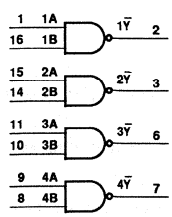
PACKAGES	TEMPERATURE RANGE	ORDER CODE
16-pin plastic DIP (300mil-wide)	-40°C to +85°C	74AC11000N 74ACT11000N
16-pin plastic SO (150mil-wide)	-40°C to +85°C	74AC11000D 74ACT11000D

PIN CONFIGURATION

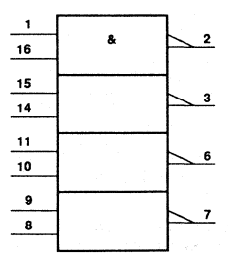
N and D Packages



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
1, 15, 11, 9	1A - 4A	Data inputs
16, 14, 10, 8	1B - 4B	Data inputs
2, 3, 6, 7	$1\overline{Y}$ - $4\overline{Y}$	Data outputs
4, 5	GND	Ground (0V)
12, 13	V_{CC}	Positive supply voltage

FUNCTION TABLE

INPUTS		OUTPUT
nA	nB	$n\overline{Y}$
L	L	H
L	H	H
H	L	H
H	H	L

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	74AC11000			74ACT11000			UNIT
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	DC supply voltage	3.0[1]	5.0	5.5	4.5	5.0	5.5	V
V_I	Input voltage	0		V_{CC}	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	0		V_{CC}	V
$\Delta t/\Delta v$	Input transition rise or fall rate	0		10	0		10	ns/V
T_A	Operating free-air temperature	-40		+85	-40		+85	°C

NOTE:
1. No electrical or switching characteristics are specified at V_{CC} < 3V. Operation between 2V and 3V is not recommended, but within that range, a device output will maintain a previously established logic state.

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	TEST CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 to+7.0	V
I_{IK} or V_I	DC input diode current[2]	$V_I < 0$	-20	mA
		$V_I > V_{CC}$	20	
	DC input voltage		-0.5 to V_{CC} +0.5	V
I_{OK} or V_O	DC output diode current[2]	$V_O < 0$	-50	mA
		$V_O > V_{CC}$	50	
	DC output voltage		-0.5 to V_{CC} +0.5	V
I_O	DC output source or sink current per output pin	V_O = 0 to V_{CC}	±50	mA
I_{CC} or I_{GND}	DC V_{CC} current		±100	mA
	DC ground current		±100	
T_{STG}	Storage temperature		-65 to 150	°C
P_{TOT}	Power dissipation per package Plastic DIP	Above 70°C:derate linearly by 8mW/K	500	mW
	Power dissipation per package Plastic surface mount (SO)	Above 70°C:derate linearly by 6mW/K	400	mW

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		V_{CC}	74AC11000				74ACT11000				UNIT
					T_A = +25°C		T_A = -40°C to +85°C		T_A = +25°C		T_A = -40°C to +85°C		
				V	Min	Max	Min	Max	Min	Max	Min	Max	
V_{IH}	High-level input voltage			3.0	2.10		2.10						V
				4.5	3.15		3.15		2.0		2.0		
				5.5	3.85		3.85		2.0		2.0		
V_{IL}	Low-level input voltage			3.0		0.90		0.90					V
				4.5		1.35		1.35		0.8		0.8	
				5.5		1.65		1.65		0.8		0.8	
V_{OH}	High-level output voltage	V_I = V_{IL} or V_{IH}	I_{OH} = -50μA	3.0	2.9		2.9						V
				4.5	4.4		4.4		4.4		4.4		
				5.5	5.4		5.4		5.4		5.4		
			I_{OH} = -4mA	3.0	2.58		2.48						
			I_{OH} = -24mA	4.5	3.94		3.8		3.94		3.8		
				5.5	4.94		4.8		4.94		4.8		
			I_{OH} = -75mA[1]	5.5			3.85				3.85		
V_{OL}	Low-level output voltage	V_I = V_{IL} or V_{IH}	I_{OL} = 50μA	3.0		0.1		0.1					V
				4.5		0.1		0.1		0.1		0.1	
				5.5		0.1		0.1		0.1		0.1	
			I_{OL} = 12mA	3.0		0.36		0.44					
			I_{OL} = 24mA	4.5		0.36		0.44		0.36		0.44	
				5.5		0.36		0.44		0.36		0.44	
			I_{OL} = 75mA[1]	5.5				1.65				1.65	
I_I	Input leakage current	V_I = V_{CC} or GND		5.5		±0.1		±1.0		±0.1		±1.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC} or GND, I_O = 0		5.5		4.0		40		4.0		40	μA
ΔI_{CC}	Supply current, TTL inputs High[2]	One input at 3.4V, other inputs at V_{CC} or GND		5.5						0.9		1.0	mA

NOTES:
1. Not more than one output should be tested at a time, and the duration of the test should not exceed 10ms.
2. This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0V or V_{CC}.

AC ELECTRICAL CHARACTERISTICS AT 3.3V ±0.3V

SYMBOL	PARAMETER	WAVEFORM	74AC11000					UNIT
			T_A = +25°C			T_A = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay nA, nB to n$\overline{Y}$	1	1.5 1.5	7.2 5.8	9.8 8.6	1.5 1.5	11.1 9.6	ns

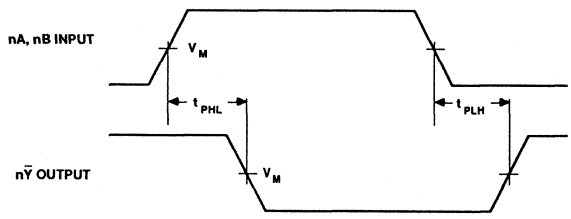
AC ELECTRICAL CHARACTERISTICS AT 5.0V ±0.5V

SYMBOL	PARAMETER	WAVEFORM	74AC11000					UNIT
			T_A = +25°C			T_A = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay nA, nB to n$\overline{Y}$	1	1.5 1.5	5.0 4.4	6.5 6.1	1.5 1.5	7.4 6.8	ns

AC ELECTRICAL CHARACTERISTICS AT 5.0V ±0.5V

SYMBOL	PARAMETER	WAVEFORM	74ACT11000					UNIT
			T_A = +25°C			T_A = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay nA, nB to n$\overline{Y}$	1	1.5 1.5	7.2 5.8	10.9 8.0	1.5 1.5	12.3 8.8	ns

AC WAVEFORMS

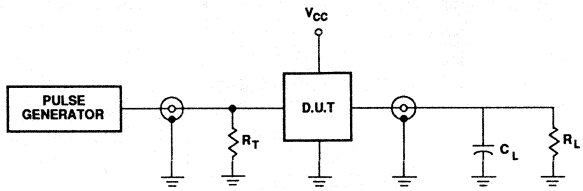


Waveform 1. Waveforms Showing the Input (nA, nB) to Output (n$\overline{Y}$) Propagation Delays

WAVEFORM CONDITIONS

	INPUTS	OUTPUTS
AC	V_{IN} = GND to V_{CC}, V_M = 50% V_{CC}	V_{OUT} = V_{OL} to V_{OH}
ACT	V_{IN} = GND to 3.0V, V_M = 1.5V	V_M = 50% V_{CC}

TEST CIRCUIT



Test Circuit

DEFINITIONS

C_L = Load capacitance, 50pF; includes jig and probe capacitance

R_L = Load resistor, 500Ω

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators

Input pulses: PRR ≤ 10MHz

$t_r = t_f = 3ns$

74AC/ACT11002

Quad 2-Input NOR Gate

Product Specification

FEATURES

- **Output capability: ±24 mA**
- **CMOS (AC) and TTL (ACT) voltage level inputs**
- **50Ω incident wave switching**
- **Center-pin V_{CC} and ground configuration to minimize high-speed switching noise**
- **I_{CC} category: SSI**

DESCRIPTION

The 74AC/ACT11002 high-performance CMOS devices combine very high speed and high output drive comparable to the most advanced TTL families.

The 74AC/ACT11002 provides four separate 2-input NOR gate functions.

GENERAL INFORMATION

SYMBOL	PARAMETER	CONDITIONS T_A = 25°C; GND = 0V; V_{CC} = 5.0V	TYPICAL		UNIT
			AC	ACT	
t_{PLH}/t_{PHL}	Propagation delay A, B, to $\overline{Y}$	C_L = 50pF	4.3	5.7	ns
C_{PD}	Power dissipation capacitance per gate[1]	f = 1MHz; C_L = 50pF	32	29	pF
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	3.5	3.5	pF
I_{LATCH}	Latch-up current	Per Jedec JC40.2 Standard 17	500	500	mA

Note:

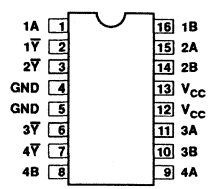
1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_I + \Sigma (C_L \times V_{CC}^2 \times f_O)$ where:
   f_I = input frequency in MHz, C_L = output load capacitance in pF,
   f_O = output frequency in MHz, V_{CC} = supply voltage in V,
   $\Sigma (C_L \times V_{CC}^2 \times f_O)$ = sum of outputs

ORDERING INFORMATION

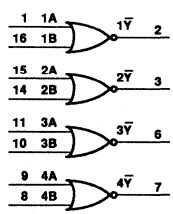
PACKAGES	TEMPERATURE RANGE	ORDER CODE
16-pin plastic DIP (300mil-wide)	-40°C to +85°C	74AC11002N 74ACT11002N
16-pin plastic SO (150mil-wide)	-40°C to +85°C	74AC11002D 74ACT11002D

PIN CONFIGURATION

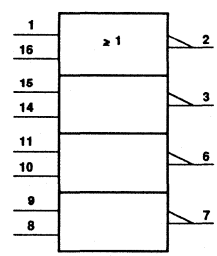
N and D Packages



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
1, 15, 11, 9	1A - 4A	Data inputs
16, 14, 10, 8	1B - 4B	Data inputs
2, 3, 6, 7	$1\overline{Y}$ - $4\overline{Y}$	Data outputs
4, 5	GND	Ground (0V)
12, 13	V_{CC}	Positive supply voltage

FUNCTION TABLE

INPUTS		OUTPUT
nA	nB	$n\overline{Y}$
L	L	H
L	H	L
H	L	L
H	H	L

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	74AC11002			74ACT11002			UNIT
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	DC supply voltage	3.0[1]	5.0	5.5	4.5	5.0	5.5	V
V_I	Input voltage	0		V_{CC}	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	0		V_{CC}	V
$\Delta t/\Delta v$	Input transition rise or fall rate	0		10	0		10	ns/V
T_A	Operating free-air temperature	-40		+85	-40		+85	°C

NOTE:

1. No electrical or switching characteristics are specified at $V_{CC} < 3V$. Operation between 2V and 3V is not recommended, but within that range, a device output will maintain a previously established logic state.

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	TEST CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 to+7.0	V
I_{IK} or V_I	DC input diode current[2]	$V_I < 0$	-20	mA
		$V_I > V_{CC}$	20	
	DC input voltage		-0.5 to V_{CC} +0.5	V
I_{OK} or V_O	DC output diode current[2]	$V_O < 0$	-50	mA
		$V_O > V_{CC}$	50	
	DC output voltage		-0.5 to V_{CC} +0.5	V
I_O	DC output source or sink current per output pin	V_O = 0 to V_{CC}	±50	mA
I_{CC} or I_{GND}	DC V_{CC} current		±100	mA
	DC ground current		±100	
T_{STG}	Storage temperature		-65 to 150	°C
P_{TOT}	Power dissipation per package Plastic DIP	Above 70°C:derate linearly by 8mW/K	500	mW
	Power dissipation per package Plastic surface mount (SO)	Above 70°C:derate linearly by 6mW/K	400	mW

NOTES:

1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		V_{CC}	74AC11002				74ACT11002				UNIT
					T_A = +25°C		T_A = -40°C to +85°C		T_A = +25°C		T_A = -40°C to +85°C		
				V	Min	Max	Min	Max	Min	Max	Min	Max	
V_{IH}	High-level input voltage			3.0	2.10		2.10						V
				4.5	3.15		3.15		2.0		2.0		
				5.5	3.85		3.85		2.0		2.0		
V_{IL}	Low-level input voltage			3.0		0.90		0.90					V
				4.5		1.35		1.35		0.8		0.8	
				5.5		1.65		1.65		0.8		0.8	
V_{OH}	High-level output voltage	V_I = V_{IL} or V_{IH}	I_{OH} = -50μA	3.0	2.9		2.9						V
				4.5	4.4		4.4		4.4		4.4		
				5.5	5.4		5.4		5.4		5.4		
			I_{OH} = -4mA	3.0	2.58		2.48						
			I_{OH} = -24mA	4.5	3.94		3.8		3.94		3.8		
				5.5	4.94		4.8		4.94		4.8		
			I_{OH} = -75mA[1]	5.5			3.85				3.85		
V_{OL}	Low-level output voltage	V_I = V_{IL} or V_{IH}	I_{OL} = 50μA	3.0		0.1		0.1					V
				4.5		0.1		0.1		0.1		0.1	
				5.5		0.1		0.1		0.1		0.1	
			I_{OL} = 12mA	3.0		0.36		0.44					
			I_{OL} = 24mA	4.5		0.36		0.44		0.36		0.44	
				5.5		0.36		0.44		0.36		0.44	
			I_{OL} = 75mA[1]	5.5				1.65				1.65	
I_I	Input leakage current	V_I = V_{CC} or GND		5.5		±0.1		±1.0		±0.1		±1.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC} or GND, I_O = 0		5.5		4.0		40		4.0		40	μA
ΔI_{CC}	Supply current, TTL inputs High[2]	One input at 3.4V, other inputs at V_{CC} or GND		5.5						0.9		1.0	mA

NOTES:
1. Not more than one output should be tested at a time, and the duration of the test should not exceed 10ms.
2. This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0V or V_{CC}.

AC ELECTRICAL CHARACTERISTICS AT 3.3V ±0.3V

SYMBOL	PARAMETER	WAVEFORM	74AC11002					UNIT
			T_A = +25°C			T_A = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay nA, nB to n$\overline{Y}$	1	1.5 1.5	7.0 6.0	8.6 7.5	1.5 1.5	9.9 8.4	ns

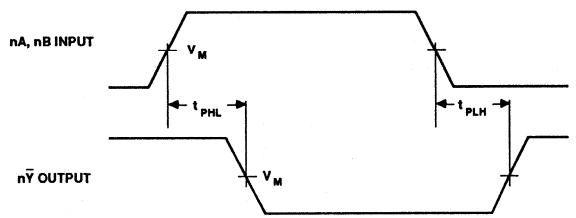
AC ELECTRICAL CHARACTERISTICS AT 5.0V ±0.5V

SYMBOL	PARAMETER	WAVEFORM	74AC11002					UNIT
			T_A = +25°C			T_A = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay nA, nB to n$\overline{Y}$	1	1.5 1.5	4.5 4.0	6.1 5.7	1.5 1.5	6.9 6.4	ns

AC ELECTRICAL CHARACTERISTICS AT 5.0V ±0.5V

SYMBOL	PARAMETER	WAVEFORM	74ACT11002					UNIT
			T_A = +25°C			T_A = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay nA, nB to n$\overline{Y}$	1	1.5 1.5	6.1 5.3	9.4 7.8	1.5 1.5	10.6 8.7	ns

AC WAVEFORMS

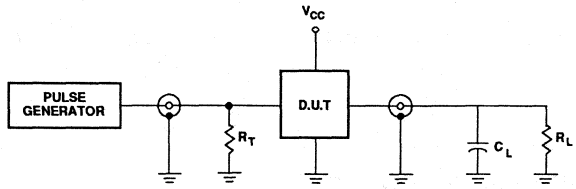


Waveform 1. Waveforms Showing the Input (nA, nB) to Output (n$\overline{Y}$) Propagation Delays

WAVEFORM CONDITIONS

	INPUTS	OUTPUTS
AC	V_{IN} = GND to V_{CC}, V_M = 50% V_{CC}	V_{OUT} = V_{OL} to V_{OH}
ACT	V_{IN} = GND to 3.0V, V_M = 1.5V	V_M = 50% V_{CC}

TEST CIRCUIT



Test Circuit

DEFINITIONS

C_L = Load capacitance, 50pF; includes jig and probe capacitance

R_L = Load resistor, 500Ω

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators

Input pulses: PRR ≤ 10MHz

$t_r = t_f = 3ns$

74AC/ACT11004

Hex Inverter

Product Specification

FEATURES

- **Output capability: ±24 mA**
- **CMOS (AC) and TTL (ACT) voltage level inputs**
- **50Ω incident wave switching**
- **Center-pin V_{CC} and ground configuration to minimize high-speed switching noise**
- **I_{CC} category: SSI**

DESCRIPTION

The 74AC/ACT11004 high-performance CMOS devices combine very high speed and high output drive comparable to the most advanced TTL families.

The 74AC/ACT11004 provides six separate inverters.

GENERAL INFORMATION

SYMBOL	PARAMETER	CONDITIONS T_A = 25°C; GND = 0V; V_{CC} = 5.0V	TYPICAL		UNIT
			AC	ACT	
t_{PLH}/ t_{PHL}	Propagation delay A, B, to $\overline{Y}$	C_L = 50pF	4.0	5.9	ns
C_{PD}	Power dissipation capacitance per gate[1]	f = 1MHz; C_L = 50pF	19	26	pF
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	3.5	3.5	pF
I_{LATCH}	Latch-up current	Per Jedec JC40.2 Standard 17	500	500	mA

Note:

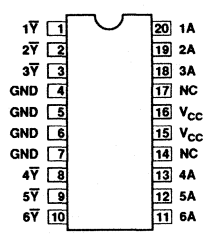
1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_I + \Sigma (C_L \times V_{CC}^2 \times f_O)$ where:
   f_I = input frequency in MHz, C_L = output load capacitance in pF,
   f_O = output frequency in MHz, V_{CC} = supply voltage in V,
   $\Sigma (C_L \times V_{CC}^2 \times f_O)$ = sum of outputs

ORDERING INFORMATION

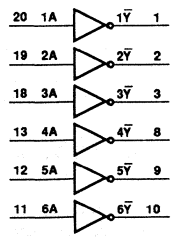
PACKAGES	TEMPERATURE RANGE	ORDER CODE
20-pin plastic DIP (300mil-wide)	-40°C to +85°C	74AC11004N 74ACT11004N
20-pin plastic SO (300mil-wide)	-40°C to +85°C	74AC11004D 74ACT11004D

PIN CONFIGURATION

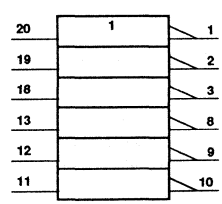
N and D Packages



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
20, 19, 18, 13, 12, 11	1A - 6A	Data inputs
1, 2, 3, 8, 9, 10	$1\overline{Y}$ - $6\overline{Y}$	Data outputs
4, 5, 6, 7	GND	Ground (0V)
15, 16	V_{CC}	Positive supply voltage

INPUT	OUTPUT
nA	$n\overline{Y}$
L	H
H	L

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	74AC11004			74ACT11004			UNIT
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	DC supply voltage	3.0[1]	5.0	5.5	4.5	5.0	5.5	V
V_I	Input voltage	0		V_{CC}	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	0		V_{CC}	V
$\Delta t/\Delta v$	Input transition rise or fall rate	0		10	0		10	ns/V
T_A	Operating free-air temperature	-40		+85	-40		+85	°C

NOTE:

1. No electrical or switching characteristics are specified at $V_{CC} < 3V$. Operation between 2V and 3V is not recommended, but within that range, a device output will maintain a previously established logic state.

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	TEST CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 to+7.0	V
I_{IK} or V_I	DC input diode current[2]	$V_I < 0$	-20	mA
		$V_I > V_{CC}$	20	
	DC input voltage		-0.5 to V_{CC} +0.5	V
I_{OK} or V_O	DC output diode current[2]	$V_O < 0$	-50	mA
		$V_O > V_{CC}$	50	
	DC output voltage		-0.5 to V_{CC} +0.5	V
I_O	DC output source or sink current per output pin	V_O = 0 to V_{CC}	±50	mA
I_{CC} or I_{GND}	DC V_{CC} current		±150	mA
	DC ground current		±150	
T_{STG}	Storage temperature		-65 to 150	°C
P_{TOT}	Power dissipation per package Plastic DIP	Above 70°C:derate linearly by 8mW/K	500	mW
	Power dissipation per package Plastic surface mount (SO)	Above 70°C:derate linearly by 6mW/K	400	mW

NOTES:

1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		V_{CC}	74AC11004				74ACT11004				UNIT
					T_A = +25°C		T_A = -40°C to +85°C		T_A = +25°C		T_A = -40°C to +85°C		
				V	Min	Max	Min	Max	Min	Max	Min	Max	
V_{IH}	High-level input voltage			3.0	2.10		2.10						V
				4.5	3.15		3.15		2.0		2.0		
				5.5	3.85		3.85		2.0		2.0		
V_{IL}	Low-level input voltage			3.0		0.90		0.90					V
				4.5		1.35		1.35		0.8		0.8	
				5.5		1.65		1.65		0.8		0.8	
V_{OH}	High-level output voltage	V_I = V_{IL} or V_{IH}	I_{OH} = -50μA	3.0	2.9		2.9						V
				4.5	4.4		4.4		4.4		4.4		
				5.5	5.4		5.4		5.4		5.4		
			I_{OH} = -4mA	3.0	2.58		2.48						
			I_{OH} = -24mA	4.5	3.94		3.8		3.94		3.8		
				5.5	4.94		4.8		4.94		4.8		
			I_{OH} = -75mA[1]	5.5			3.85				3.85		
V_{OL}	Low-level output voltage	V_I = V_{IL} or V_{IH}	I_{OL} = 50μA	3.0		0.1		0.1					V
				4.5		0.1		0.1		0.1		0.1	
				5.5		0.1		0.1		0.1		0.1	
			I_{OL} = 12mA	3.0		0.36		0.44					
			I_{OL} = 24mA	4.5		0.36		0.44		0.36		0.44	
				5.5		0.36		0.44		0.36		0.44	
			I_{OL} = 75mA[1]	5.5				1.65				1.65	
I_I	Input leakage current	V_I = V_{CC} or GND		5.5		±0.1		±1.0		±0.1		±1.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC} or GND, I_O = 0		5.5		4.0		40		4.0		40	μA
ΔI_{CC}	Supply current, TTL inputs High[2]	One input at 3.4V, other inputs at V_{CC} or GND		5.5						0.9		1.0	mA

NOTES:
1. Not more than one output should be tested at a time, and the duration of the test should not exceed 10ms.
2. This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0V or V_{CC}.

AC ELECTRICAL CHARACTERISTICS AT 3.3V ±0.3V

SYMBOL	PARAMETER	WAVEFORM	74AC11004					UNIT
			T_A = +25°C			T_A = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay nA, nB to n$\overline{Y}$	1	1.5 1.5	6.1 5.2	9.0 7.4	1.5 1.5	10.0 8.2	ns

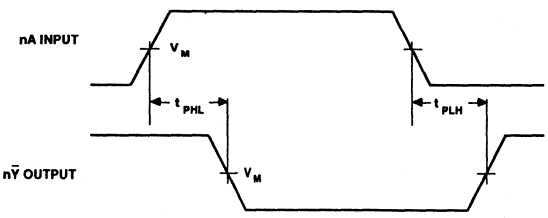
AC ELECTRICAL CHARACTERISTICS AT 5.0V ±0.5V

SYMBOL	PARAMETER	WAVEFORM	74AC11004					UNIT
			T_A = +25°C			T_A = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay nA, nB to n$\overline{Y}$	1	1.5 1.5	4.2 3.8	6.3 5.5	1.5 1.5	7.1 6.0	ns

AC ELECTRICAL CHARACTERISTICS AT 5.0V ±0.5V

SYMBOL	PARAMETER	WAVEFORM	74ACT11004					UNIT
			T_A = +25°C			T_A = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay nA, nB to n$\overline{Y}$	1	1.5 1.5	5.3 6.4	9.0 8.7	1.5 1.5	9.7 9.6	ns

AC WAVEFORMS

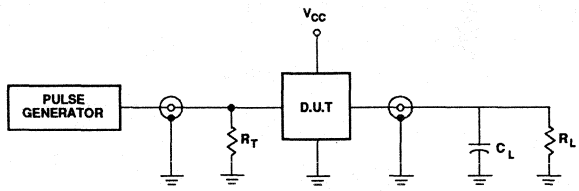


Waveform 1. Waveforms Showing the Input (nA) to Output (n$\overline{Y}$) Propagation Delays

WAVEFORM CONDITIONS

	INPUTS	OUTPUTS
AC	V_{IN} = GND to V_{CC}, V_M = 50% V_{CC}	V_{OUT} = V_{OL} to V_{OH}
ACT	V_{IN} = GND to 3.0V, V_M = 1.5V	V_M = 50% V_{CC}

TEST CIRCUIT



Test Circuit

DEFINITIONS

C_L = Load capacitance, 50pF; includes jig and probe capacitance

R_L = Load resistor, 500Ω

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators

Input pulses: PRR ≤ 10MHz

$t_r = t_f$ = 3ns

74AC/ACT11008

Quad 2-Input AND Gate

Product Specification

FEATURES

- **Output capability: ±24 mA**
- **CMOS (AC) and TTL (ACT) voltage level inputs**
- **50Ω incident wave switching**
- **Center-pin V_{CC} and ground configuration to minimize high-speed switching noise**
- **I_{CC} category: SSI**

DESCRIPTION

The 74AC/ACT11008 high-performance CMOS devices combine very high speed and high output drive comparable to the most advanced TTL families.

The 74AC/ACT11008 provides four separate 2-input AND gate functions.

GENERAL INFORMATION

SYMBOL	PARAMETER	CONDITIONS T_A = 25°C; GND = 0V; V_{CC} = 5.0V	TYPICAL		UNIT
			AC	ACT	
t_{PLH}/t_{PHL}	Propagation delay A, B, to Y	C_L = 50pF	4.2	5.5	ns
C_{PD}	Power dissipation capacitance per gate[1]	f = 1MHz; C_L = 50pF	29	29	pF
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	3.5	3.5	pF
I_{LATCH}	Latch-up current	Per Jedec JC40.2 Standard 17	500	500	mA

Note:

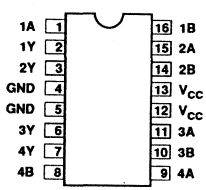
1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_I + \Sigma (C_L \times V_{CC}^2 \times f_O)$ where:
   f_I = input frequency in MHz, C_L = output load capacitance in pF,
   f_O = output frequency in MHz, V_{CC} = supply voltage in V,
   $\Sigma (C_L \times V_{CC}^2 \times f_O)$ = sum of outputs

ORDERING INFORMATION

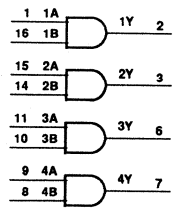
PACKAGES	TEMPERATURE RANGE	ORDER CODE
16-pin plastic DIP (300mil-wide)	-40°C to +85°C	74AC11008N 74ACT11008N
16-pin plastic SO (150mil-wide)	-40°C to +85°C	74AC11008D 74ACT11008D

PIN CONFIGURATION

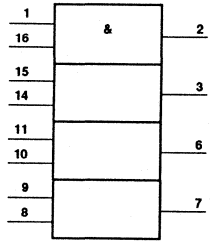
N and D Packages



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
1, 15, 11, 9	1A - 4A	Data inputs
16, 14, 10, 8	1B - 4B	Data inputs
2, 3, 6, 7	1Y - 4Y	Data outputs
4, 5	GND	Ground (0V)
12, 13	V_{CC}	Positive supply voltage

FUNCTION TABLE

INPUTS		OUTPUT
nA	nB	nY
L	L	L
L	H	L
H	L	L
H	H	H

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	74AC11008			74ACT11008			UNIT
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	DC supply voltage	3.0[1]	5.0	5.5	4.5	5.0	5.5	V
V_I	Input voltage	0		V_{CC}	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	0		V_{CC}	V
$\Delta t/\Delta v$	Input transition rise or fall rate	0		10	0		10	ns/V
T_A	Operating free-air temperature	-40		+85	-40		+85	°C

NOTE:

1. No electrical or switching characteristics are specified at $V_{CC} < 3V$. Operation between 2V and 3V is not recommended, but within that range, a device output will maintain a previously established logic state.

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	TEST CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 to+7.0	V
I_{IK} or V_I	DC input diode current[2]	$V_I < 0$	-20	mA
		$V_I > V_{CC}$	20	
	DC input voltage		-0.5 to V_{CC} +0.5	V
I_{OK} or V_O	DC output diode current[2]	$V_O < 0$	-50	mA
		$V_O > V_{CC}$	50	
	DC output voltage		-0.5 to V_{CC} +0.5	V
I_O	DC output source or sink current per output pin	V_O = 0 to V_{CC}	±50	mA
I_{CC} or I_{GND}	DC V_{CC} current		±100	mA
	DC ground current		±100	
T_{STG}	Storage temperature		-65 to 150	°C
P_{TOT}	Power dissipation per package Plastic DIP	Above 70°C:derate linearly by 8mW/K	500	mW
	Power dissipation per package Plastic surface mount (SO)	Above 70°C:derate linearly by 6mW/K	400	mW

NOTES:

1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		V_{CC}	74AC11008				74ACT11008				UNIT
					T_A = +25°C		T_A = -40°C to +85°C		T_A = +25°C		T_A = -40°C to +85°C		
				V	Min	Max	Min	Max	Min	Max	Min	Max	
V_{IH}	High-level input voltage			3.0	2.10		2.10						V
				4.5	3.15		3.15		2.0		2.0		
				5.5	3.85		3.85		2.0		2.0		
V_{IL}	Low-level input voltage			3.0		0.90		0.90					V
				4.5		1.35		1.35		0.8		0.8	
				5.5		1.65		1.65		0.8		0.8	
V_{OH}	High-level output voltage	V_I = V_{IL} or V_{IH}	I_{OH} = -50μA	3.0	2.9		2.9						V
				4.5	4.4		4.4		4.4		4.4		
				5.5	5.4		5.4		5.4		5.4		
			I_{OH} = -4mA	3.0	2.58		2.48						
			I_{OH} = -24mA	4.5	3.94		3.8		3.94		3.8		
				5.5	4.94		4.8		4.94		4.8		
			I_{OH} = -75mA[1]	5.5			3.85				3.85		
V_{OL}	Low-level output voltage	V_I = V_{IL} or V_{IH}	I_{OL} = 50μA	3.0		0.1		0.1					V
				4.5		0.1		0.1		0.1		0.1	
				5.5		0.1		0.1		0.1		0.1	
			I_{OL} = 12mA	3.0		0.36		0.44					
			I_{OL} = 24mA	4.5		0.36		0.44		0.36		0.44	
				5.5		0.36		0.44		0.36		0.44	
			I_{OL} = 75mA[1]	5.5				1.65				1.65	
I_I	Input leakage current	V_I = V_{CC} or GND		5.5		±0.1		±1.0		±0.1		±1.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC} or GND, I_O = 0		5.5		4.0		40		4.0		40	μA
ΔI_{CC}	Supply current, TTL inputs High[2]	One input at 3.4V, other inputs at V_{CC} or GND		5.5						0.9		1.0	mA

NOTES:
1. Not more than one output should be tested at a time, and the duration of the test should not exceed 10ms.
2. This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0V or V_{CC}.

AC ELECTRICAL CHARACTERISTICS AT 3.3V ±0.3V

SYMBOL	PARAMETER	WAVEFORM	74AC11008					UNIT
			T_A = +25°C			T_A = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay nA, nB to nY	1	1.5 1.5	6.3 5.6	9.0 7.8	1.5 1.5	10.2 8.6	ns

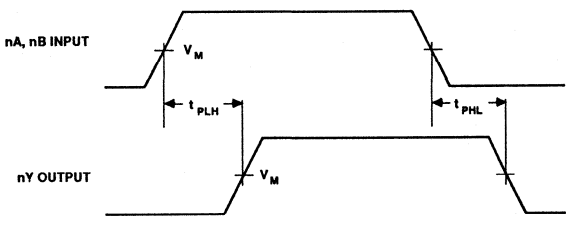
AC ELECTRICAL CHARACTERISTICS AT 5.0V ±0.5V

SYMBOL	PARAMETER	WAVEFORM	74AC11008					UNIT
			T_A = +25°C			T_A = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay nA, nB to nY	1	1.5 1.5	4.3 4.0	6.2 5.9	1.5 1.5	6.9 6.5	ns

AC ELECTRICAL CHARACTERISTICS AT 5.0V ±0.5V

SYMBOL	PARAMETER	WAVEFORM	74ACT11008					UNIT
			T_A = +25°C			T_A = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay nA, nB to nY	1	1.5 1.5	5.8 5.2	8.0 7.7	1.5 1.5	9.0 8.2	ns

AC WAVEFORMS

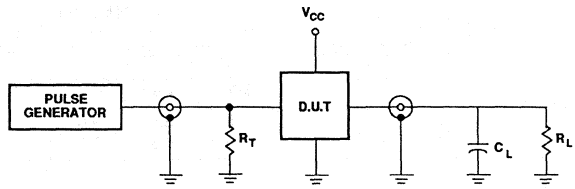


Waveform 1. Waveforms Showing the Inputs (nA, nB) to Output (nY) Propagation Delays

WAVEFORM CONDITIONS

	INPUTS	OUTPUTS
AC	V_{IN} = GND to V_{CC}, V_M = 50% V_{CC}	V_{OUT} = V_{OL} to V_{OH}
ACT	V_{IN} = GND to 3.0V, V_M = 1.5V	V_M = 50% V_{CC}

TEST CIRCUIT



Test Circuit

DEFINITIONS

C_L = Load capacitance, 50pF; includes jig and probe capacitance

R_L = Load resistor, 500Ω

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators

Input pulses: PRR ≤ 10MHz

$t_r = t_f = 3ns$

74AC/ACT11010

Triple 3-Input NAND Gate

Product Specification

FEATURES

- **Output capability: ±24 mA**
- **CMOS (AC) and TTL (ACT) voltage level inputs**
- **50Ω incident wave switching**
- **Center-pin V_{CC} and ground configuration to minimize high-speed switching noise**
- **I_{CC} category: SSI**

DESCRIPTION

The 74AC/ACT11010 high-performance CMOS devices combine very high speed and high output drive comparable to the most advanced TTL families.

The 74AC/ACT11010 provides three separate 3-input NAND gate functions.

GENERAL INFORMATION

SYMBOL	PARAMETER	CONDITIONS T_A = 25°C; GND = 0V; V_{CC} = 5.0V	TYPICAL		UNIT
			AC	ACT	
t_{PLH}/t_{PHL}	Propagation delay A, B, C to $\overline{Y}$	C_L = 50pF	4.5	5.8	ns
C_{PD}	Power dissipation capacitance per gate[1]	f = 1MHz; C_L = 50pF	23	27	pF
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	3.5	3.5	pF
I_{LATCH}	Latch-up current	Per Jedec JC40.2 Standard 17	500	500	mA

Note:

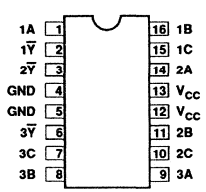
1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_I + \Sigma (C_L \times V_{CC}^2 \times f_O)$ where:
   f_I = input frequency in MHz, C_L = output load capacitance in pF,
   f_O = output frequency in MHz, V_{CC} = supply voltage in V,
   $\Sigma (C_L \times V_{CC}^2 \times f_O)$ = sum of outputs

ORDERING INFORMATION

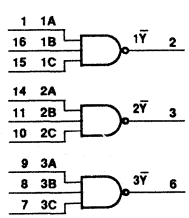
PACKAGES	TEMPERATURE RANGE	ORDER CODE
16-pin plastic DIP (300mil-wide)	-40°C to +85°C	74AC11010N 74ACT11010N
16-pin plastic SO (150mil-wide)	-40°C to +85°C	74AC11010D 74ACT11010D

PIN CONFIGURATION

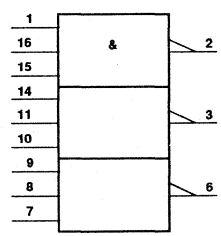
N and D Packages



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
1, 14, 9	1A - 3A	Data inputs
16, 11, 8	1B - 3B	Data inputs
15, 10, 7	1C - 3C	Data inputs
2, 3, 6	$1\overline{Y}$ - $3\overline{Y}$	Data outputs
4, 5	GND	Ground (0V)
12, 13	V_{CC}	Positive supply voltage

INPUTS			OUTPUT
nA	nB	nC	$n\overline{Y}$
L	L	L	H
L	L	H	H
L	H	L	H
L	H	H	H
H	L	L	H
H	L	H	H
H	H	L	H
H	H	H	L

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	74AC11010			74ACT11010			UNIT
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	DC supply voltage	3.0[1]	5.0	5.5	4.5	5.0	5.5	V
V_I	Input voltage	0		V_{CC}	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	0		V_{CC}	V
$\Delta t/\Delta v$	Input transition rise or fall rate	0		10	0		10	ns/V
T_A	Operating free-air temperature	-40		+85	-40		+85	°C

NOTE:
1. No electrical or switching characteristics are specified at $V_{CC} < 3V$. Operation between 2V and 3V is not recommended, but within that range, a device output will maintain a previously established logic state.

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	TEST CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 to+7.0	V
I_{IK} or V_I	DC input diode current[2]	$V_I < 0$	-20	mA
		$V_I > V_{CC}$	20	
	DC input voltage		-0.5 to V_{CC} +0.5	V
I_{OK} or V_O	DC output diode current[2]	$V_O < 0$	-50	mA
		$V_O > V_{CC}$	50	
	DC output voltage		-0.5 to V_{CC} +0.5	V
I_O	DC output source or sink current per output pin	V_O = 0 to V_{CC}	±50	mA
I_{CC} or I_{GND}	DC V_{CC} current		±100	mA
	DC ground current		±100	
T_{STG}	Storage temperature		-65 to 150	°C
P_{TOT}	Power dissipation per package Plastic DIP	Above 70°C:derate linearly by 8mW/K	500	mW
	Power dissipation per package Plastic surface mount (SO)	Above 70°C:derate linearly by 6mW/K	400	mW

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		V_{CC}	74AC11010				74ACT11010				UNIT
					T_A = +25°C		T_A = -40°C to +85°C		T_A = +25°C		T_A = -40°C to +85°C		
				V	Min	Max	Min	Max	Min	Max	Min	Max	
V_{IH}	High-level input voltage			3.0	2.10		2.10						V
				4.5	3.15		3.15		2.0		2.0		
				5.5	3.85		3.85		2.0		2.0		
V_{IL}	Low-level input voltage			3.0		0.90		0.90					V
				4.5		1.35		1.35		0.8		0.8	
				5.5		1.65		1.65		0.8		0.8	
V_{OH}	High-level output voltage	V_I = V_{IL} or V_{IH}	I_{OH} = -50μA	3.0	2.9		2.9						V
				4.5	4.4		4.4		4.4		4.4		
				5.5	5.4		5.4		5.4		5.4		
			I_{OH} = -4mA	3.0	2.58		2.48						
			I_{OH} = -24mA	4.5	3.94		3.8		3.94		3.8		
				5.5	4.94		4.8		4.94		4.8		
			I_{OH} = -75mA[1]	5.5			3.85				3.85		
V_{OL}	Low-level output voltage	V_I = V_{IL} or V_{IH}	I_{OL} = 50μA	3.0		0.1		0.1					V
				4.5		0.1		0.1		0.1		0.1	
				5.5		0.1		0.1		0.1		0.1	
			I_{OL} = 12mA	3.0		0.36		0.44					
			I_{OL} = 24mA	4.5		0.36		0.44		0.36		0.44	
				5.5		0.36		0.44		0.36		0.44	
			I_{OL} = 75mA[1]	5.5				1.65				1.65	
I_I	Input leakage current	V_I = V_{CC} or GND		5.5		±0.1		±1.0		±0.1		±1.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC} or GND, I_O = 0		5.5		4.0		40		4.0		40	μA
ΔI_{CC}	Supply current, TTL inputs High[2]	One input at 3.4V, other inputs at V_{CC} or GND		5.5						0.9		1.0	mA

NOTES:
1. Not more than one output should be tested at a time, and the duration of the test should not exceed 10ms.
2. This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0V or V_{CC}.

AC ELECTRICAL CHARACTERISTICS AT 3.3V ±0.3V

SYMBOL	PARAMETER	WAVEFORM	74AC11010					UNIT
			T_A = +25°C			T_A = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay nA, nB, nC to n$\overline{Y}$	1	1.5 1.5	5.9 5.8	8.5 9.0	1.5 1.5	9.3 9.9	ns

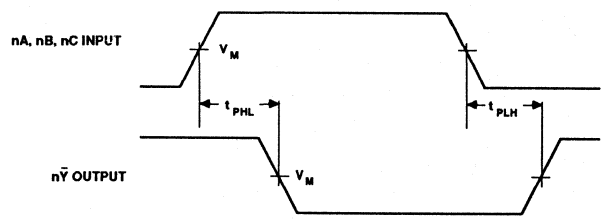
AC ELECTRICAL CHARACTERISTICS AT 5.0V ±0.5V

SYMBOL	PARAMETER	WAVEFORM	74AC11010					UNIT
			T_A = +25°C			T_A = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay nA, nB, nC to n$\overline{Y}$	1	1.5 1.5	4.4 4.6	6.2 6.4	1.5 1.5	6.7 7.0	ns

AC ELECTRICAL CHARACTERISTICS AT 5.0V ±0.5V

SYMBOL	PARAMETER	WAVEFORM	74ACT11010					UNIT
			T_A = +25°C			T_A = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay nA, nB, nC to n$\overline{Y}$	1	1.5 1.5	5.8 5.7	8.2 7.4	1.5 1.5	8.9 8.2	ns

AC WAVEFORMS

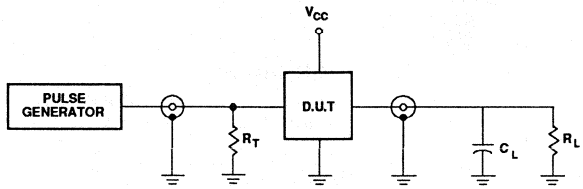


Waveform 1. Waveforms Showing the Input (nA, nB, nC) to Output (n$\overline{Y}$) Propagation Delays

WAVEFORM CONDITIONS

	INPUTS	OUTPUTS
AC	V_{IN} = GND to V_{CC}, V_M = 50% V_{CC}	V_{OUT} = V_{OL} to V_{OH}
ACT	V_{IN} = GND to 3.0V, V_M = 1.5V	V_M = 50% V_{CC}

TEST CIRCUIT



Test Circuit

DEFINITIONS

C_L = Load capacitance, 50pF; includes jig and probe capacitance

R_L = Load resistor, 500Ω

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators

Input pulses: PRR ≤ 10MHz

$t_r = t_f$ = 3ns

74AC/ACT11011

Triple 3-Input AND Gate

Product Specification

FEATURES

- **Output capability: ±24 mA**
- **CMOS (AC) and TTL (ACT) voltage level inputs**
- **50Ω incident wave switching**
- **Center-pin V_{CC} and ground configuration to minimize high-speed switching noise**
- **I_{CC} category: SSI**

DESCRIPTION

The 74AC/ACT11011 high-performance CMOS devices combine very high speed and high output drive comparable to the most advanced TTL families.

The 74AC/ACT11011 provides three separate 3-input AND gate functions.

GENERAL INFORMATION

SYMBOL	PARAMETER	CONDITIONS T_A = 25°C; GND = 0V; V_{CC} = 5.0V	TYPICAL		UNIT
			AC	ACT	
t_{PLH}/t_{PHL}	Propagation delay A, B, C to Y	C_L = 50pF	4.3	6.0	ns
C_{PD}	Power dissipation capacitance per gate[1]	f = 1MHz; C_L = 50pF	28	28	pF
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	3.5	3.5	pF
I_{LATCH}	Latch-up current	Per Jedec JC40.2 Standard 17	500	500	mA

Note:

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):

$$P_D = C_{PD} \times V_{CC}^2 \times f_I + \Sigma (C_L \times V_{CC}^2 \times f_O)$$ where:

f_I = input frequency in MHz, C_L = output load capacitance in pF,

f_O = output frequency in MHz, V_{CC} = supply voltage in V,

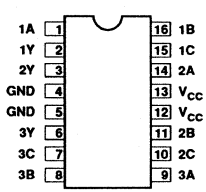
$\Sigma (C_L \times V_{CC}^2 \times f_O)$ = sum of outputs

ORDERING INFORMATION

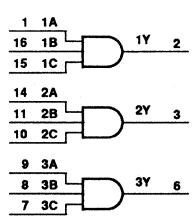
PACKAGES	TEMPERATURE RANGE	ORDER CODE
16-pin plastic DIP (300mil-wide)	-40°C to +85°C	74AC11011N 74ACT11011N
16-pin plastic SO (150mil-wide)	-40°C to +85°C	74AC11011D 74ACT11011D

PIN CONFIGURATION

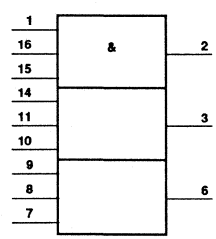
N and D Packages



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
1, 14, 9	1A - 3A	Data inputs
16, 11, 8	1B - 3B	Data inputs
15, 10, 7	1C - 3C	Data inputs
2, 3, 6	1Y - 3Y	Data outputs
4, 5	GND	Ground (0V)
12, 13	V_{CC}	Positive supply voltage

FUNCTION TABLE

INPUTS			OUTPUT
nA	nB	nC	nY
L	L	L	L
L	L	H	L
L	H	L	L
L	H	H	L
H	L	L	L
H	L	H	L
H	H	L	L
H	H	H	H

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	74AC11011			74ACT11011			UNIT
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	DC supply voltage	3.0[1]	5.0	5.5	4.5	5.0	5.5	V
V_I	Input voltage	0		V_{CC}	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	0		V_{CC}	V
$\Delta t/\Delta v$	Input transition rise or fall rate	0		10	0		10	ns/V
T_A	Operating free-air temperature	-40		+85	-40		+85	°C

NOTE:
1. No electrical or switching characteristics are specified at V_{CC} < 3V. Operation between 2V and 3V is not recommended, but within that range, a device output will maintain a previously established logic state.

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	TEST CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 to+7.0	V
I_{IK} or V_I	DC input diode current[2]	$V_I < 0$	-20	mA
		$V_I > V_{CC}$	20	
	DC input voltage		-0.5 to V_{CC} +0.5	V
I_{OK} or V_O	DC output diode current[2]	$V_O < 0$	-50	mA
		$V_O > V_{CC}$	50	
	DC output voltage		-0.5 to V_{CC} +0.5	V
I_O	DC output source or sink current per output pin	V_O = 0 to V_{CC}	±50	mA
I_{CC} or I_{GND}	DC V_{CC} current		±100	mA
	DC ground current		±100	
T_{STG}	Storage temperature		-65 to 150	°C
P_{TOT}	Power dissipation per package Plastic DIP	Above 70°C:derate linearly by 8mW/K	500	mW
	Power dissipation per package Plastic surface mount (SO)	Above 70°C:derate linearly by 6mW/K	400	mW

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		V_{CC}	74AC11011				74ACT11011				UNIT
					T_A = +25°C		T_A = -40°C to +85°C		T_A = +25°C		T_A = -40°C to +85°C		
				V	Min	Max	Min	Max	Min	Max	Min	Max	
V_{IH}	High-level input voltage			3.0	2.10		2.10						V
				4.5	3.15		3.15		2.0		2.0		
				5.5	3.85		3.85		2.0		2.0		
V_{IL}	Low-level input voltage			3.0		0.90		0.90					V
				4.5		1.35		1.35		0.8		0.8	
				5.5		1.65		1.65		0.8		0.8	
V_{OH}	High-level output voltage	V_I = V_{IL} or V_{IH}	I_{OH} = -50μA	3.0	2.9		2.9						V
				4.5	4.4		4.4		4.4		4.4		
				5.5	5.4		5.4		5.4		5.4		
			I_{OH} = -4mA	3.0	2.58		2.48						
			I_{OH} = -24mA	4.5	3.94		3.8		3.94		3.8		
				5.5	4.94		4.8		4.94		4.8		
			I_{OH} = -75mA[1]	5.5			3.85				3.85		
V_{OL}	Low-level output voltage	V_I = V_{IL} or V_{IH}	I_{OL} = 50μA	3.0		0.1		0.1					V
				4.5		0.1		0.1		0.1		0.1	
				5.5		0.1		0.1		0.1		0.1	
			I_{OL} = 12mA	3.0		0.36		0.44					
			I_{OL} = 24mA	4.5		0.36		0.44		0.36		0.44	
				5.5		0.36		0.44		0.36		0.44	
			I_{OL} = 75mA[1]	5.5				1.65				1.65	
I_I	Input leakage current	V_I = V_{CC} or GND		5.5		±0.1		±1.0		±0.1		±1.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC} or GND, I_O = 0		5.5		4.0		40		4.0		40	μA
ΔI_{CC}	Supply current, TTL inputs High[2]	One input at 3.4V, other inputs at V_{CC} or GND		5.5						0.9		1.0	mA

NOTES:
1. Not more than one output should be tested at a time, and the duration of the test should not exceed 10ms.
2. This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0V or V_{CC}.

AC ELECTRICAL CHARACTERISTICS AT 3.3V ±0.3V

SYMBOL	PARAMETER	WAVEFORM	74AC11011					UNIT
			T_A = +25°C			T_A = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay nA, nB, nC to nY	1	1.5 1.5	6.0 6.0	8.3 8.2	1.5 1.5	9.1 9.0	ns

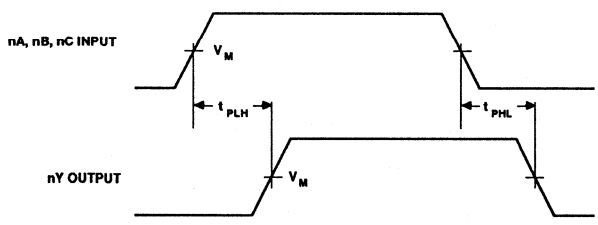
AC ELECTRICAL CHARACTERISTICS AT 5.0V ±0.5V

SYMBOL	PARAMETER	WAVEFORM	74AC11011					UNIT
			T_A = +25°C			T_A = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay nA, nB, nC to nY	1	1.5 1.5	4.0 4.5	5.9 6.4	1.5 1.5	6.5 6.9	ns

AC ELECTRICAL CHARACTERISTICS AT 5.0V ±0.5V

SYMBOL	PARAMETER	WAVEFORM	74ACT11011					UNIT
			T_A = +25°C			T_A = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay nA, nB, nC to nY	1	1.5 1.5	6.5 5.5	8.6 7.9	1.5 1.5	9.6 8.7	ns

AC WAVEFORMS

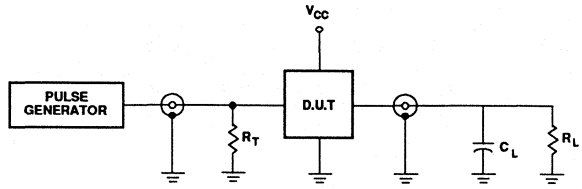


Waveform 1. Waveforms Showing the Input (nA, nB, nC) to Output (nY) Propagation Delays

WAVEFORM CONDITIONS

	INPUTS	OUTPUTS
AC	V_{IN} = GND to V_{CC}, V_M = 50% V_{CC}	V_{OUT} = V_{OL} to V_{OH}
ACT	V_{IN} = GND to 3.0V, V_M = 1.5V	V_M = 50% V_{CC}

TEST CIRCUIT



Test Circuit

DEFINITIONS

C_L = Load capacitance, 50pF; includes jig and probe capacitance

R_L = Load resistor, 500Ω

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators

Input pulses: PRR ≤ 10MHz

$t_r = t_f$ = 3ns

74AC/ACT11013

Dual 4-Input NAND Schmitt-Trigger

AC11013: Preliminary Specification
ACT11013: Objective Specification

FEATURES

- **Output capability: ±24 mA**
- **CMOS (AC) and TTL (ACT) voltage level inputs**
- **50Ω incident wave switching**
- **Center-pin V_{CC} and ground configuration to minimize high-speed switching noise**
- **I_{CC} category: SSI**

DESCRIPTION

The 74AC/ACT11013 high-performance CMOS devices combine very high speed and high output drive comparable to the most advanced TTL families.

The 74AC/ACT11013 provides two separate 4-input NAND gate functions which are capable of transforming slowly changing input signals into sharply defined, jitter-free output signals. In addition, they have greater noise margin than conventional NAND gates.

GENERAL INFORMATION

SYMBOL	PARAMETER	CONDITIONS T_A = 25°C; GND = 0V; V_{CC} = 5.0V	TYPICAL		UNIT
			AC	ACT	
t_{PLH}/t_{PHL}	Propagation delay A, B, C, D to $\overline{Y}$	C_L = 50pF	5.2	8.0	ns
C_{PD}	Power dissipation capacitance per gate[1]	f = 1MHz; C_L = 50pF	29	32	pF
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	3.5	3.5	pF
I_{LATCH}	Latch-up current	Per Jedec JC40.2 Standard 17	500	500	mA

Note:

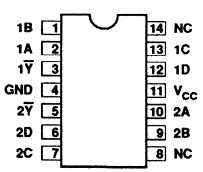
1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_I + \Sigma (C_L \times V_{CC}^2 \times f_O)$ where:
   f_I = input frequency in MHz, C_L = output load capacitance in pF,
   f_O = output frequency in MHz, V_{CC} = supply voltage in V,
   $\Sigma (C_L \times V_{CC}^2 \times f_O)$ = sum of outputs

ORDERING INFORMATION

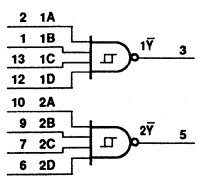
PACKAGES	TEMPERATURE RANGE	ORDER CODE
14-pin plastic DIP (300mil-wide)	-40°C to +85°C	74AC11013N 74ACT11013N
14-pin plastic SO (150mil-wide)	-40°C to +85°C	74AC11013D 74ACT11013D

PIN CONFIGURATION

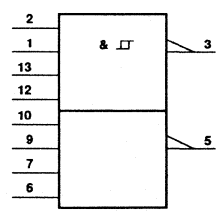
N and D Packages



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
2, 10	1A - 2A	Data inputs
1, 9	1B - 2B	Data inputs
13, 7	1C - 2C	Data inputs
12, 6	1D - 2D	Data inputs
3, 5	$1\overline{Y}$ - $2\overline{Y}$	Data outputs
4	GND	Ground (0V)
11	V_{CC}	Positive supply voltage

FUNCTION TABLE

INPUTS				OUTPUT
nA	nB	nC	nD	$n\overline{Y}$
H	H	H	H	L
L	X	X	X	H
X	L	X	X	H
X	X	L	X	H
X	X	X	L	H

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	74AC11013			74ACT11013			UNIT
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	DC supply voltage	3.0[1]	5.0	5.5	4.5	5.0	5.5	V
V_I	Input voltage	0		V_{CC}	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	0		V_{CC}	V
$\Delta t/\Delta v$	Input transition rise or fall rate	0		100	0		100	ns/V
T_A	Operating free-air temperature	-40		+85	-40		+85	°C

NOTE:

1. No electrical or switching characteristics are specified at $V_{CC} < 3V$. Operation between 2V and 3V is not recommended, but within that range, a device output will maintain a previously established logic state.

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	TEST CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 to+7.0	V
I_{IK} or V_I	DC input diode current[2]	$V_I < 0$	-20	mA
		$V_I > V_{CC}$	20	
	DC input voltage		-0.5 to V_{CC} +0.5	V
I_{OK} or V_O	DC output diode current[2]	$V_O < 0$	-50	mA
		$V_O > V_{CC}$	50	
	DC output voltage		-0.5 to V_{CC} +0.5	V
I_O	DC output source or sink current per output pin	V_O = 0 to V_{CC}	±50	mA
I_{CC} or I_{GND}	DC V_{CC} current		±100	mA
	DC ground current		±100	
T_{STG}	Storage temperature		-65 to 150	°C
P_{TOT}	Power dissipation per package Plastic DIP	Above 70°C:derate linearly by 8mW/K	500	mW
	Power dissipation per package Plastic surface mount (SO)	Above 70°C:derate linearly by 6mW/K	400	mW

NOTES:

1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		V_{CC}	74AC11013				74ACT11013				UNIT
					T_A = +25°C		T_A = -40°C to +85°C		T_A = +25°C		T_A = -40°C to +85°C		
				V	Min	Max	Min	Max	Min	Max	Min	Max	
V_{T+}	Positive-going threshold			3.0		2.2		2.2					V
				4.5		3.2		3.2		2.0		2.0	
				5.5		3.9		3.9		2.0		2.0	
V_{T-}	Negative-going threshold			3.0	0.5		0.5						V
				4.5	0.9		0.9			0.8		0.8	
				5.5	1.1		1.1			0.8		0.8	
ΔV_T	Hysteresis (V_{T+} - V_{T-})			3.0	0.3	1.2	0.3	1.2					V
				4.5	0.4	1.4	0.4	1.4	0.4	1.2	0.4	1.2	
				5.5	0.5	1.6	0.5	1.6	0.4	1.2	0.4	1.2	
V_{IH}	High-level input voltage			3.0	2.10		2.10						V
				4.5	3.15		3.15		2.0		2.0		
				5.5	3.85		3.85		2.0		2.0		
V_{IL}	Low-level input voltage			3.0		0.90		0.90					V
				4.5		1.35		1.35		0.8		0.8	
				5.5		1.65		1.65		0.8		0.8	
V_{OH}	High-level output voltage	V_I = V_{IL} or V_{IH}	I_{OH} = -50μA	3.0	2.9		2.9						V
				4.5	4.4		4.4		4.4		4.4		
				5.5	5.4		5.4		5.4		5.4		
			I_{OH} = -4mA	3.0	2.58		2.48						
			I_{OH} = -24mA	4.5	3.94		3.8		3.94		3.8		
				5.5	4.94		4.8		4.94		4.8		
			I_{OH} = -75mA[1]	5.5			3.85				3.85		
V_{OL}	Low-level output voltage	V_I = V_{IL} or V_{IH}	I_{OL} = 50μA	3.0		0.1		0.1					V
				4.5		0.1		0.1		0.1		0.1	
				5.5		0.1		0.1		0.1		0.1	
			I_{OL} = 12mA	3.0		0.36		0.44					
			I_{OL} = 24mA	4.5		0.36		0.44		0.36		0.44	
				5.5		0.36		0.44		0.36		0.44	
			I_{OL} = 75mA[1]	5.5				1.65				1.65	
I_I	Input leakage current	V_I = V_{CC} or GND		5.5		±0.1		±1.0		±0.1		±1.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC} or GND, I_O = 0		5.5		4.0		40		4.0		40	μA
ΔI_{CC}	Supply current, TTL inputs High[2]	One input at 3.4V, other inputs at V_{CC} or GND		5.5						0.9		1.0	mA

NOTES:

1. Not more than one output should be tested at a time, and the duration of the test should not exceed 10ms.
2. This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0V or V_{CC}.

AC ELECTRICAL CHARACTERISTICS AT 3.3V ±0.3V

SYMBOL	PARAMETER	WAVEFORM	74AC11013					UNIT
			T_A = +25°C			T_A = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay nA, nB, nC, nD to n$\overline{Y}$	1	1.5 1.5	7.3 7.2	8.7 8.7	1.5 1.5	10.0 10.2	ns

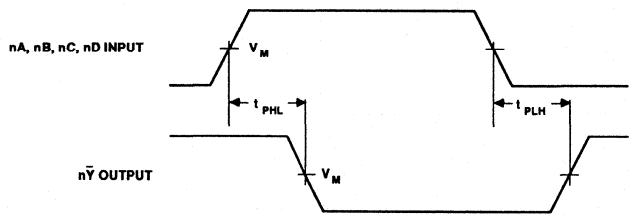
AC ELECTRICAL CHARACTERISTICS AT 5.0V ±0.5V

SYMBOL	PARAMETER	WAVEFORM	74AC11013					UNIT
			T_A = +25°C			T_A = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay nA, nB, nC, nD to n$\overline{Y}$	1	1.5 1.5	5.1 5.2	6.4 7.0	1.5 1.5	7.3 8.1	ns

AC ELECTRICAL CHARACTERISTICS AT 5.0V ±0.5V

SYMBOL	PARAMETER	WAVEFORM	74ACT11013					UNIT
			T_A = +25°C			T_A = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay nA, nB, nC, nD to n$\overline{Y}$	1	1.5 1.5			1.5 1.5		ns

AC WAVEFORMS

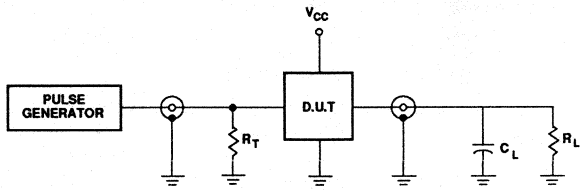


Waveform 1. Waveforms Showing the Input (nA, nB, nC, nD) to Output (n$\overline{Y}$) Propagation Delays

WAVEFORM CONDITIONS

	INPUTS	OUTPUTS
AC	V_{IN} = GND to V_{CC}, V_M = 50% V_{CC}	V_{OUT} = V_{OL} to V_{OH}
ACT	V_{IN} = GND to 3.0V, V_M = 1.5V	V_M = 50% V_{CC}

TEST CIRCUIT



Test Circuit

DEFINITIONS

C_L = Load capacitance, 50pF; includes jig and probe capacitance

R_L = Load resistor, 500Ω

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators

Input pulses: PRR ≤ 10MHz

$t_r = t_f$ = 3ns

74AC/ACT11014

Hex Inverter Schmitt-Trigger

AC11014: Preliminary Specification
ACT11014: Objective Specification

FEATURES

- **Output capability: ±24 mA**
- **CMOS (AC) and TTL (ACT) voltage level inputs**
- **50Ω incident wave switching**
- **Center-pin V_{CC} and ground configuration to minimize high-speed switching noise**
- **I_{CC} category: SSI**

DESCRIPTION

The 74AC/ACT11014 high-performance CMOS devices combine very high speed and high output drive comparable to the most advanced TTL families.

The 74AC/ACT11014 provides six separate inverters which are capable of transforming slowly changing input signals into sharply defined, jitter-free output signals. In addition, they have greater noise margin than conventional inverters.

GENERAL INFORMATION

SYMBOL	PARAMETER	CONDITIONS T_A = 25°C; GND = 0V; V_{CC} = 5.0V	TYPICAL		UNIT
			AC	ACT	
t_{PLH}/t_{PHL}	Propagation delay A, B, to $\overline{Y}$	C_L = 50pF	6.9	8.5	ns
C_{PD}	Power dissipation capacitance per gate[1]	f = 1MHz; C_L = 50pF	27	36	pF
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	4.0	4.0	pF
I_{LATCH}	Latch-up current	Per Jedec JC40.2 Standard 17	500	500	mA

Note:

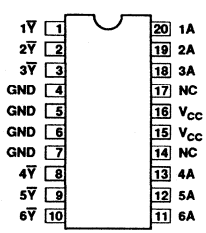
1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_I + \Sigma (C_L \times V_{CC}^2 \times f_O)$ where:
   f_I = input frequency in MHz, C_L = output load capacitance in pF,
   f_O = output frequency in MHz, V_{CC} = supply voltage in V,
   $\Sigma (C_L \times V_{CC}^2 \times f_O)$ = sum of outputs

ORDERING INFORMATION

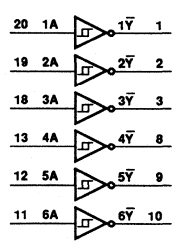
PACKAGES	TEMPERATURE RANGE	ORDER CODE
20-pin plastic DIP (300mil-wide)	-40°C to +85°C	74AC11014N 74ACT11014N
20-pin plastic SO (300mil-wide)	-40°C to +85°C	74AC11014D 74ACT11014D

PIN CONFIGURATION

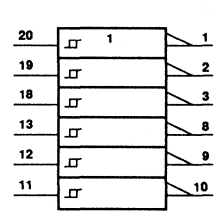
N and D Packages



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
20, 19, 18, 13, 12, 11	1A - 6A	Data inputs
1, 2, 3, 8, 9, 10	$1\overline{Y}$ - $6\overline{Y}$	Data outputs
4, 5, 6, 7	GND	Ground (0V)
15, 16	V_{CC}	Positive supply voltage

INPUT	OUTPUT
nA	$n\overline{Y}$
L	H
H	L

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	74AC11014			74ACT11014			UNIT
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	DC supply voltage	3.0[1]	5.0	5.5	4.5	5.0	5.5	V
V_I	Input voltage	0		V_{CC}	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	0		V_{CC}	V
$\Delta t/\Delta v$	Input transition rise or fall rate	0		100	0		100	ns/V
T_A	Operating free-air temperature	-40		+85	-40		+85	°C

NOTE:
1. No electrical or switching characteristics are specified at V_{CC} < 3V. Operation between 2V and 3V is not recommended, but within that range, a device output will maintain a previously established logic state.

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	TEST CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 to+7.0	V
I_{IK} or V_I	DC input diode current[2]	$V_I < 0$	-20	mA
		$V_I > V_{CC}$	20	
	DC input voltage		-0.5 to V_{CC} +0.5	V
I_{OK} or V_O	DC output diode current[2]	$V_O < 0$	-50	mA
		$V_O > V_{CC}$	50	
	DC output voltage		-0.5 to V_{CC} +0.5	V
I_O	DC output source or sink current per output pin	V_O = 0 to V_{CC}	±50	mA
I_{CC} or I_{GND}	DC V_{CC} current		±150	mA
	DC ground current		±150	
T_{STG}	Storage temperature		-65 to 150	°C
P_{TOT}	Power dissipation per package Plastic DIP	Above 70°C:derate linearly by 8mW/K	500	mW
	Power dissipation per package Plastic surface mount (SO)	Above 70°C:derate linearly by 6mW/K	400	mW

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		V_{CC}	74AC11014				74ACT11014				UNIT
					T_A = +25°C		T_A = -40°C to +85°C		T_A = +25°C		T_A = -40°C to +85°C		
				V	Min	Max	Min	Max	Min	Max	Min	Max	
V_{T+}	Positive-going threshold			3.0		2.2		2.2					V
				4.5		3.2		3.2		2.0		2.0	
				5.5		3.9		3.9		2.0		2.0	
V_{T-}	Negative-going threshold			3.0	0.5		0.5						V
				4.5	0.9		0.9			0.8		0.8	
				5.5	1.1		1.1			0.8		0.8	
ΔV_T	Hysteresis ($V_{T+} - V_{T-}$)			3.0	0.3	1.2	0.3	1.2					V
				4.5	0.4	1.4	0.4	1.4	0.4	1.2	0.4	1.2	
				5.5	0.5	1.6	0.5	1.6	0.4	1.2	0.4	1.2	
V_{IH}	High-level input voltage			3.0	2.10		2.10						V
				4.5	3.15		3.15		2.0		2.0		
				5.5	3.85		3.85		2.0		2.0		
V_{IL}	Low-level input voltage			3.0		0.90		0.90					V
				4.5		1.35		1.35		0.8		0.8	
				5.5		1.65		1.65		0.8		0.8	
V_{OH}	High-level output voltage	V_I = V_{IL} or V_{IH}	I_{OH} = -50μA	3.0	2.9		2.9						V
				4.5	4.4		4.4		4.4		4.4		
				5.5	5.4		5.4		5.4		5.4		
			I_{OH} = -4mA	3.0	2.58		2.48						
			I_{OH} = -24mA	4.5	3.94		3.8		3.94		3.8		
				5.5	4.94		4.8		4.94		4.8		
			I_{OH} = -75mA[1]	5.5			3.85				3.85		
V_{OL}	Low-level output voltage	V_I = V_{IL} or V_{IH}	I_{OL} = 50μA	3.0		0.1		0.1					V
				4.5		0.1		0.1		0.1		0.1	
				5.5		0.1		0.1		0.1		0.1	
			I_{OL} = 12mA	3.0		0.36		0.44					
			I_{OL} = 24mA	4.5		0.36		0.44		0.36		0.44	
				5.5		0.36		0.44		0.36		0.44	
			I_{OL} = 75mA[1]	5.5				1.65				1.65	
I_I	Input leakage current	V_I = V_{CC} or GND		5.5		±0.1		±1.0		±0.1		±1.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC} or GND, I_O = 0		5.5		4.0		40		4.0		40	μA
ΔI_{CC}	Supply current, TTL inputs High[2]	One input at 3.4V, other inputs at V_{CC} or GND		5.5						0.9		1.0	mA

NOTES:
1. Not more than one output should be tested at a time, and the duration of the test should not exceed 10ms.
2. This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0V or V_{CC}.

AC ELECTRICAL CHARACTERISTICS AT 3.3V ±0.3V

SYMBOL	PARAMETER	WAVEFORM	74AC11014					UNIT
			T_A = +25°C			T_A = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay nA, nB to $n\overline{Y}$	1	1.5 1.5	6.6 6.5	9.3 8.4	1.5 1.5	10.1 9.2	ns

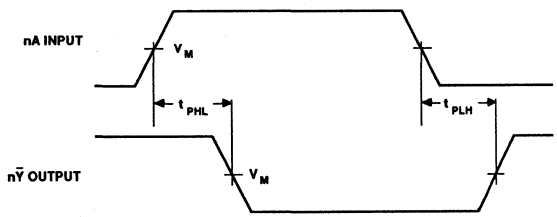
AC ELECTRICAL CHARACTERISTICS AT 5.0V ±0.5V

SYMBOL	PARAMETER	WAVEFORM	74AC11014					UNIT
			T_A = +25°C			T_A = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay nA, nB to $n\overline{Y}$	1	1.5 1.5	4.6 4.9	6.9 6.8	1.5 1.5	7.4 7.3	ns

AC ELECTRICAL CHARACTERISTICS AT 5.0V ±0.5V

SYMBOL	PARAMETER	WAVEFORM	74ACT11014					UNIT
			T_A = +25°C			T_A = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay nA, nB to $n\overline{Y}$	1	1.5 1.5			1.5 1.5		ns

AC WAVEFORMS

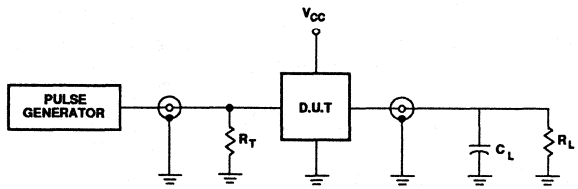


Waveform 1. Waveforms Showing the Input (nA) to Output ($n\overline{Y}$) Propagation Delays

WAVEFORM CONDITIONS

	INPUTS	OUTPUTS
AC	V_{IN} = GND to V_{CC}, V_M = 50% V_{CC}	V_{OUT} = V_{OL} to V_{OH}
ACT	V_{IN} = GND to 3.0V, V_M = 1.5V	V_M = 50% V_{CC}

TEST CIRCUIT



Test Circuit

DEFINITIONS

C_L = Load capacitance, 50pF; includes jig and probe capacitance

R_L = Load resistor, 500Ω

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators

Input pulses: PRR ≤ 10MHz

$t_r = t_f = 3ns$

74AC/ACT11020

Dual 4-Input NAND Gate

Product Specification

FEATURES

- **Output capability: ±24 mA**
- **CMOS (AC) and TTL (ACT) voltage level inputs**
- **50Ω incident wave switching**
- **Center-pin V_{CC} and ground configuration to minimize high-speed switching noise**
- **I_{CC} category: SSI**

DESCRIPTION

The 74AC/ACT11020 high-performance CMOS devices combine very high speed and high output drive comparable to the most advanced TTL families.

The 74AC/ACT11020 provides two separate 4-input NAND gate functions.

GENERAL INFORMATION

SYMBOL	PARAMETER	CONDITIONS T_A = 25°C; GND = 0V; V_{CC} = 5.0V	TYPICAL		UNIT
			AC	ACT	
t_{PLH}/t_{PHL}	Propagation delay A, B, C, D to $\overline{Y}$	C_L = 50pF	4.4	5.9	ns
C_{PD}	Power dissipation capacitance per gate[1]	f = 1MHz; C_L = 50pF	19	27	pF
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	3.5	3.5	pF
I_{LATCH}	Latch-up current	Per Jedec JC40.2 Standard 17	500	500	mA

Note:

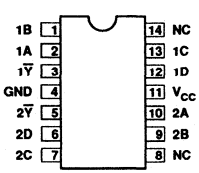
1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_I + \Sigma (C_L \times V_{CC}^2 \times f_O)$ where:
   f_I = input frequency in MHz, C_L = output load capacitance in pF,
   f_O = output frequency in MHz, V_{CC} = supply voltage in V,
   $\Sigma (C_L \times V_{CC}^2 \times f_O)$ = sum of outputs

ORDERING INFORMATION

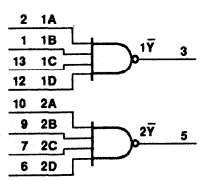
PACKAGES	TEMPERATURE RANGE	ORDER CODE
14-pin plastic DIP (300mil-wide)	-40°C to +85°C	74AC11020N 74ACT11020N
14-pin plastic SO (150mil-wide)	-40°C to +85°C	74AC11020D 74ACT11020D

PIN CONFIGURATION

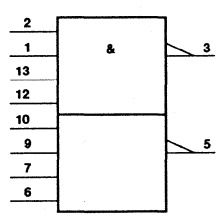
N and D Packages



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
2, 10	1A - 2A	Data inputs
1, 9	1B - 2B	Data inputs
13, 7	1C - 2C	Data inputs
12, 6	1D - 2D	Data inputs
3, 5	$1\overline{Y}$ - $2\overline{Y}$	Data outputs
4	GND	Ground (0V)
11	V_{CC}	Positive supply voltage

FUNCTION TABLE

INPUTS				OUTPUT
nA	nB	nC	nD	$n\overline{Y}$
H	H	H	H	L
L	X	X	X	H
X	L	X	X	H
X	X	L	X	H
X	X	X	L	H

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	74AC11020			74ACT11020			UNIT
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	DC supply voltage	3.0[1]	5.0	5.5	4.5	5.0	5.5	V
V_I	Input voltage	0		V_{CC}	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	0		V_{CC}	V
$\Delta t/\Delta v$	Input transition rise or fall rate	0		10	0		10	ns/V
T_A	Operating free-air temperature	-40		+85	-40		+85	°C

NOTE:

1. No electrical or switching characteristics are specified at $V_{CC} < 3V$. Operation between 2V and 3V is not recommended, but within that range, a device output will maintain a previously established logic state.

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	TEST CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 to+7.0	V
I_{IK} or V_I	DC input diode current[2]	$V_I < 0$	-20	mA
		$V_I > V_{CC}$	20	
	DC input voltage		-0.5 to V_{CC} +0.5	V
I_{OK} or V_O	DC output diode current[2]	$V_O < 0$	-50	mA
		$V_O > V_{CC}$	50	
	DC output voltage		-0.5 to V_{CC} +0.5	V
I_O	DC output source or sink current per output pin	V_O = 0 to V_{CC}	±50	mA
I_{CC} or I_{GND}	DC V_{CC} current		±100	mA
	DC ground current		±100	
T_{STG}	Storage temperature		-65 to 150	°C
P_{TOT}	Power dissipation per package Plastic DIP	Above 70°C:derate linearly by 8mW/K	500	mW
	Power dissipation per package Plastic surface mount (SO)	Above 70°C:derate linearly by 6mW/K	400	mW

NOTES:

1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		V_{CC}	74AC11020				74ACT11020				UNIT
					T_A = +25°C		T_A = -40°C to +85°C		T_A = +25°C		T_A = -40°C to +85°C		
				V	Min	Max	Min	Max	Min	Max	Min	Max	
V_{IH}	High-level input voltage			3.0	2.10		2.10						V
				4.5	3.15		3.15		2.0		2.0		
				5.5	3.85		3.85		2.0		2.0		
V_{IL}	Low-level input voltage			3.0		0.90		0.90					V
				4.5		1.35		1.35		0.8		0.8	
				5.5		1.65		1.65		0.8		0.8	
V_{OH}	High-level output voltage	V_I = V_{IL} or V_{IH}	I_{OH} = -50μA	3.0	2.9		2.9						V
				4.5	4.4		4.4		4.4		4.4		
				5.5	5.4		5.4		5.4		5.4		
			I_{OH} = -4mA	3.0	2.58		2.48						
			I_{OH} = -24mA	4.5	3.94		3.8		3.94		3.8		
				5.5	4.94		4.8		4.94		4.8		
			I_{OH} = -75mA[1]	5.5			3.85				3.85		
V_{OL}	Low-level output voltage	V_I = V_{IL} or V_{IH}	I_{OL} = 50μA	3.0		0.1		0.1					V
				4.5		0.1		0.1		0.1		0.1	
				5.5		0.1		0.1		0.1		0.1	
			I_{OL} = 12mA	3.0		0.36		0.44					
			I_{OL} = 24mA	4.5		0.36		0.44		0.36		0.44	
				5.5		0.36		0.44		0.36		0.44	
			I_{OL} = 75mA[1]	5.5				1.65				1.65	
I_I	Input leakage current	V_I = V_{CC} or GND		5.5		±0.1		±1.0		±0.1		±1.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC} or GND, I_O = 0		5.5		4.0		40		4.0		40	μA
ΔI_{CC}	Supply current, TTL inputs High[2]	One input at 3.4V, other inputs at V_{CC} or GND		5.5						0.9		1.0	mA

NOTES:
1. Not more than one output should be tested at a time, and the duration of the test should not exceed 10ms.
2. This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0V or V_{CC}.

AC ELECTRICAL CHARACTERISTICS AT 3.3V ±0.3V

SYMBOL	PARAMETER	WAVEFORM	74AC11020					UNIT
			T_A = +25°C			T_A = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay nA, nB, nC, nD to n$\overline{Y}$	1	1.5 1.5	6.4 6.4	8.6 9.2	1.5 1.5	9.4 10.1	ns

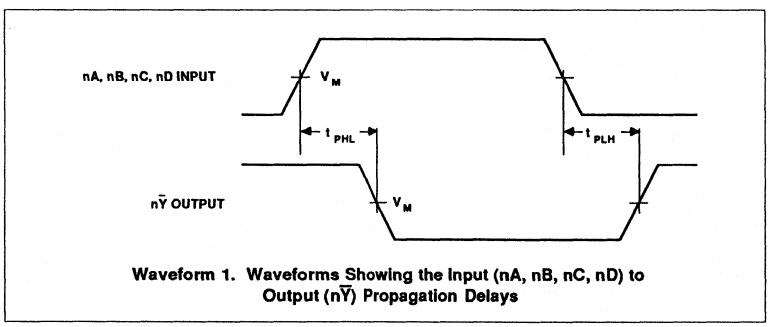
AC ELECTRICAL CHARACTERISTICS AT 5.0V ±0.5V

SYMBOL	PARAMETER	WAVEFORM	74AC11020					UNIT
			T_A = +25°C			T_A = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay nA, nB, nC, nD to n$\overline{Y}$	1	1.5 1.5	4.3 4.4	6.3 6.7	1.5 1.5	6.7 7.3	ns

AC ELECTRICAL CHARACTERISTICS AT 5.0V ±0.5V

SYMBOL	PARAMETER	WAVEFORM	74ACT11020					UNIT
			T_A = +25°C			T_A = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay nA, nB, nC, nD to n$\overline{Y}$	1	1.5 1.5	5.6 6.1	8.5 8.4	1.5 1.5	9.1 9.2	ns

AC WAVEFORMS

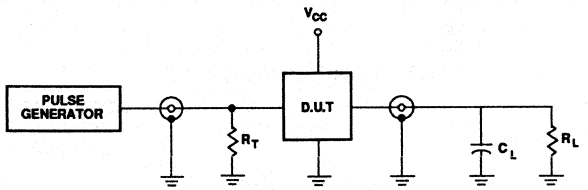


Waveform 1. Waveforms Showing the Input (nA, nB, nC, nD) to Output (n$\overline{Y}$) Propagation Delays

WAVEFORM CONDITIONS

	INPUTS	OUTPUTS
AC	V_{IN} = GND to V_{CC}, V_M = 50% V_{CC}	V_{OUT} = V_{OL} to V_{OH}
ACT	V_{IN} = GND to 3.0V, V_M = 1.5V	V_M = 50% V_{CC}

TEST CIRCUIT



Test Circuit

DEFINITIONS

C_L = Load capacitance, 50pF; includes jig and probe capacitance

R_L = Load resistor, 500Ω

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators

Input pulses: PRR ≤ 10MHz

$t_r = t_f$ = 3ns

74AC/ACT11021

Dual 4-Input AND Gate

Product Specification

FEATURES

- **Output capability: ±24 mA**
- **CMOS (AC) and TTL (ACT) voltage level inputs**
- **50Ω incident wave switching**
- **Center-pin V_{CC} and ground configuration to minimize high-speed switching noise**
- **I_{CC} category: SSI**

DESCRIPTION

The 74AC/ACT11021 high-performance CMOS devices combine very high speed and high output drive comparable to the most advanced TTL families.

The 74AC/ACT11021 provides two separate 4-input AND gate functions.

GENERAL INFORMATION

SYMBOL	PARAMETER	CONDITIONS T_A = 25°C; GND = 0V; V_{CC} = 5.0V	TYPICAL		UNIT
			AC	ACT	
t_{PLH}/ t_{PHL}	Propagation delay A, B, C, D to Y	C_L = 50pF	5.1	6.1	ns
C_{PD}	Power dissipation capacitance per gate[1]	f = 1MHz; C_L = 50pF	38	37	pF
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	3.5	3.5	pF
I_{LATCH}	Latch-up current	Per Jedec JC40.2 Standard 17	500	500	mA

Note:

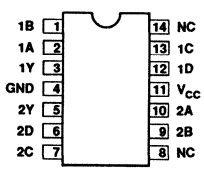
1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_I + \Sigma (C_L \times V_{CC}^2 \times f_O)$ where:
   f_I = input frequency in MHz, C_L = output load capacitance in pF,
   f_O = output frequency in MHz, V_{CC} = supply voltage in V,
   $\Sigma (C_L \times V_{CC}^2 \times f_O)$ = sum of outputs

ORDERING INFORMATION

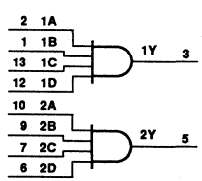
PACKAGES	TEMPERATURE RANGE	ORDER CODE
14-pin plastic DIP (300mil-wide)	-40°C to +85°C	74AC11021N 74ACT11021N
14-pin plastic SO (150mil-wide)	-40°C to +85°C	74AC11021D 74ACT11021D

PIN CONFIGURATION

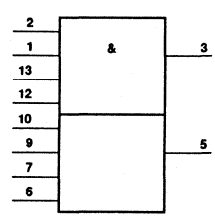
N and D Packages



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
2, 10	1A - 2A	Data inputs
1, 9	1B - 2B	Data inputs
13, 7	1C - 2C	Data inputs
12, 6	1D - 2D	Data inputs
3, 5	1Y - 2Y	Data outputs
4	GND	Ground (0V)
11	V_{CC}	Positive supply voltage

FUNCTION TABLE

INPUTS				OUTPUT
nA	nB	nC	nD	nY
H	H	H	H	H
L	X	X	X	L
X	L	X	X	L
X	X	L	X	L
X	X	X	L	L

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	74AC11021			74ACT11021			UNIT
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	DC supply voltage	3.0[1]	5.0	5.5	4.5	5.0	5.5	V
V_I	Input voltage	0		V_{CC}	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	0		V_{CC}	V
$\Delta t/\Delta v$	Input transition rise or fall rate	0		10	0		10	ns/V
T_A	Operating free-air temperature	-40		+85	-40		+85	°C

NOTE:

1. No electrical or switching characteristics are specified at $V_{CC} < 3V$. Operation between 2V and 3V is not recommended, but within that range, a device output will maintain a previously established logic state.

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	TEST CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 to+7.0	V
I_{IK} or V_I	DC input diode current[2]	$V_I < 0$	-20	mA
		$V_I > V_{CC}$	20	
	DC input voltage		-0.5 to V_{CC} +0.5	V
I_{OK} or V_O	DC output diode current[2]	$V_O < 0$	-50	mA
		$V_O > V_{CC}$	50	
	DC output voltage		-0.5 to V_{CC} +0.5	V
I_O	DC output source or sink current per output pin	V_O = 0 to V_{CC}	±50	mA
I_{CC} or I_{GND}	DC V_{CC} current		±100	mA
	DC ground current		±100	
T_{STG}	Storage temperature		-65 to 150	°C
P_{TOT}	Power dissipation per package Plastic DIP	Above 70°C:derate linearly by 8mW/K	500	mW
	Power dissipation per package Plastic surface mount (SO)	Above 70°C:derate linearly by 6mW/K	400	mW

NOTES:

1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		V_{CC}	74AC11021				74ACT11021				UNIT
					T_A = +25°C		T_A = -40°C to +85°C		T_A = +25°C		T_A = -40°C to +85°C		
				V	Min	Max	Min	Max	Min	Max	Min	Max	
V_{IH}	High-level input voltage			3.0	2.10		2.10						V
				4.5	3.15		3.15		2.0		2.0		
				5.5	3.85		3.85		2.0		2.0		
V_{IL}	Low-level input voltage			3.0		0.90		0.90					V
				4.5		1.35		1.35		0.8		0.8	
				5.5		1.65		1.65		0.8		0.8	
V_{OH}	High-level output voltage	V_I = V_{IL} or V_{IH}	I_{OH} = -50μA	3.0	2.9		2.9						V
				4.5	4.4		4.4		4.4		4.4		
				5.5	5.4		5.4		5.4		5.4		
			I_{OH} = -4mA	3.0	2.58		2.48						
			I_{OH} = -24mA	4.5	3.94		3.8		3.94		3.8		
				5.5	4.94		4.8		4.94		4.8		
			I_{OH} = -75mA[1]	5.5			3.85				3.85		
V_{OL}	Low-level output voltage	V_I = V_{IL} or V_{IH}	I_{OL} = 50μA	3.0		0.1		0.1					V
				4.5		0.1		0.1		0.1		0.1	
				5.5		0.1		0.1		0.1		0.1	
			I_{OL} = 12mA	3.0		0.36		0.44					
			I_{OL} = 24mA	4.5		0.36		0.44		0.36		0.44	
				5.5		0.36		0.44		0.36		0.44	
			I_{OL} = 75mA[1]	5.5				1.65				1.65	
I_I	Input leakage current	V_I = V_{CC} or GND		5.5		±0.1		±1.0		±0.1		±1.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC} or GND, I_O = 0		5.5		4.0		40		4.0		40	μA
ΔI_{CC}	Supply current, TTL inputs High[2]	One input at 3.4V, other inputs at V_{CC} or GND		5.5						0.9		1.0	mA

NOTES:
1. Not more than one output should be tested at a time, and the duration of the test should not exceed 10ms.
2. This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0V or V_{CC}.

AC ELECTRICAL CHARACTERISTICS AT 3.3V ±0.3V

SYMBOL	PARAMETER	WAVEFORM	74AC11021					UNIT
			T_A = +25°C			T_A = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay nA, nB, nC, nD to nY	1	1.5 1.5	8.2 6.4	11.4 8.7	1.5 1.5	13.0 9.3	ns

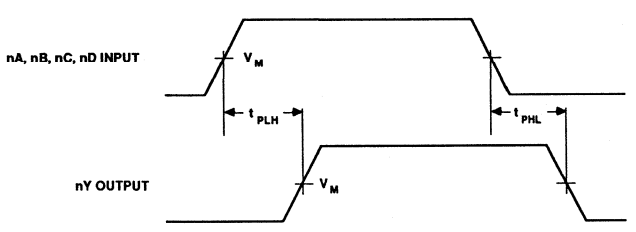
AC ELECTRICAL CHARACTERISTICS AT 5.0V ±0.5V

SYMBOL	PARAMETER	WAVEFORM	74AC11021					UNIT
			T_A = +25°C			T_A = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay nA, nB, nC, nD to nY	1	1.5 1.5	5.6 4.6	7.8 6.5	1.5 1.5	8.8 6.9	ns

AC ELECTRICAL CHARACTERISTICS AT 5.0V ±0.5V

SYMBOL	PARAMETER	WAVEFORM	74ACT11021					UNIT
			T_A = +25°C			T_A = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay nA, nB, nC, nD to nY	1	1.5 1.5	6.7 5.4	8.8 8.3	1.5 1.5	9.8 8.9	ns

AC WAVEFORMS

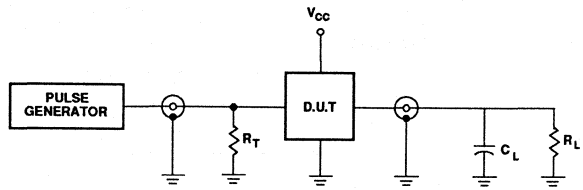


Waveform 1. Waveforms Showing the Input (nA, nB, nC, nD) to Output (nY) Propagation Delays

WAVEFORM CONDITIONS

	INPUTS	OUTPUTS
AC	V_{IN} = GND to V_{CC}, V_M = 50% V_{CC}	V_{OUT} = V_{OL} to V_{OH}
ACT	V_{IN} = GND to 3.0V, V_M = 1.5V	V_M = 50% V_{CC}

TEST CIRCUIT



Test Circuit

DEFINITIONS

C_L = Load capacitance, 50pF; includes jig and probe capacitance

R_L = Load resistor, 500Ω

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators

Input pulses: PRR ≤ 10MHz

$t_r = t_f$ = 3ns

74AC/ACT11027

Triple 3-Input NOR Gate

Product Specification

FEATURES

- **Output capability: ±24 mA**
- **CMOS (AC) and TTL (ACT) voltage level inputs**
- **50Ω incident wave switching**
- **Center-pin V_{CC} and ground configuration to minimize high-speed switching noise**
- **I_{CC} category: SSI**

DESCRIPTION

The 74AC/ACT11027 high-performance CMOS devices combine very high speed and high output drive comparable to the most advanced TTL families.

The 74AC/ACT11027 provides three separate 3-input NOR gate functions.

GENERAL INFORMATION

SYMBOL	PARAMETER	CONDITIONS T_A = 25°C; GND = 0V; V_{CC} = 5.0V	TYPICAL		UNIT
			AC	ACT	
t_{PLH}/t_{PHL}	Propagation delay A, B, C to $\overline{Y}$	C_L = 50pF	4.4	5.5	ns
C_{PD}	Power dissipation capacitance per gate[1]	f = 1MHz; C_L = 50pF	24	27	pF
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	3.5	3.5	pF
I_{LATCH}	Latch-up current	Per Jedec JC40.2 Standard 17	500	500	mA

Note:

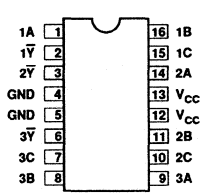
1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_I + \Sigma (C_L \times V_{CC}^2 \times f_O)$ where:
   f_I = input frequency in MHz, C_L = output load capacitance in pF,
   f_O = output frequency in MHz, V_{CC} = supply voltage in V,
   $\Sigma (C_L \times V_{CC}^2 \times f_O)$ = sum of outputs

ORDERING INFORMATION

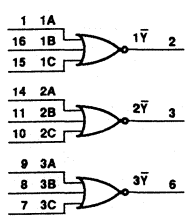
PACKAGES	TEMPERATURE RANGE	ORDER CODE
16-pin plastic DIP (300mil-wide)	-40°C to +85°C	74AC11027N 74ACT11027N
16-pin plastic SO (150mil-wide)	-40°C to +85°C	74AC11027D 74ACT11027D

PIN CONFIGURATION

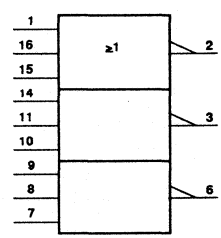
N and D Packages



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
1, 14, 9	1A - 3A	Data inputs
16, 11, 8	1B - 3B	Data inputs
15, 10, 7	1C - 3C	Data inputs
2, 3, 6	$1\overline{Y}$ - $3\overline{Y}$	Data outputs
4, 5	GND	Ground (0V)
12, 13	V_{CC}	Positive supply voltage

INPUTS			OUTPUT
nA	nB	nC	$n\overline{Y}$
L	L	L	H
X	X	H	L
X	H	X	L
H	X	X	L

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	74AC11027			74ACT11027			UNIT
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	DC supply voltage	3.0[1]	5.0	5.5	4.5	5.0	5.5	V
V_I	Input voltage	0		V_{CC}	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	0		V_{CC}	V
$\Delta t/\Delta v$	Input transition rise or fall rate	0		10	0		10	ns/V
T_A	Operating free-air temperature	-40		+85	-40		+85	°C

NOTE:

1. No electrical or switching characteristics are specified at $V_{CC} < 3V$. Operation between 2V and 3V is not recommended, but within that range, a device output will maintain a previously established logic state.

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	TEST CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 to+7.0	V
I_{IK} or V_I	DC input diode current[2]	$V_I < 0$	-20	mA
		$V_I > V_{CC}$	20	
	DC input voltage		-0.5 to V_{CC} +0.5	V
I_{OK} or V_O	DC output diode current[2]	$V_O < 0$	-50	mA
		$V_O > V_{CC}$	50	
	DC output voltage		-0.5 to V_{CC} +0.5	V
I_O	DC output source or sink current per output pin	V_O = 0 to V_{CC}	±50	mA
I_{CC} or I_{GND}	DC V_{CC} current		±100	mA
	DC ground current		±100	
T_{STG}	Storage temperature		-65 to 150	°C
P_{TOT}	Power dissipation per package Plastic DIP	Above 70°C:derate linearly by 8mW/K	500	mW
	Power dissipation per package Plastic surface mount (SO)	Above 70°C:derate linearly by 6mW/K	400	mW

NOTES:

1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		V_{CC}	74AC11027				74ACT11027				UNIT
					T_A = +25°C		T_A = -40°C to +85°C		T_A = +25°C		T_A = -40°C to +85°C		
				V	Min	Max	Min	Max	Min	Max	Min	Max	
V_{IH}	High-level input voltage			3.0	2.10		2.10						V
				4.5	3.15		3.15		2.0		2.0		
				5.5	3.85		3.85		2.0		2.0		
V_{IL}	Low-level input voltage			3.0		0.90		0.90					V
				4.5		1.35		1.35		0.8		0.8	
				5.5		1.65		1.65		0.8		0.8	
V_{OH}	High-level output voltage	V_I = V_{IL} or V_{IH}	I_{OH} = -50μA	3.0	2.9		2.9						V
				4.5	4.4		4.4		4.4		4.4		
				5.5	5.4		5.4		5.4		5.4		
			I_{OH} = -4mA	3.0	2.58		2.48						
			I_{OH} = -24mA	4.5	3.94		3.8		3.94		3.8		
				5.5	4.94		4.8		4.94		4.8		
			I_{OH} = -75mA[1]	5.5			3.85				3.85		
V_{OL}	Low-level output voltage	V_I = V_{IL} or V_{IH}	I_{OL} = 50μA	3.0		0.1		0.1					V
				4.5		0.1		0.1		0.1		0.1	
				5.5		0.1		0.1		0.1		0.1	
			I_{OL} = 12mA	3.0		0.36		0.44					
			I_{OL} = 24mA	4.5		0.36		0.44		0.36		0.44	
				5.5		0.36		0.44		0.36		0.44	
			I_{OL} = 75mA[1]	5.5				1.65				1.65	
I_I	Input leakage current	V_I = V_{CC} or GND		5.5		±0.1		±1.0		±0.1		±1.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC} or GND, I_O = 0		5.5		4.0		40		4.0		40	μA
ΔI_{CC}	Supply current, TTL inputs High[2]	One input at 3.4V, other inputs at V_{CC} or GND		5.5						0.9		1.0	mA

NOTES:
1. Not more than one output should be tested at a time, and the duration of the test should not exceed 10ms.
2. This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0V or V_{CC}.

AC ELECTRICAL CHARACTERISTICS AT 3.3V ±0.3V

SYMBOL	PARAMETER	WAVEFORM	74AC11027					UNIT
			T_A = +25°C			T_A = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay nA, nB, nC to n$\overline{Y}$	1	1.5 1.5	6.3 7.6	9.8 10.9	1.5 1.5	10.9 12.0	ns

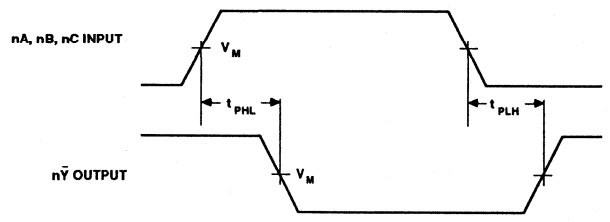
AC ELECTRICAL CHARACTERISTICS AT 5.0V ±0.5V

SYMBOL	PARAMETER	WAVEFORM	74AC11027					UNIT
			T_A = +25°C			T_A = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay nA, nB, nC to n$\overline{Y}$	1	1.5 1.5	4.3 4.5	6.8 7.5	1.5 1.5	7.7 8.1	ns

AC ELECTRICAL CHARACTERISTICS AT 5.0V ±0.5V

SYMBOL	PARAMETER	WAVEFORM	74ACT11027					UNIT
			T_A = +25°C			T_A = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay nA, nB, nC to n$\overline{Y}$	1	1.5 1.5	5.0 6.0	9.2 8.6	1.5 1.5	10.1 9.4	ns

AC WAVEFORMS

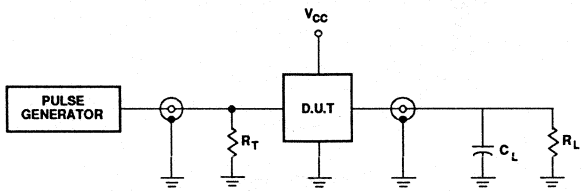


Waveform 1. Waveforms Showing the Input (nA, nB, nC) to Output (n$\overline{Y}$) Propagation Delays

WAVEFORM CONDITIONS

	INPUTS	OUTPUTS
AC	V_{IN} = GND to V_{CC}, V_M = 50% V_{CC}	V_{OUT} = V_{OL} to V_{OH}
ACT	V_{IN} = GND to 3.0V, V_M = 1.5V	V_M = 50% V_{CC}

TEST CIRCUIT



Test Circuit

DEFINITIONS

C_L = Load capacitance, 50pF; includes jig and probe capacitance

R_L = Load resistor, 500Ω

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators

Input pulses: PRR ≤ 10MHz

$t_r = t_f$ = 3ns

74AC/ACT11030

8-Input NAND Gate

Product Specification

FEATURES

- **Output capability: ±24 mA**
- **CMOS (AC) and TTL (ACT) voltage level inputs**
- **50Ω incident wave switching**
- **Center-pin V_{CC} and ground configuration to minimize high-speed switching noise**
- **I_{CC} category: SSI**

DESCRIPTION

The 74AC/ACT11030 high-performance CMOS devices combine very high speed and high output drive comparable to the most advanced TTL families.

The 74AC/ACT11030 provides one 8-input NAND gate function.

GENERAL INFORMATION

SYMBOL	PARAMETER	CONDITIONS T_A = 25°C; GND = 0V; V_{CC} = 5.0V	TYPICAL		UNIT
			AC	ACT	
t_{PLH}/ t_{PHL}	Propagation delay A through H to $\overline{Y}$	C_L = 50pF	4.8	5.7	ns
C_{PD}	Power dissipation capacitance per gate[1]	f = 1MHz; C_L = 50pF	42	41	pF
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	3.5	3.5	pF
I_{LATCH}	Latch-up current	Per Jedec JC40.2 Standard 17	500	500	mA

Note:

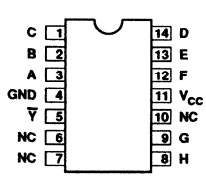
1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_I + \Sigma (C_L \times V_{CC}^2 \times f_O)$ where:
   f_I = input frequency in MHz, C_L = output load capacitance in pF,
   f_O = output frequency in MHz, V_{CC} = supply voltage in V,
   $\Sigma (C_L \times V_{CC}^2 \times f_O)$ = sum of outputs

ORDERING INFORMATION

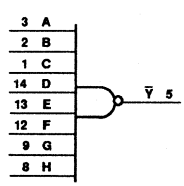
PACKAGES	TEMPERATURE RANGE	ORDER CODE
14-pin plastic DIP (300mil-wide)	-40°C to +85°C	74AC11030N 74ACT11030N
14-pin plastic SO (150mil-wide)	-40°C to +85°C	74AC11030D 74ACT11030D

PIN CONFIGURATION

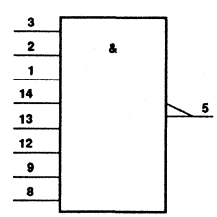
N and D Packages



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
3, 2, 1, 14 13, 12, 9, 8	A, B, C, D, E, F, G, H	Data inputs
5	$\overline{Y}$	Data output
4	GND	Ground (0V)
11	V_{CC}	Positive supply voltage

FUNCTION TABLE

INPUTS	OUTPUT
A through H	$\overline{Y}$
All inputs H	L
One or more inputs L	H

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	74AC11030			74ACT11030			UNIT
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	DC supply voltage	3.0[1]	5.0	5.5	4.5	5.0	5.5	V
V_I	Input voltage	0		V_{CC}	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	0		V_{CC}	V
$\Delta t/\Delta v$	Input transition rise or fall rate	0		10	0		10	ns/V
T_A	Operating free-air temperature	-40		+85	-40		+85	°C

NOTE:
1. No electrical or switching characteristics are specified at V_{CC} < 3V. Operation between 2V and 3V is not recommended, but within that range, a device output will maintain a previously established logic state.

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	TEST CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 to+7.0	V
I_{IK} or V_I	DC input diode current[2]	$V_I < 0$	-20	mA
		$V_I > V_{CC}$	20	
	DC input voltage		-0.5 to V_{CC} +0.5	V
I_{OK} or V_O	DC output diode current[2]	$V_O < 0$	-50	mA
		$V_O > V_{CC}$	50	
	DC output voltage		-0.5 to V_{CC} +0.5	V
I_O	DC output source or sink current per output pin	V_O = 0 to V_{CC}	±50	mA
I_{CC} or I_{GND}	DC V_{CC} current		±100	mA
	DC ground current		±100	
T_{STG}	Storage temperature		-65 to 150	°C
P_{TOT}	Power dissipation per package Plastic DIP	Above 70°C:derate linearly by 8mW/K	500	mW
	Power dissipation per package Plastic surface mount (SO)	Above 70°C:derate linearly by 6mW/K	400	mW

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		V_{CC}	74AC11030				74ACT11030				UNIT
					T_A = +25°C		T_A = -40°C to +85°C		T_A = +25°C		T_A = -40°C to +85°C		
				V	Min	Max	Min	Max	Min	Max	Min	Max	
V_{IH}	High-level input voltage			3.0	2.10		2.10						V
				4.5	3.15		3.15		2.0		2.0		
				5.5	3.85		3.85		2.0		2.0		
V_{IL}	Low-level input voltage			3.0		0.90		0.90					V
				4.5		1.35		1.35		0.8		0.8	
				5.5		1.65		1.65		0.8		0.8	
V_{OH}	High-level output voltage	V_I = V_{IL} or V_{IH}	I_{OH} = -50μA	3.0	2.9		2.9						V
				4.5	4.4		4.4		4.4		4.4		
				5.5	5.4		5.4		5.4		5.4		
			I_{OH} = -4mA	3.0	2.58		2.48						
			I_{OH} = -24mA	4.5	3.94		3.8		3.94		3.8		
				5.5	4.94		4.8		4.94		4.8		
			I_{OH} = -75mA[1]	5.5			3.85				3.85		
V_{OL}	Low-level output voltage	V_I = V_{IL} or V_{IH}	I_{OL} = 50μA	3.0		0.1		0.1					V
				4.5		0.1		0.1		0.1		0.1	
				5.5		0.1		0.1		0.1		0.1	
			I_{OL} = 12mA	3.0		0.36		0.44					
			I_{OL} = 24mA	4.5		0.36		0.44		0.36		0.44	
				5.5		0.36		0.44		0.36		0.44	
			I_{OL} = 75mA[1]	5.5				1.65				1.65	
I_I	Input leakage current	V_I = V_{CC} or GND		5.5		±0.1		±1.0		±0.1		±1.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC} or GND, I_O = 0		5.5		4.0		40		4.0		40	μA
ΔI_{CC}	Supply current, TTL inputs High[2]	One input at 3.4V, other inputs at V_{CC} or GND		5.5						0.9		1.0	mA

NOTES:
1. Not more than one output should be tested at a time, and the duration of the test should not exceed 10ms.
2. This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0V or V_{CC}.

AC ELECTRICAL CHARACTERISTICS AT 3.3V ±0.3V

SYMBOL	PARAMETER	WAVEFORM	74AC11030					UNIT
			T_A = +25°C			T_A = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay A, B, C, D, E, F, G, H to $\overline{Y}$	1	1.5 1.5	6.9 6.4	9.1 8.8	1.5 1.5	9.9 9.8	ns

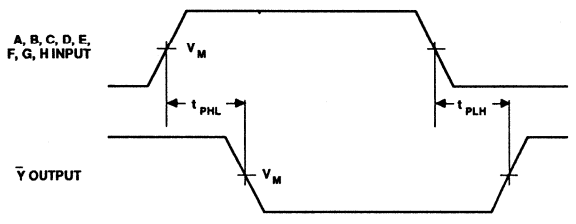
AC ELECTRICAL CHARACTERISTICS AT 5.0V ±0.5V

SYMBOL	PARAMETER	WAVEFORM	74AC11030					UNIT
			T_A = +25°C			T_A = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay A, B, C, D, E, F, G, H to $\overline{Y}$	1	1.5 1.5	4.8 4.8	6.7 6.7	1.5 1.5	7.2 7.4	ns

AC ELECTRICAL CHARACTERISTICS AT 5.0V ±0.5V

SYMBOL	PARAMETER	WAVEFORM	74ACT11030					UNIT
			T_A = +25°C			T_A = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay A, B, C, D, E, F, G, H to $\overline{Y}$	1	1.5 1.5	5.4 5.9	8.1 7.8	1.5 1.5	8.5 8.7	ns

AC WAVEFORMS

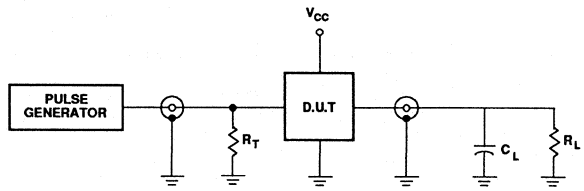


Waveform 1. Waveforms Showing the Input (A, B, C, D, E, F, G, H) to Output ($\overline{Y}$) Propagation Delays.

WAVEFORM CONDITIONS

	INPUTS	OUTPUTS
AC	V_{IN} = GND to V_{CC}, V_M = 50% V_{CC}	V_{OUT} = V_{OL} to V_{OH}
ACT	V_{IN} = GND to 3.0V, V_M = 1.5V	V_M = 50% V_{CC}

TEST CIRCUIT



Test Circuit

DEFINITIONS

C_L = Load capacitance, 50pF; includes jig and probe capacitance

R_L = Load resistor, 500Ω

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators

Input pulses: PRR ≤ 10MHz

$t_r = t_f = 3ns$

74AC/ACT11032
Quad 2-Input OR Gate
Product Specification

FEATURES

- **Output capability: ±24 mA**
- **CMOS (AC) and TTL (ACT) voltage level inputs**
- **50Ω incident wave switching**
- **Center-pin V_{CC} and ground configuration to minimize high-speed switching noise**
- **I_{CC} category: SSI**

DESCRIPTION

The 74AC/ACT11032 high-performance CMOS devices combine very high speed and high output drive comparable to the most advanced TTL families.

The 74AC/ACT11032 provides four separate 2-input OR gate functions.

GENERAL INFORMATION

SYMBOL	PARAMETER	CONDITIONS T_A = 25°C; GND = 0V; V_{CC} = 5.0V	TYPICAL		UNIT
			AC	ACT	
t_{PLH}/ t_{PHL}	Propagation delay A, B, to Y	C_L = 50pF	4.1	5.6	ns
C_{PD}	Power dissipation capacitance per gate[1]	f = 1MHz; C_L = 50pF	24	25	pF
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	3.5	3.5	pF
I_{LATCH}	Latch-up current	Per Jedec JC40.2 Standard 17	500	500	mA

Note:

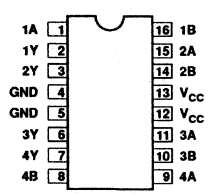
1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_I + \Sigma (C_L \times V_{CC}^2 \times f_O)$ where:
   f_I = input frequency in MHz, C_L = output load capacitance in pF,
   f_O = output frequency in MHz, V_{CC} = supply voltage in V,
   $\Sigma (C_L \times V_{CC}^2 \times f_O)$ = sum of outputs

ORDERING INFORMATION

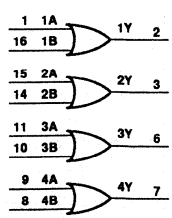
PACKAGES	TEMPERATURE RANGE	ORDER CODE
16-pin plastic DIP (300mil-wide)	-40°C to +85°C	74AC11032N 74ACT11032N
16-pin plastic SO (150mil-wide)	-40°C to +85°C	74AC11032D 74ACT11032D

PIN CONFIGURATION

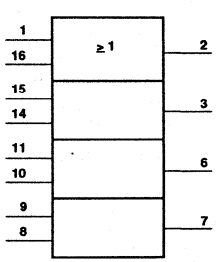
N and D Packages



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
1, 15, 11, 9	1A - 4A	Data inputs
16, 14, 10, 8	1B - 4B	Data inputs
2, 3, 6, 7	1Y - 4Y	Data outputs
4, 5	GND	Ground (0V)
12, 13	V_{CC}	Positive supply voltage

FUNCTION TABLE

INPUTS		OUTPUT
nA	nB	nY
L	L	L
L	H	H
H	L	H
H	H	H

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	74AC11032			74ACT11032			UNIT
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	DC supply voltage	3.0[1]	5.0	5.5	4.5	5.0	5.5	V
V_I	Input voltage	0		V_{CC}	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	0		V_{CC}	V
$\Delta t/\Delta v$	Input transition rise or fall rate	0		10	0		10	ns/V
T_A	Operating free-air temperature	-40		+85	-40		+85	°C

NOTE:

1. No electrical or switching characteristics are specified at $V_{CC} < 3V$. Operation between 2V and 3V is not recommended, but within that range, a device output will maintain a previously established logic state.

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	TEST CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 to+7.0	V
I_{IK} or V_I	DC input diode current[2]	$V_I < 0$	-20	mA
		$V_I > V_{CC}$	20	
	DC input voltage		-0.5 to V_{CC} +0.5	V
I_{OK} or V_O	DC output diode current[2]	$V_O < 0$	-50	mA
		$V_O > V_{CC}$	50	
	DC output voltage		-0.5 to V_{CC} +0.5	V
I_O	DC output source or sink current per output pin	V_O = 0 to V_{CC}	±50	mA
I_{CC} or I_{GND}	DC V_{CC} current		±100	mA
	DC ground current		±100	
T_{STG}	Storage temperature		-65 to 150	°C
P_{TOT}	Power dissipation per package Plastic DIP	Above 70°C:derate linearly by 8mW/K	500	mW
	Power dissipation per package Plastic surface mount (SO)	Above 70°C:derate linearly by 6mW/K	400	mW

NOTES:

1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		V_{CC}	74AC11032				74ACT11032				UNIT
					T_A = +25°C		T_A = -40°C to +85°C		T_A = +25°C		T_A = -40°C to +85°C		
				V	Min	Max	Min	Max	Min	Max	Min	Max	
V_{IH}	High-level input voltage			3.0	2.10		2.10						V
				4.5	3.15		3.15		2.0		2.0		
				5.5	3.85		3.85		2.0		2.0		
V_{IL}	Low-level input voltage			3.0		0.90		0.90					V
				4.5		1.35		1.35		0.8		0.8	
				5.5		1.65		1.65		0.8		0.8	
V_{OH}	High-level output voltage	V_I = V_{IL} or V_{IH}	I_{OH} = -50μA	3.0	2.9		2.9						V
				4.5	4.4		4.4		4.4		4.4		
				5.5	5.4		5.4		5.4		5.4		
			I_{OH} = -4mA	3.0	2.58		2.48						
			I_{OH} = -24mA	4.5	3.94		3.8		3.94		3.8		
				5.5	4.94		4.8		4.94		4.8		
			I_{OH} = -75mA[1]	5.5			3.85				3.85		
V_{OL}	Low-level output voltage	V_I = V_{IL} or V_{IH}	I_{OL} = 50μA	3.0		0.1		0.1					V
				4.5		0.1		0.1		0.1		0.1	
				5.5		0.1		0.1		0.1		0.1	
			I_{OL} = 12mA	3.0		0.36		0.44					
			I_{OL} = 24mA	4.5		0.36		0.44		0.36		0.44	
				5.5		0.36		0.44		0.36		0.44	
			I_{OL} = 75mA[1]	5.5				1.65				1.65	
I_I	Input leakage current	V_I = V_{CC} or GND		5.5		±0.1		±1.0		±0.1		±1.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC} or GND, I_O = 0		5.5		4.0		40		4.0		40	μA
ΔI_{CC}	Supply current, TTL inputs High[2]	One input at 3.4V, other inputs at V_{CC} or GND		5.5						0.9		1.0	mA

NOTES:
1. Not more than one output should be tested at a time, and the duration of the test should not exceed 10ms.
2. This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0V or V_{CC}.

AC ELECTRICAL CHARACTERISTICS AT 3.3V ±0.3V

SYMBOL	PARAMETER	WAVEFORM	74AC11002					UNIT
			T_A = +25°C			T_A = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay nA, nB to nY	1	1.5 1.5	6.3 5.4	8.7 7.4	1.5 1.5	9.7 8.0	ns

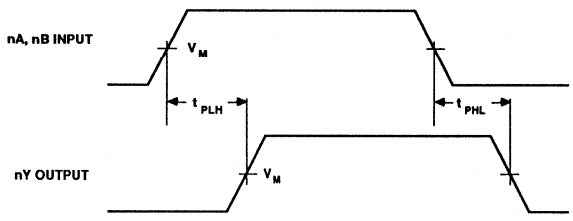
AC ELECTRICAL CHARACTERISTICS AT 5.0V ±0.5V

SYMBOL	PARAMETER	WAVEFORM	74AC11032					UNIT
			T_A = +25°C			T_A = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay nA, nB to nY	1	1.5 1.5	4.3 3.8	6.2 5.5	1.5 1.5	6.7 5.9	ns

AC ELECTRICAL CHARACTERISTICS AT 5.0V ±0.5V

SYMBOL	PARAMETER	WAVEFORM	74ACT11032					UNIT
			T_A = +25°C			T_A = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay nA, nB to nY	1	1.5 1.5	6.2 4.9	8.1 7.4	1.5 1.5	9.0 8.0	ns

AC WAVEFORMS

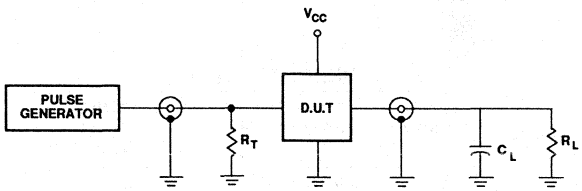


Waveform 1. Waveforms Showing the Input (nA, nB) to Output (nY) Propagation Delays

WAVEFORM CONDITIONS

	INPUTS	OUTPUTS
AC	V_{IN} = GND to V_{CC}, V_M = 50% V_{CC}	V_{OUT} = V_{OL} to V_{OH}
ACT	V_{IN} = GND to 3.0V, V_M = 1.5V	V_M = 50% V_{CC}

TEST CIRCUIT



Test Circuit

DEFINITIONS

C_L = Load capacitance, 50pF; includes jig and probe capacitance

R_L = Load resistor, 500Ω

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators

Input pulses: PRR ≤ 10MHz

$t_r = t_f = 3ns$

74AC/ACT11034

Hex Non-Inverter

Product Specification

FEATURES

- **Output capability: ±24 mA**
- **CMOS (AC) and TTL (ACT) voltage level inputs**
- **50Ω incident wave switching**
- **Center-pin V_{CC} and ground configuration to minimize high-speed switching noise**
- **I_{CC} category: SSI**

DESCRIPTION

The 74AC/ACT11034 high-performance CMOS devices combine very high speed and high output drive comparable to the most advanced TTL families.

The 74AC/ACT11034 provides six separate non-inverters.

GENERAL INFORMATION

SYMBOL	PARAMETER	CONDITIONS T_A = 25°C; GND = 0V; V_{CC} = 5.0V	TYPICAL		UNIT
			AC	ACT	
t_{PLH}/t_{PHL}	Propagation delay A, B, to Y	C_L = 50pF	4.0	5.7	ns
C_{PD}	Power dissipation capacitance per gate[1]	f = 1MHz; C_L = 50pF	27	29	pF
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	3.5	3.5	pF
I_{LATCH}	Latch-up current	Per Jedec JC40.2 Standard 17	500	500	mA

Note:

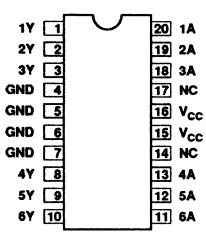
1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_I + \Sigma (C_L \times V_{CC}^2 \times f_O)$ where:
   f_I = input frequency in MHz, C_L = output load capacitance in pF,
   f_O = output frequency in MHz, V_{CC} = supply voltage in V,
   $\Sigma (C_L \times V_{CC}^2 \times f_O)$ = sum of outputs

ORDERING INFORMATION

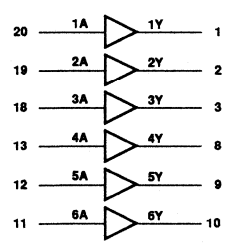
PACKAGES	TEMPERATURE RANGE	ORDER CODE
20-pin plastic DIP (300mil-wide)	-40°C to +85°C	74AC11034N 74ACT11034N
20-pin plastic SO (300mil-wide)	-40°C to +85°C	74AC11034D 74ACT11034D

PIN CONFIGURATION

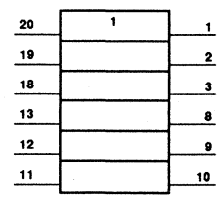
N and D Packages



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
20, 19, 18, 13, 12, 11	1A - 6A	Data inputs
1, 2, 3, 8, 9, 10	1Y - 6Y	Data outputs
4, 5, 6, 7	GND	Ground (0V)
15, 16	V_{CC}	Positive supply voltage

FUNCTION TABLE

INPUT	OUTPUT
nA	nY
L	L
H	H

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	74AC11034			74ACT11034			UNIT
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	DC supply voltage	3.0[1]	5.0	5.5	4.5	5.0	5.5	V
V_I	Input voltage	0		V_{CC}	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	0		V_{CC}	V
$\Delta t/\Delta v$	Input transition rise or fall rate	0		10	0		10	ns/V
T_A	Operating free-air temperature	-40		+85	-40		+85	°C

NOTE:
1. No electrical or switching characteristics are specified at $V_{CC} < 3V$. Operation between 2V and 3V is not recommended, but within that range, a device output will maintain a previously established logic state.

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	TEST CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 to+7.0	V
I_{IK} or V_I	DC input diode current[2]	$V_I < 0$	-20	mA
		$V_I > V_{CC}$	20	
	DC input voltage		-0.5 to V_{CC} +0.5	V
I_{OK} or V_O	DC output diode current[2]	$V_O < 0$	-50	mA
		$V_O > V_{CC}$	50	
	DC output voltage		-0.5 to V_{CC} +0.5	V
I_O	DC output source or sink current per output pin	V_O = 0 to V_{CC}	±50	mA
I_{CC} or I_{GND}	DC V_{CC} current		±150	mA
	DC ground current		±150	
T_{STG}	Storage temperature		-65 to 150	°C
P_{TOT}	Power dissipation per package Plastic DIP	Above 70°C:derate linearly by 8mW/K	500	mW
	Power dissipation per package Plastic surface mount (SO)	Above 70°C:derate linearly by 6mW/K	400	mW

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		V_{CC}	74AC11034				74ACT11034				UNIT
					T_A = +25°C		T_A = -40°C to +85°C		T_A = +25°C		T_A = -40°C to +85°C		
				V	Min	Max	Min	Max	Min	Max	Min	Max	
V_{IH}	High-level input voltage			3.0	2.10		2.10						V
				4.5	3.15		3.15		2.0		2.0		
				5.5	3.85		3.85		2.0		2.0		
V_{IL}	Low-level input voltage			3.0		0.90		0.90					V
				4.5		1.35		1.35		0.8		0.8	
				5.5		1.65		1.65		0.8		0.8	
V_{OH}	High-level output voltage	V_I = V_{IL} or V_{IH}	I_{OH} = -50μA	3.0	2.9		2.9						V
				4.5	4.4		4.4		4.4		4.4		
				5.5	5.4		5.4		5.4		5.4		
			I_{OH} = -4mA	3.0	2.58		2.48						
			I_{OH} = -24mA	4.5	3.94		3.8		3.94		3.8		
				5.5	4.94		4.8		4.94		4.8		
			I_{OH} = -75mA[1]	5.5			3.85				3.85		
V_{OL}	Low-level output voltage	V_I = V_{IL} or V_{IH}	I_{OL} = 50μA	3.0		0.1		0.1					V
				4.5		0.1		0.1		0.1		0.1	
				5.5		0.1		0.1		0.1		0.1	
			I_{OL} = 12mA	3.0		0.36		0.44					
			I_{OL} = 24mA	4.5		0.36		0.44		0.36		0.44	
				5.5		0.36		0.44		0.36		0.44	
			I_{OL} = 75mA[1]	5.5				1.65				1.65	
I_I	Input leakage current	V_I = V_{CC} or GND		5.5		±0.1		±1.0		±0.1		±1.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC} or GND, I_O = 0		5.5		4.0		40		4.0		40	μA
ΔI_{CC}	Supply current, TTL inputs High[2]	One input at 3.4V, other inputs at V_{CC} or GND		5.5						0.9		1.0	mA

NOTES:
1. Not more than one output should be tested at a time, and the duration of the test should not exceed 10ms.
2. This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0V or V_{CC}.

AC ELECTRICAL CHARACTERISTICS AT 3.3V ±0.3V

SYMBOL	PARAMETER	WAVEFORM	74AC11034					UNIT
			T_A = +25°C			T_A = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay nA, nB to nY	1	1.5 1.5	5.7 5.5	9.1 8.3	1.5 1.5	10.1 9.2	ns

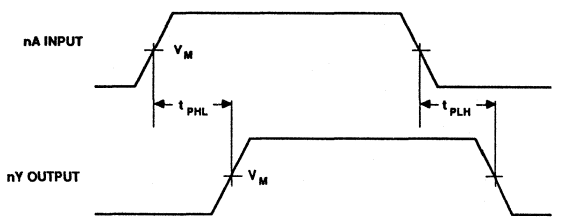
AC ELECTRICAL CHARACTERISTICS AT 5.0V ±0.5V

SYMBOL	PARAMETER	WAVEFORM	74AC11034					UNIT
			T_A = +25°C			T_A = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay nA, nB to nY	1	1.5 1.5	4.0 4.0	6.3 6.2	1.5 1.5	6.9 6.8	ns

AC ELECTRICAL CHARACTERISTICS AT 5.0V ±0.5V

SYMBOL	PARAMETER	WAVEFORM	74ACT11034					UNIT
			T_A = +25°C			T_A = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay nA, nB to nY	1	1.5 1.5	6.1 5.2	8.9 8.0	1.5 1.5	9.9 8.9	ns

AC WAVEFORMS

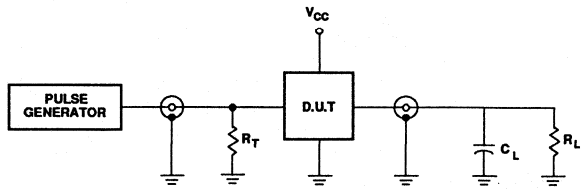


Waveform 1. Waveforms Showing the Input (nA) to Output (nY) Propagation Delays

WAVEFORM CONDITIONS

	INPUTS	OUTPUTS
AC	V_{IN} = GND to V_{CC}, V_M = 50% V_{CC}	V_{OUT} = V_{OL} to V_{OH}
ACT	V_{IN} = GND to 3.0V, V_M = 1.5V	V_M = 50% V_{CC}

TEST CIRCUIT



Test Circuit

DEFINITIONS

C_L = Load capacitance, 50pF; includes jig and probe capacitance

R_L = Load resistor, 500Ω

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators

Input pulses: PRR ≤ 10MHz

$t_r = t_f$ = 3ns

74AC/ACT11051

Dual 2-Wide 2-Input, 2-Wide 3-Input AND-OR-INVERT Gate

Objective Specification

FEATURES

- **Output capability: ±24 mA**
- **CMOS (AC) and TTL (ACT) voltage level inputs**
- **50Ω incident wave switching**
- **Center-pin V_{CC} and ground configuration to minimize high-speed switching noise**
- **I_{CC} category: SSI**

DESCRIPTION

The 74AC/ACT11051 high-performance CMOS devices combine very high speed and high output drive comparable to the most advanced TTL families.

GENERAL INFORMATION

SYMBOL	PARAMETER	CONDITIONS T_A = 25°C; GND = 0V; V_{CC} = 5.0V	TYPICAL		UNIT
			AC	ACT	
t_{PLH}/t_{PHL}	Propagation delay A, B, C, D, E, F to n$\overline{Y}$	C_L = 50pF	3.5	4.5	ns
C_{PD}	Power dissipation capacitance per gate[1]	f = 1MHz; C_L = 50pF	56	50	pF
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	3.5	3.5	pF
I_{LATCH}	Latch-up current	Per Jedec JC40.2 Standard 17	500	500	mA

Note:

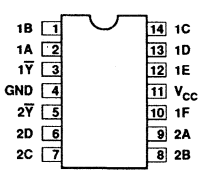
1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_I + \Sigma (C_L \times V_{CC}^2 \times f_O)$ where:
   f_I = input frequency in MHz, C_L = output load capacitance in pF,
   f_O = output frequency in MHz, V_{CC} = supply voltage in V,
   $\Sigma (C_L \times V_{CC}^2 \times f_O)$ = sum of outputs

ORDERING INFORMATION

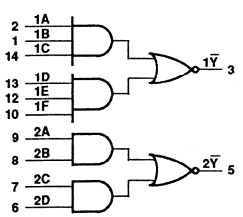
PACKAGES	TEMPERATURE RANGE	ORDER CODE
14-pin plastic DIP (300mil-wide)	-40°C to +85°C	74AC11051N 74ACT11051N
14-pin plastic SO (150mil-wide)	-40°C to +85°C	74AC11051D 74ACT11051D

PIN CONFIGURATION

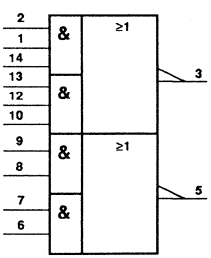
N and D Packages



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
2, 1, 14, 13, 12, 10	1A - 1F	Data inputs
9, 8, 7, 6	2A- 2D	Data inputs
3, 5	$1\overline{Y}$, $2\overline{Y}$	Data outputs
4	GND	Ground (0V)
11	V_{CC}	Positive supply voltage

FUNCTION TABLE
For 3-Input Gates

INPUTS						OUTPUT
A	B	C	D	E	F	$1\overline{Y}$
H	H	H	X	X	X	L
X	X	X	H	H	H	L
All other combinations						H

FUNCTION TABLE
For 2-Input Gates

INPUTS				OUTPUT
A	B	C	D	$2\overline{Y}$
H	H	X	X	L
X	X	H	H	L
All other combinations				H

H = High voltage level
L = Low voltage level
X = Don't care

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	74AC11051			74ACT11051			UNIT
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	DC supply voltage	3.0[1]	5.0	5.5	4.5	5.0	5.5	V
V_I	Input voltage	0		V_{CC}	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	0		V_{CC}	V
$\Delta t/\Delta v$	Input transition rise or fall rate	0		10	0		10	ns/V
T_A	Operating free-air temperature	-40		+85	-40		+85	°C

NOTE:
1. No electrical or switching characteristics are specified at V_{CC} < 3V. Operation between 2V and 3V is not recommended, but within that range, a device output will maintain a previously established logic state.

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	TEST CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 to+7.0	V
I_{IK} or V_I	DC input diode current[2]	$V_I < 0$	-20	mA
		$V_I > V_{CC}$	20	
	DC input voltage		-0.5 to V_{CC} +0.5	V
I_{OK} or V_O	DC output diode current[2]	$V_O < 0$	-50	mA
		$V_O > V_{CC}$	50	
	DC output voltage		-0.5 to V_{CC} +0.5	V
I_O	DC output source or sink current per output pin	V_O = 0 to V_{CC}	±50	mA
I_{CC} or I_{GND}	DC V_{CC} current		±100	mA
	DC ground current		±100	
T_{STG}	Storage temperature		-65 to 150	°C
P_{TOT}	Power dissipation per package Plastic DIP	Above 70°C:derate linearly by 8mW/K	500	mW
	Power dissipation per package Plastic surface mount (SO)	Above 70°C:derate linearly by 6mW/K	400	mW

NOTES:

1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		V_{CC}	74AC11051				74ACT11051				UNIT
					T_A = +25°C		T_A = -40°C to +85°C		T_A = +25°C		T_A = -40°C to +85°C		
				V	Min	Max	Min	Max	Min	Max	Min	Max	
V_{IH}	High-level input voltage			3.0	2.10		2.10						V
				4.5	3.15		3.15		2.0		2.0		
				5.5	3.85		3.85		2.0		2.0		
V_{IL}	Low-level input voltage			3.0		0.90		0.90					V
				4.5		1.35		1.35		0.8		0.8	
				5.5		1.65		1.65		0.8		0.8	
V_{OH}	High-level output voltage	V_I = V_{IL} or V_{IH}	I_{OH} = -50μA	3.0	2.9		2.9						V
				4.5	4.4		4.4		4.4		4.4		
				5.5	5.4		5.4		5.4		5.4		
			I_{OH} = -4mA	3.0	2.58		2.48						
			I_{OH} = -24mA	4.5	3.94		3.8		3.94		3.8		
				5.5	4.94		4.8		4.94		4.8		
			I_{OH} = -75mA[1]	5.5			3.85				3.85		
V_{OL}	Low-level output voltage	V_I = V_{IL} or V_{IH}	I_{OL} = 50μA	3.0		0.1		0.1					V
				4.5		0.1		0.1		0.1		0.1	
				5.5		0.1		0.1		0.1		0.1	
			I_{OL} = 12mA	3.0		0.36		0.44					
			I_{OL} = 24mA	4.5		0.36		0.44		0.36		0.44	
				5.5		0.36		0.44		0.36		0.44	
			I_{OL} = 75mA[1]	5.5				1.65				1.65	
I_I	Input leakage current	V_I = V_{CC} or GND		5.5		±0.1		±1.0		±0.1		±1.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC} or GND, I_O = 0		5.5		4.0		40		4.0		40	μA
ΔI_{CC}	Supply current, TTL inputs High[2]	One input at 3.4V, other inputs at V_{CC} or GND		5.5						0.9		1.0	mA

NOTES:
1. Not more than one output should be tested at a time, and the duration of the test should not exceed 10ms.
2. This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0V or V_{CC}.

74AC/ACT11064

4-2-3-2-Input AND-OR-INVERT Gate

Objective Specification

FEATURES

- **Output capability: ±24 mA**
- **CMOS (AC) and TTL (ACT) voltage level inputs**
- **50Ω incident wave switching**
- **Center-pin V_{CC} and ground configuration to minimize high-speed switching noise**
- **I_{CC} category: SSI**

DESCRIPTION

The 74AC/ACT11064 high-performance CMOS devices combine very high speed and high output drive comparable to the most advanced TTL families.

GENERAL INFORMATION

SYMBOL	PARAMETER	CONDITIONS T_A = 25°C; GND = 0V; V_{CC} = 5.0V	TYPICAL		UNIT
			AC	ACT	
t_{PLH}/t_{PHL}	Propagation delay A—K to $\overline{Y}$	C_L = 50pF	4.1	5.0	ns
C_{PD}	Power dissipation capacitance[1]	f = 1MHz; C_L = 50pF	38	35	pF
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	3.5	3.5	pF
I_{LATCH}	Latch-up current	Per Jedec JC40.2 Standard 17	500	500	mA

Note:

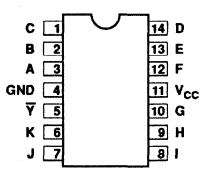
1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_I + \Sigma (C_L \times V_{CC}^2 \times f_O)$ where:
   f_I = input frequency in MHz, C_L = output load capacitance in pF,
   f_O = output frequency in MHz, V_{CC} = supply voltage in V,
   $\Sigma (C_L \times V_{CC}^2 \times f_O)$ = sum of outputs

ORDERING INFORMATION

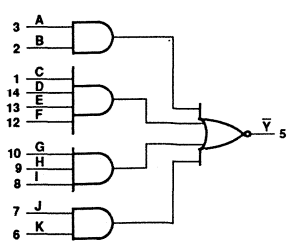
PACKAGES	TEMPERATURE RANGE	ORDER CODE
14-pin plastic DIP (300mil-wide)	-40°C to +85°C	74AC11064N 74ACT11064N
14-pin plastic SO (150mil-wide)	-40°C to +85°C	74AC11064D 74ACT11064D

PIN CONFIGURATION

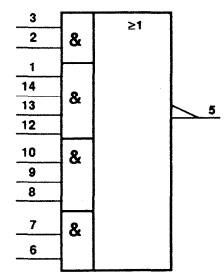
N and D Packages



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
3, 2, 1, 14, 13, 12, 10, 9, 8, 7, 6	A- K	Data inputs
5	$\overline{Y}$	Data output
4	GND	Ground (0V)
11	V_{CC}	Positive supply voltage

FUNCTION TABLE

INPUTS											OUTPUT
A	B	C	D	E	F	G	H	I	J	K	$\overline{Y}$
H	H	X	X	X	X	X	X	X	X	X	L
X	X	H	H	H	H	X	X	X	X	X	L
X	X	X	X	X	X	H	H	H	X	X	L
X	X	X	X	X	X	X	X	X	H	H	L
All other combinations											H

H = High voltage level
L = Low voltage level
N = Don't care

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	74AC11064			74ACT11064			UNIT
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	DC supply voltage	3.0[1]	5.0	5.5	4.5	5.0	5.5	V
V_I	Input voltage	0		V_{CC}	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	0		V_{CC}	V
$\Delta t/\Delta v$	Input transition rise or fall rate	0		10	0		10	ns/V
T_A	Operating free-air temperature	-40		+85	-40		+85	°C

NOTE:
1. No electrical or switching characteristics are specified at V_{CC} < 3V. Operation between 2V and 3V is not recommended, but within that range, a device output will maintain a previously established logic state.

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	TEST CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 to+7.0	V
I_{IK} or V_I	DC input diode current[2]	$V_I < 0$	-20	mA
		$V_I > V_{CC}$	20	
	DC input voltage		-0.5 to V_{CC} +0.5	V
I_{OK} or V_O	DC output diode current[2]	$V_O < 0$	-50	mA
		$V_O > V_{CC}$	50	
	DC output voltage		-0.5 to V_{CC} +0.5	V
I_O	DC output source or sink current per output pin	V_O = 0 to V_{CC}	±50	mA
I_{CC} or I_{GND}	DC V_{CC} current		±100	mA
	DC ground current		±100	
T_{STG}	Storage temperature		-65 to 150	°C
P_{TOT}	Power dissipation per package Plastic DIP	Above 70°C:derate linearly by 8mW/K	500	mW
	Power dissipation per package Plastic surface mount (SO)	Above 70°C:derate linearly by 6mW/K	400	mW

NOTES:

1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		V_{CC}	74AC11064				74ACT11064				UNIT
					T_A = +25°C		T_A = -40°C to +85°C		T_A = +25°C		T_A = -40°C to +85°C		
				V	Min	Max	Min	Max	Min	Max	Min	Max	
V_{IH}	High-level input voltage			3.0	2.10		2.10						V
				4.5	3.15		3.15		2.0		2.0		
				5.5	3.85		3.85		2.0		2.0		
V_{IL}	Low-level input voltage			3.0		0.90		0.90					V
				4.5		1.35		1.35		0.8		0.8	
				5.5		1.65		1.65		0.8		0.8	
V_{OH}	High-level output voltage	V_I = V_{IL} or V_{IH}	I_{OH} = -50μA	3.0	2.9		2.9						V
				4.5	4.4		4.4		4.4		4.4		
				5.5	5.4		5.4		5.4		5.4		
			I_{OH} = -4mA	3.0	2.58		2.48						
			I_{OH} = -24mA	4.5	3.94		3.8		3.94		3.8		
				5.5	4.94		4.8		4.94		4.8		
			I_{OH} = -75mA[1]	5.5			3.85				3.85		
V_{OL}	Low-level output voltage	V_I = V_{IL} or V_{IH}	I_{OL} = 50μA	3.0		0.1		0.1					V
				4.5		0.1		0.1		0.1		0.1	
				5.5		0.1		0.1		0.1		0.1	
			I_{OL} = 12mA	3.0		0.36		0.44					
			I_{OL} = 24mA	4.5		0.36		0.44		0.36		0.44	
				5.5		0.36		0.44		0.36		0.44	
			I_{OL} = 75mA[1]	5.5				1.65				1.65	
I_I	Input leakage current	V_I = V_{CC} or GND		5.5		±0.1		±1.0		±0.1		±1.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC} or GND, I_O = 0		5.5		4.0		40		4.0		40	μA
ΔI_{CC}	Supply current, TTL inputs High[2]	One input at 3.4V, other inputs at V_{CC} or GND		5.5						0.9		1.0	mA

NOTES:
1. Not more than one output should be tested at a time, and the duration of the test should not exceed 10ms.
2. This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0V or V_{CC}.

74AC/ACT11074

Dual D-Type Flip-Flop w/Set and Reset; Positive-Edge Trigger

Product Specification

FEATURES

- **Output capability: ±24 mA**
- **CMOS (AC) and TTL (ACT) voltage level inputs**
- **50Ω incident wave switching**
- **Center-pin V_{CC} and ground configuration to minimize high-speed switching noise**
- **I_{CC} category: SSI**

DESCRIPTION

The 74AC/ACT11074 high-performance CMOS devices combine very high speed and high output drive comparable to the most advanced TTL families.

The 74AC/ACT11074 provides two D-type flip-flops with independent Data, Clock, Set and Reset inputs, and complementary Q and $\overline{Q}$ outputs.

Set ($\overline{S}_n$) and Reset ($\overline{R}_n$) are asynchronous active-Low inputs and operate independently of the Clock input. Information on the Data (D) input is transferred to the Q output on the Low-to-High transition of the clock pulse. Clock triggering occurs at a voltage level of the clock pulse and is not directly related to the transition time of the positive-going pulse. The D inputs must be stable one set-up time prior to the Low-to-High clock transition for predictable operation.

GENERAL INFORMATION

SYMBOL	PARAMETER	CONDITIONS T_A = 25°C; GND = 0V; V_{CC} = 5.0V	TYPICAL		UNIT
			AC	ACT	
t_{PLH}/t_{PHL}	Propagation delay CP_n to Q_n or $\overline{Q}_n$	C_L = 50pF	5.2	5.9	ns
C_{PD}	Power dissipation capacitance per flip-flop[1]	f = 1MHz; C_L = 50pF	30	30	pF
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	3.5	3.5	pF
I_{LATCH}	Latch-up current	Per Jedec JC40.2 Standard 17	500	500	mA
f_{MAX}	Maximum clock frequency	C_L = 50pF	150	125	MHz

Note:

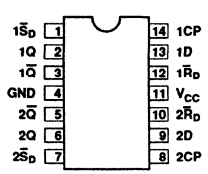
1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_I + \Sigma (C_L \times V_{CC}^2 \times f_O)$ where:
   f_I = input frequency in MHz, C_L = output load capacitance in pF,
   f_O = output frequency in MHz, V_{CC} = supply voltage in V,
   $\Sigma (C_L \times V_{CC}^2 \times f_O)$ = sum of outputs

ORDERING INFORMATION

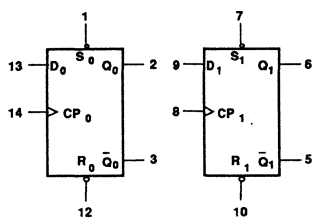
PACKAGES	TEMPERATURE RANGE	ORDER CODE
14-pin plastic DIP (300mil-wide)	-40°C to +85°C	74AC11074N 74ACT11074N
14-pin plastic SO (150mil-wide)	-40°C to +85°C	74AC11074D 74ACT11074D

PIN CONFIGURATION

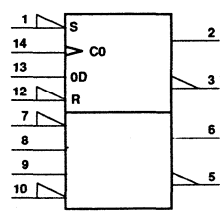
N and D Packages



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
13, 9	D_0 - D_1	Data inputs
2, 6	Q_0 - Q_1	Data outputs
3, 5	$\overline{Q}_0$ - $\overline{Q}_1$	Data outputs (complements of Q_n outputs)
1, 7	$\overline{S}_0$ - $\overline{S}_1$	Set inputs (active Low)
12, 10	$\overline{R}_0$ - $\overline{R}_1$	Reset inputs (active Low)
14, 8	CP_0 - CP_1	Clock inputs
4	GND	Ground (0V)
11	V_{CC}	Positive supply voltage

FUNCTION TABLE

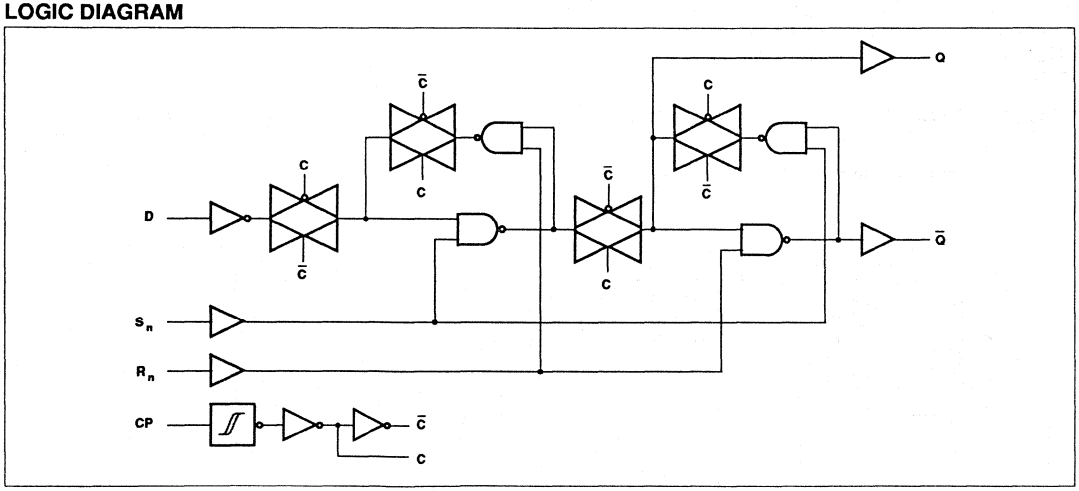
OPERATING MODE	INPUTS				OUTPUTS	
	$\overline{S}$	$\overline{R}$	CP	D	Q	$\overline{Q}$
Asynchronous set	L	H	X	X	H	L
Asynchronous reset	H	L	X	X	L	H
Undetermined[1]	L	L	X	X	H	H
Load "1" (set)	H	H	↑	h	H	L
Load "0" (reset)	H	H	↑	l	L	H
No change – hold	H	H	L	X	Q_0	$\overline{Q}_0$

H = High voltage level steady state
h = High voltage level one set-up time prior to the Low-to-High clock transition
L = Low voltage level steady state
l = Low voltage level one set-up time prior to the Low-to-High clock transition
X = Don't care
↑ = Low-to-High clock transition

NOTE:

1. This configuration is nonstable; that is, it will not persist when either Set or Reset returns to its inactive (High) level.

LOGIC DIAGRAM



RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	74AC11074			74ACT11074			UNIT
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	DC supply voltage	3.0[1]	5.0	5.5	4.5	5.0	5.5	V
V_I	Input voltage	0		V_{CC}	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	0		V_{CC}	V
$\Delta t/\Delta v$	Input transition rise or fall rate	0		10	0		10	ns/V
T_A	Operating free-air temperature	-40		+85	-40		+85	°C

NOTE:

1. No electrical or switching characteristics are specified at $V_{CC} < 3V$. Operation between 2V and 3V is not recommended, but within that range, a device output will maintain a previously established logic state.

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	TEST CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 to+7.0	V
I_{IK} or V_I	DC input diode current[2]	$V_I < 0$	-20	mA
		$V_I > V_{CC}$	20	
	DC input voltage		-0.5 to V_{CC} +0.5	V
I_{OK} or V_O	DC output diode current[2]	$V_O < 0$	-50	mA
		$V_O > V_{CC}$	50	
	DC output voltage		-0.5 to V_{CC} +0.5	V
I_O	DC output source or sink current per output pin	V_O = 0 to V_{CC}	±50	mA
I_{CC} or I_{GND}	DC V_{CC} current		±100	mA
	DC ground current		±100	
T_{STG}	Storage temperature		-65 to 150	°C
P_{TOT}	Power dissipation per package Plastic DIP	Above 70°C:derate linearly by 8mW/K	500	mW
	Power dissipation per package Plastic surface mount (SO)	Above 70°C:derate linearly by 6mW/K	400	mW

NOTES:

1. *Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.*
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		V_{CC}	74AC11074				74ACT11074				UNIT
					T_A = +25°C		T_A = -40°C to +85°C		T_A = +25°C		T_A = -40°C to +85°C		
				V	Min	Max	Min	Max	Min	Max	Min	Max	
V_{IH}	High-level input voltage			3.0	2.10		2.10						V
				4.5	3.15		3.15		2.0		2.0		
				5.5	3.85		3.85		2.0		2.0		
V_{IL}	Low-level input voltage			3.0		0.90		0.90					V
				4.5		1.35		1.35		0.8		0.8	
				5.5		1.65		1.65		0.8		0.8	
V_{OH}	High-level output voltage	V_I = V_{IL} or V_{IH}	I_{OH} = -50μA	3.0	2.9		2.9						V
				4.5	4.4		4.4		4.4		4.4		
				5.5	5.4		5.4		5.4		5.4		
			I_{OH} = -4mA	3.0	2.58		2.48						
			I_{OH} = -24mA	4.5	3.94		3.8		3.94		3.8		
				5.5	4.94		4.8		4.94		4.8		
			I_{OH} = -75mA[1]	5.5			3.85				3.85		
V_{OL}	Low-level output voltage	V_I = V_{IL} or V_{IH}	I_{OL} = 50μA	3.0		0.1		0.1					V
				4.5		0.1		0.1		0.1		0.1	
				5.5		0.1		0.1		0.1		0.1	
			I_{OL} = 12mA	3.0		0.36		0.44					
			I_{OL} = 24mA	4.5		0.36		0.44		0.36		0.44	
				5.5		0.36		0.44		0.36		0.44	
			I_{OL} = 75mA[1]	5.5				1.65				1.65	
I_I	Input leakage current	V_I = V_{CC} or GND		5.5		±0.1		±1.0		±0.1		±1.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC} or GND, I_O = 0		5.5		4.0		40		4.0		40	μA
ΔI_{CC}	Supply current, TTL inputs High[2]	One input at 3.4V, other inputs at V_{CC} or GND		5.5						0.9		1.0	mA

NOTES:
1. Not more than one output should be tested at a time, and the duration of the test should not exceed 10ms.
2. This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0V or V_{CC}.

AC ELECTRICAL CHARACTERISTICS AT 3.3V ±0.3V

SYMBOL	PARAMETER	WAVEFORM	74AC11074					UNIT
			T_A = +25°C			T_A = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	1	100	125		100		MHz
t_{PLH} t_{PHL}	Propagation delay CP_n to Q_n, $\overline{Q}_n$	1	1.5 1.5	7.7 7.3	10.5 9.7	1.5 1.5	11.3 10.6	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{S}_n$, $\overline{R}_n$ to Q_n, $\overline{Q}_n$	2	1.5 1.5	5.8 6.5	9.3 11.4	1.5 1.5	10.0 12.2	ns
t_S	Setup time, High or Low D_n to CP_n	1	5.0			5.0		ns
t_H	Hold time, High or Low CP_n to D_n	1	0			0		ns
t_W	Clock pulse width High or Low	1	5.0			5.0		ns
t_W	$\overline{S}_n$ or $\overline{R}_n$ pulse width, Low	2	4.0			4.0		ns
t_{REC}	Recovery time $\overline{S}_n$ or $\overline{R}_n$ to CP_n	3	1.0			1.0		ns

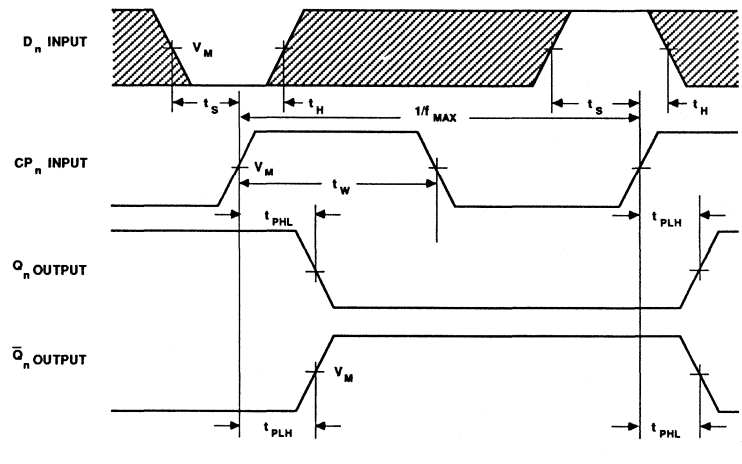
AC ELECTRICAL CHARACTERISTICS AT 5.0V ±0.5V

SYMBOL	PARAMETER	WAVEFORM	74AC11074					UNIT
			T_A = +25°C			T_A = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	1	125	150		125		MHz
t_{PLH} t_{PHL}	Propagation delay CP_n to Q_n, $\overline{Q}_n$	1	1.5 1.5	5.4 5.0	7.5 6.9	1.5 1.5	8.2 7.5	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{S}_n$, $\overline{R}_n$ to Q_n, $\overline{Q}_n$	2	1.5 1.5	4.2 4.7	6.6 8.2	1.5 1.5	7.1 9.0	ns
t_S	Setup time, High or Low D_n to CP_n	1	3.5			3.5		ns
t_H	Hold time, High or Low CP_n to D_n	1	0			0		ns
t_W	Clock pulse width High or Low	1	4.0			4.0		ns
t_W	$\overline{S}_n$ or $\overline{R}_n$ pulse width, Low	2	4.0			4.0		ns
t_{REC}	Recovery time $\overline{S}_n$ or $\overline{R}_n$ to CP_n	3	1.0			1.0		ns

AC ELECTRICAL CHARACTERISTICS AT 5.0V ±0.5V

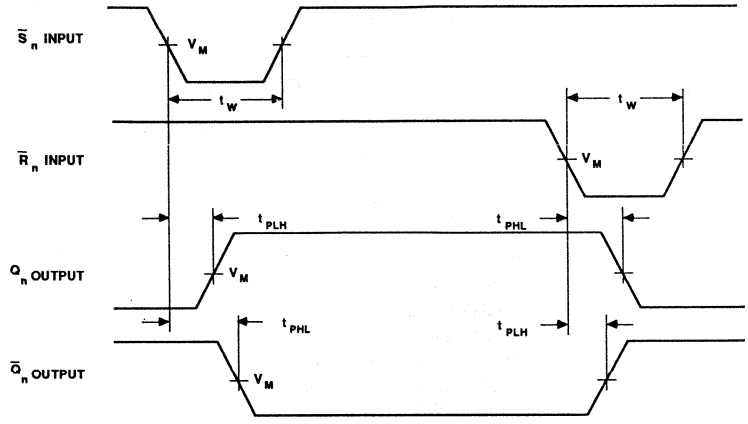
SYMBOL	PARAMETER	WAVEFORM	74ACT11074					UNIT
			T_A = +25°C			T_A = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	1	100	125		100		MHz
t_{PLH} t_{PHL}	Propagation delay CP_n to Q_n, $\overline{Q}_n$	1	1.5 1.5	6.0 5.7	8.5 8.0	1.5 1.5	9.4 8.8	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{S}_n$, $\overline{R}_n$ to Q_n, $\overline{Q}_n$	2	1.5 1.5	5.7 6.6	8.9 11.3	1.5 1.5	9.6 12.5	ns
t_S	Setup time, High or Low D_n to CP_n	1	4.5			4.5		ns
t_H	Hold time, High or Low CP_n to D_n	1	0			0		ns
t_W	Clock pulse width High or Low	1	5.0			5.0		ns
t_W	$\overline{S}_n$ or $\overline{R}_n$ pulse width, Low	2	5.0			5.0		ns
t_{REC}	Recovery time $\overline{S}_n$ or $\overline{R}_n$ to CP_n	3	2.0			2.0		ns

AC WAVEFORMS

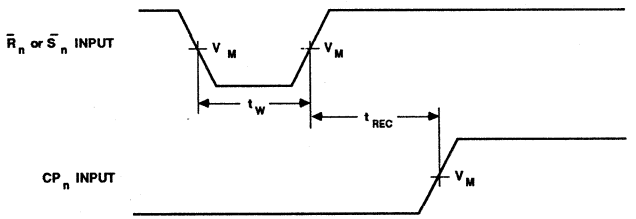


Waveform 1. Waveforms Showing Clock to Output Delays, Data Setup, and Clock Pulse Width

AC WAVEFORMS (Continued)



Waveform 2. Waveforms Showing Set and Reset to Output Delays, Set and Reset Pulse Widths

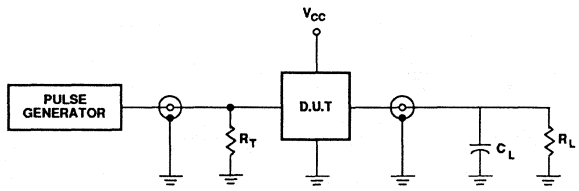


Waveform 3. Waveforms Showing Recovery Time

WAVEFORM CONDITIONS

	INPUTS	OUTPUTS
AC	V_{IN} = GND to V_{CC}, V_M = 50% V_{CC}	V_{OUT} = V_{OL} to V_{OH}
ACT	V_{IN} = GND to 3.0V, V_M = 1.5V	V_M = 50% V_{CC}

TEST CIRCUIT



Test Circuit

DEFINITIONS

C_L = Load capacitance, 50pF; includes jig and probe capacitance

R_L = Load resistor, 500Ω

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators

Input pulses: PRR ≤ 10MHz

$t_r = t_f$ = 3ns

74AC/ACT11086

Quad 2-Input Exclusive-OR Gate

Product Specification

FEATURES

- **Output capability: ±24 mA**
- **CMOS (AC) and TTL (ACT) voltage level inputs**
- **50Ω incident wave switching**
- **Center-pin V_{CC} and ground configuration to minimize high-speed switching noise**
- **I_{CC} category: SSI**

DESCRIPTION

The 74AC/ACT11086 high-performance CMOS devices combine very high speed and high output drive comparable to the most advanced TTL families.

The 74AC/ACT11086 provides four separate 2-input exclusive-OR gate functions.

GENERAL INFORMATION

SYMBOL	PARAMETER	CONDITIONS T_A = 25°C; GND = 0V; V_{CC} = 5.0V	TYPICAL		UNIT
			AC	ACT	
t_{PLH}/t_{PHL}	Propagation delay A, B, to Y	C_L = 50pF	3.8	5.1	ns
C_{PD}	Power dissipation capacitance per gate[1]	f = 1MHz; C_L = 50pF	27	26	pF
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	3.5	3.5	pF
I_{LATCH}	Latch-up current	Per Jedec JC40.2 Standard 17	500	500	mA

Note:

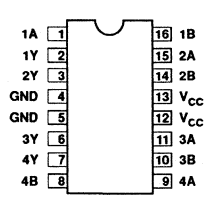
1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_I + \Sigma (C_L \times V_{CC}^2 \times f_O)$ where:
   f_I = input frequency in MHz, C_L = output load capacitance in pF,
   f_O = output frequency in MHz, V_{CC} = supply voltage in V,
   $\Sigma (C_L \times V_{CC}^2 \times f_O)$ = sum of outputs

ORDERING INFORMATION

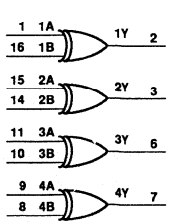
PACKAGES	TEMPERATURE RANGE	ORDER CODE
16-pin plastic DIP (300mil-wide)	-40°C to +85°C	74AC11086N 74ACT11086N
16-pin plastic SO (150mil-wide)	-40°C to +85°C	74AC11086D 74ACT11086D

PIN CONFIGURATION

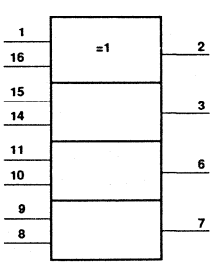
N and D Packages



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
1, 15, 11, 9	1A - 4A	Data inputs
16, 14, 10, 8	1B - 4B	Data inputs
2, 3, 6, 7	1Y - 4Y	Data outputs
4, 5	GND	Ground (0V)
12, 13	V_{CC}	Positive supply voltage

FUNCTION TABLE

INPUTS		OUTPUT
nA	nB	nY
L	L	L
L	H	H
H	L	H
H	H	L

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	74AC11086			74ACT11086			UNIT
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	DC supply voltage	3.0[1]	5.0	5.5	4.5	5.0	5.5	V
V_I	Input voltage	0		V_{CC}	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	0		V_{CC}	V
$\Delta t/\Delta v$	Input transition rise or fall rate	0		10	0		10	ns/V
T_A	Operating free-air temperature	-40		+85	-40		+85	°C

NOTE:

1. No electrical or switching characteristics are specified at V_{CC} < 3V. Operation between 2V and 3V is not recommended, but within that range, a device output will maintain a previously established logic state.

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	TEST CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 to+7.0	V
I_{IK} or V_I	DC input diode current[2]	$V_I < 0$	-20	mA
		$V_I > V_{CC}$	20	
	DC input voltage		-0.5 to V_{CC} +0.5	V
I_{OK} or V_O	DC output diode current[2]	$V_O < 0$	-50	mA
		$V_O > V_{CC}$	50	
	DC output voltage		-0.5 to V_{CC} +0.5	V
I_O	DC output source or sink current per output pin	V_O = 0 to V_{CC}	±50	mA
I_{CC} or I_{GND}	DC V_{CC} current		±100	mA
	DC ground current		±100	
T_{STG}	Storage temperature		-65 to 150	°C
P_{TOT}	Power dissipation per package Plastic DIP	Above 70°C:derate linearly by 8mW/K	500	mW
	Power dissipation per package Plastic surface mount (SO)	Above 70°C:derate linearly by 6mW/K	400	mW

NOTES:

1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		V_{CC}	74AC11086				74ACT11086				UNIT
					T_A = +25°C		T_A = -40°C to +85°C		T_A = +25°C		T_A = -40°C to +85°C		
				V	Min	Max	Min	Max	Min	Max	Min	Max	
V_{IH}	High-level input voltage			3.0	2.10		2.10						V
				4.5	3.15		3.15		2.0		2.0		
				5.5	3.85		3.85		2.0		2.0		
V_{IL}	Low-level input voltage			3.0		0.90		0.90					V
				4.5		1.35		1.35		0.8		0.8	
				5.5		1.65		1.65		0.8		0.8	
V_{OH}	High-level output voltage	V_I = V_{IL} or V_{IH}	I_{OH} = -50μA	3.0	2.9		2.9						V
				4.5	4.4		4.4		4.4		4.4		
				5.5	5.4		5.4		5.4		5.4		
			I_{OH} = -4mA	3.0	2.58		2.48						
			I_{OH} = -24mA	4.5	3.94		3.8		3.94		3.8		
				5.5	4.94		4.8		4.94		4.8		
			I_{OH} = -75mA[1]	5.5			3.85				3.85		
V_{OL}	Low-level output voltage	V_I = V_{IL} or V_{IH}	I_{OL} = 50μA	3.0		0.1		0.1					V
				4.5		0.1		0.1		0.1		0.1	
				5.5		0.1		0.1		0.1		0.1	
			I_{OL} = 12mA	3.0		0.36		0.44					
			I_{OL} = 24mA	4.5		0.36		0.44		0.36		0.44	
				5.5		0.36		0.44		0.36		0.44	
			I_{OL} = 75mA[1]	5.5				1.65				1.65	
I_I	Input leakage current	V_I = V_{CC} or GND		5.5		±0.1		±1.0		±0.1		±1.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC} or GND, I_O = 0		5.5		4.0		40		4.0		40	μA
ΔI_{CC}	Supply current, TTL inputs High[2]	One input at 3.4V, other inputs at V_{CC} or GND		5.5						0.9		1.0	mA

NOTES:
1. Not more than one output should be tested at a time, and the duration of the test should not exceed 10ms.
2. This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0V or V_{CC}.

AC ELECTRICAL CHARACTERISTICS AT 3.3V ±0.3V

SYMBOL	PARAMETER	WAVEFORM	74AC11086					UNIT
			T_A = +25°C			T_A = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay nA, nB to nY	1	1.5 1.5	5.6 5.1	9.4 7.4	1.5 1.5	10.6 8.2	ns

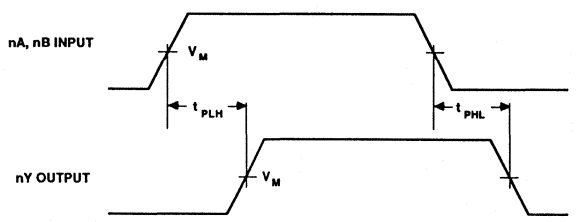
AC ELECTRICAL CHARACTERISTICS AT 5.0V ±0.5V

SYMBOL	PARAMETER	WAVEFORM	74AC11086					UNIT
			T_A = +25°C			T_A = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay nA, nB to nY	1	1.5 1.5	3.8 3.8	6.8 6.2	1.5 1.5	7.6 6.8	ns

AC ELECTRICAL CHARACTERISTICS AT 5.0V ±0.5V

SYMBOL	PARAMETER	WAVEFORM	74ACT11086					UNIT
			T_A = +25°C			T_A = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay nA, nB to nY	1	1.5 1.5	5.1 5.1	8.7 8.0	1.5 1.5	9.6 9.0	ns

AC WAVEFORMS

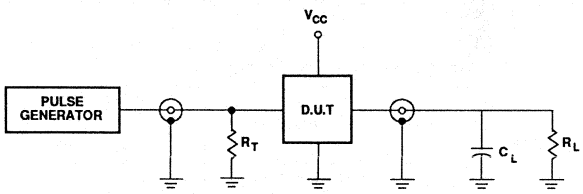


Waveform 1. Waveforms Showing the Input (nA, nB) to Output (nY) Propagation Delays

WAVEFORM CONDITIONS

	INPUTS	OUTPUTS
AC	V_{IN} = GND to V_{CC}, V_M = 50% V_{CC}	V_{OUT} = V_{OL} to V_{OH}
ACT	V_{IN} = GND to 3.0V, V_M = 1.5V	V_M = 50% V_{CC}

TEST CIRCUIT



Test Circuit

DEFINITIONS

C_L = Load capacitance, 50pF; includes jig and probe capacitance

R_L = Load resistor, 500Ω

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators

Input pulses: PRR ≤ 10MHz

$t_r = t_f = 3ns$

74AC/ACT11109

Dual J-$\overline{K}$ Flip-Flop with Set and Reset; Positive Edge-Triggered

Product Specification

FEATURES

- **Output capability: ±24 mA**
- **CMOS (AC) and TTL (ACT) voltage level inputs**
- **50Ω incident wave switching**
- **Center-pin V_{CC} and ground configuration to minimize high-speed switching noise**
- **I_{CC} category: SSI**

DESCRIPTION

The 74AC/ACT11109 high-performance CMOS devices combine very high speed and high output drive comparable to the most advanced TTL families.

The 74AC/ACT11109 provides two J-$\overline{K}$ flip-flops with independent Data, Clock, Set and Reset inputs, and complementary Q and $\overline{Q}$ outputs.

Set ($\overline{S}_n$) and Reset ($\overline{R}_n$) are asynchronous active-Low inputs and operate independently of the Clock input.

Information at the J and $\overline{K}$ inputs is transferred to the Q output on the Low-to-High transition of the clock pulse. Clock triggering occurs at a voltage level of the clock pulse and is not directly related to the transition time of the positive-going pulse. The J and $\overline{K}$ inputs must be stable one set-up time prior to the Low-to-High clock transition for predictable operation. The J and K inputs may be tied together to allow operation as a D flip-flop.

GENERAL INFORMATION

SYMBOL	PARAMETER	CONDITIONS T_A = 25°C; GND = 0V; V_{CC} = 5.0V	TYPICAL		UNIT
			AC	ACT	
t_{PLH}/ t_{PHL}	Propagation delay CP_n to Q_n or $\overline{Q}_n$	C_L = 50pF	5.3	5.8	ns
C_{PD}	Power dissipation capacitance per flip-flop[1]	f = 1MHz; C_L = 50pF	32	31	pF
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	3.5	3.5	pF
I_{LATCH}	Latch-up current	Per Jedec JC40.2 Standard 17	500	500	mA
f_{MAX}	Maximum clock frequency	C_L = 50pF	125	125	MHz

Note:

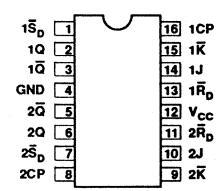
1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_I + \Sigma (C_L \times V_{CC}^2 \times f_O)$ where:
   f_I = input frequency in MHz, C_L = output load capacitance in pF,
   f_O = output frequency in MHz, V_{CC} = supply voltage in V,
   $\Sigma (C_L \times V_{CC}^2 \times f_O)$ = sum of outputs

ORDERING INFORMATION

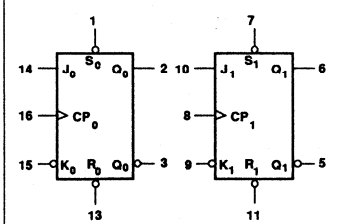
PACKAGES	TEMPERATURE RANGE	ORDER CODE
16-pin plastic DIP (300mil-wide)	-40°C to +85°C	74AC11109N 74ACT11109N
16-pin plastic SO (150mil-wide)	-40°C to +85°C	74AC11109D 74ACT11109D

PIN CONFIGURATION

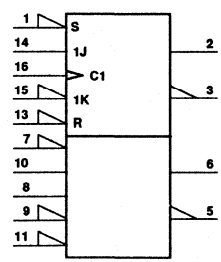
N and D Packages



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



Dual J-$\overline{K}$ Flip-Flop with Set and Reset; Positive Edge-Triggered

74AC/ACT11109

PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
14, 10	J_0 - J_1	Data inputs
15, 9	$\overline{K}_0$ - $\overline{K}_1$	Data inputs
2, 6	Q_0 - Q_1	Data outputs
3, 5	$\overline{Q}_0$ - $\overline{Q}_1$	Data outputs (complements of Q_n outputs)
1, 7	$\overline{S}_0$ - $\overline{S}_1$	Set inputs (active Low)
13, 11	$\overline{R}_0$ - $\overline{R}_1$	Reset inputs (active Low)
16, 8	CP_0 - CP_1	Clock inputs
4	GND	Ground (0V)
12	V_{CC}	Positive supply voltage

FUNCTION TABLE

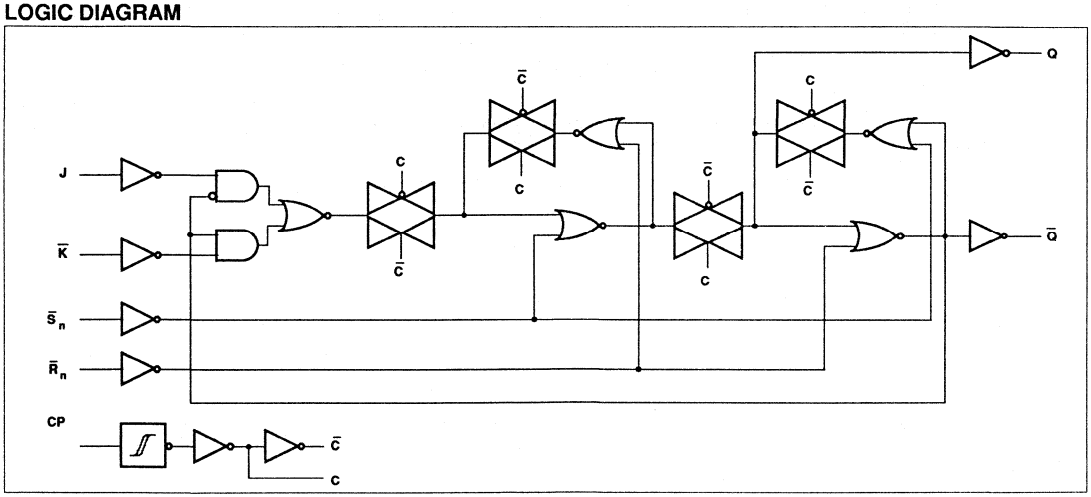
OPERATING MODE	INPUTS					OUTPUTS	
	$\overline{S}$	$\overline{R}$	CP	J	$\overline{K}$	Q	$\overline{Q}$
Asynchronous set	L	H	X	X	X	H	L
Asynchronous reset (clear)	H	L	X	X	X	L	H
Undetermined[1]	L	L	X	X	X	H	H
Load "0" (reset)	H	H	↑	l	l	L	H
Load "1" (set)	H	H	↑	h	h	H	L
Toggle	H	H	↑	h	l	$\overline{q}$	q
No change – hold	H	H	L	X	X	Q_0	$\overline{Q}_0$

H = High voltage level steady state
h = High voltage level one set-up time prior to the Low-to-High clock transition
L = Low voltage level steady state
l = Low voltage level one set-up time prior to the Low-to-High clock transition
X = Don't care
q = Lower case letters indicate the state of the referenced output prior to the Low-to-High clock transition
↑ = Low-to-High clock transition

NOTE:

1. This configuration is nonstable; that is, it will not persist when either Set or Reset returns to its inactive (High) level.

LOGIC DIAGRAM



RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	74AC11109			74ACT11109			UNIT
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	DC supply voltage	3.0[1]	5.0	5.5	4.5	5.0	5.5	V
V_I	Input voltage	0		V_{CC}	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	0		V_{CC}	V
$\Delta t/\Delta v$	Input transition rise or fall rate	0		10	0		10	ns/V
T_A	Operating free-air temperature	-40		+85	-40		+85	°C

NOTE:

1. No electrical or switching characteristics are specified at V_{CC} < 3V. Operation between 2V and 3V is not recommended, but within that range, a device output will maintain a previously established logic state.

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	TEST CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 to+7.0	V
I_{IK} or V_I	DC input diode current[2]	$V_I < 0$	-20	mA
		$V_I > V_{CC}$	20	
	DC input voltage		-0.5 to V_{CC} +0.5	V
I_{OK} or V_O	DC output diode current[2]	$V_O < 0$	-50	mA
		$V_O > V_{CC}$	50	
	DC output voltage		-0.5 to V_{CC} +0.5	V
I_O	DC output source or sink current per output pin	V_O = 0 to V_{CC}	±50	mA
I_{CC} or I_{GND}	DC V_{CC} current		±100	mA
	DC ground current		±100	
T_{STG}	Storage temperature		-65 to 150	°C
P_{TOT}	Power dissipation per package Plastic DIP	Above 70°C:derate linearly by 8mW/K	500	mW
	Power dissipation per package	Above 70°C:derate linearly by 6mW/K	400	mW

NOTES:

1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		V_{CC}	74AC11109				74ACT11109				UNIT
					T_A = +25°C		T_A = -40°C to +85°C		T_A = +25°C		T_A = -40°C to +85°C		
				V	Min	Max	Min	Max	Min	Max	Min	Max	
V_{IH}	High-level input voltage			3.0	2.10		2.10						V
				4.5	3.15		3.15		2.0		2.0		
				5.5	3.85		3.85		2.0		2.0		
V_{IL}	Low-level input voltage			3.0		0.90		0.90					V
				4.5		1.35		1.35		0.8		0.8	
				5.5		1.65		1.65		0.8		0.8	
V_{OH}	High-level output voltage	V_I = V_{IL} or V_{IH}	I_{OH} = -50μA	3.0	2.9		2.9						V
				4.5	4.4		4.4		4.4		4.4		
				5.5	5.4		5.4		5.4		5.4		
			I_{OH} = -4mA	3.0	2.58		2.48						
			I_{OH} = -24mA	4.5	3.94		3.8		3.94		3.8		
				5.5	4.94		4.8		4.94		4.8		
			I_{OH} = -75mA[1]	5.5			3.85				3.85		
V_{OL}	Low-level output voltage	V_I = V_{IL} or V_{IH}	I_{OL} = 50μA	3.0		0.1		0.1					V
				4.5		0.1		0.1		0.1		0.1	
				5.5		0.1		0.1		0.1		0.1	
			I_{OL} = 12mA	3.0		0.36		0.44					
			I_{OL} = 24mA	4.5		0.36		0.44		0.36		0.44	
				5.5		0.36		0.44		0.36		0.44	
			I_{OL} = 75mA[1]	5.5				1.65				1.65	
I_I	Input leakage current	V_I = V_{CC} or GND		5.5		±0.1		±1.0		±0.1		±1.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC} or GND, I_O = 0		5.5		4.0		40		4.0		40	μA
ΔI_{CC}	Supply current, TTL inputs High[2]	One input at 3.4V, other inputs at V_{CC} or GND		5.5						0.9		1.0	mA

NOTES:
1. Not more than one output should be tested at a time, and the duration of the test should not exceed 10ms.
2. This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0V or V_{CC}.

AC ELECTRICAL CHARACTERISTICS AT 3.3V ±0.3V

SYMBOL	PARAMETER	WAVEFORM	74AC11109					UNIT
			T_A = +25°C			T_A = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	1	70	100		70		MHz
t_{PLH} t_{PHL}	Propagation delay CP_n to Q_n, $\overline{Q}_n$	1	1.5 1.5	8.0 7.5	11.4 10.5	1.5 1.5	12.7 11.8	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{S}_n$, $\overline{R}_n$ to Q_n, $\overline{Q}_n$	2	1.5 1.5	6.5 8.0	9.0 12.6	1.5 1.5	9.9 13.7	ns
t_S	Setup time, High or Low J_n or $\overline{K}_n$ to CP_n	1	5.5			5.5		ns
t_H	Hold time, High or Low CP_n to J_n or $\overline{K}_n$	1	0			0		ns
t_W	Clock pulse width High or Low	1	7.2			7.2		ns
t_W	$\overline{S}_n$ or $\overline{R}_n$ pulse width, Low	2	5.0			5.0		ns
t_{REC}	Recovery time $\overline{S}_n$ or $\overline{R}_n$ to CP_n	3	2.5			2.5		ns

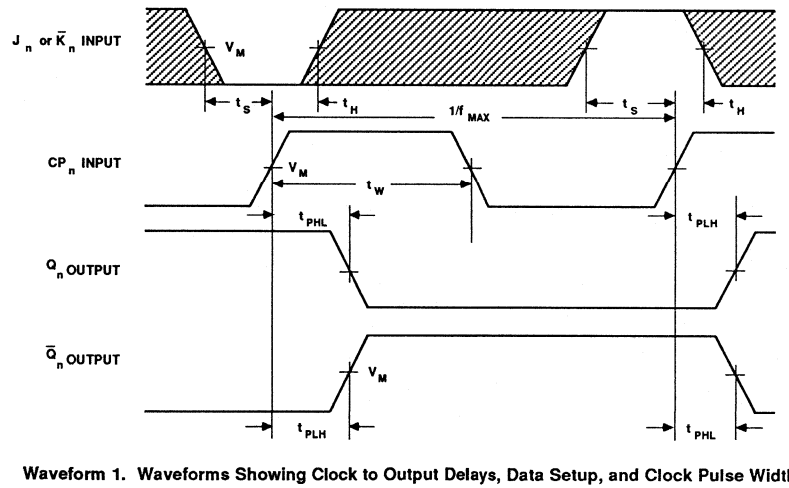
AC ELECTRICAL CHARACTERISTICS AT 5.0V ±0.5V

SYMBOL	PARAMETER	WAVEFORM	74AC11109					UNIT
			T_A = +25°C			T_A = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	1	100	125		100		MHz
t_{PLH} t_{PHL}	Propagation delay CP_n to Q_n, $\overline{Q}_n$	1	1.5 1.5	5.5 5.0	7.9 7.3	1.5 1.5	8.8 8.1	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{S}_n$, $\overline{R}_n$ to Q_n, $\overline{Q}_n$	2	1.5 1.5	4.5 5.0	6.5 8.6	1.5 1.5	7.1 9.6	ns
t_S	Setup time, High or Low J_n or $\overline{K}_n$ to CP_n	1	4.5			4.5		ns
t_H	Hold time, High or Low CP_n to J_n or $\overline{K}_n$	1	0			0		ns
t_W	Clock pulse width High or Low	1	5.0			5.0		ns
t_W	$\overline{S}_n$ or $\overline{R}_n$ pulse width, Low	2	4.0			4.0		ns
t_{REC}	Recovery time $\overline{S}_n$ or $\overline{R}_n$ to CP_n	3	2.0			2.0		ns

AC ELECTRICAL CHARACTERISTICS AT 5.0V ±0.5V

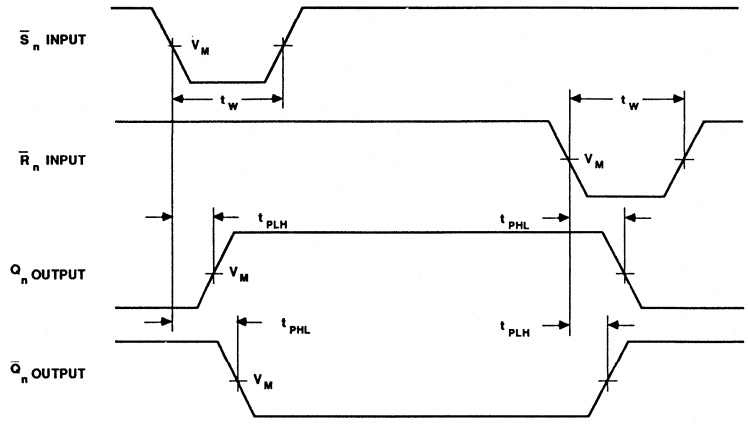
SYMBOL	PARAMETER	WAVEFORM	74ACT11109					UNIT
			T_A = +25°C			T_A = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	1	100	125		100		MHz
t_{PLH} t_{PHL}	Propagation delay CP_n to Q_n, $\overline{Q}_n$	1	1.5 1.5	6.0 5.5	8.3 7.6	1.5 1.5	9.1 8.3	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{S}_n$, $\overline{R}_n$ to Q_n, $\overline{Q}_n$	2	1.5 1.5	5.5 6.0	8.6 10.8	1.5 1.5	9.2 11.8	ns
t_S	Setup time, High or Low J_n or $\overline{K}_n$ to CP_n	1	5.5			5.5		ns
t_H	Hold time, High or Low CP_n to J_n or $\overline{K}_n$	1	0			0		ns
t_W	Clock pulse width High or Low	1	5.0			5.0		ns
t_W	$\overline{S}_n$ or $\overline{R}_n$ pulse width, Low	2	5.5			5.5		ns
t_{REC}	Recovery time $\overline{S}_n$ or $\overline{R}_n$ to CP_n	3	2.0			2.0		ns

AC WAVEFORMS

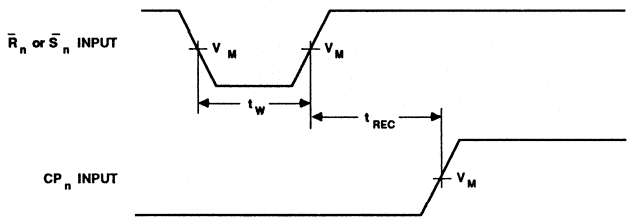


Waveform 1. Waveforms Showing Clock to Output Delays, Data Setup, and Clock Pulse Width

AC WAVEFORMS (Continued)



Waveform 2. Waveforms Showing Set and Reset to Output Delays, Set and Reset Pulse Widths

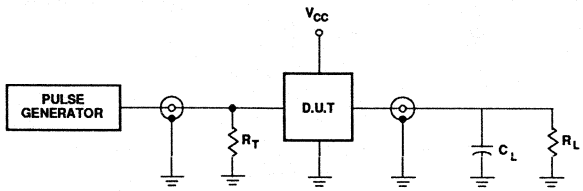


Waveform 3. Waveforms Showing Recovery Time

WAVEFORM CONDITIONS

	INPUTS	OUTPUTS
AC	V_{IN} = GND to V_{CC}, V_M = 50% V_{CC}	V_{OUT} = V_{OL} to V_{OH}
ACT	V_{IN} = GND to 3.0V, V_M = 1.5V	V_M = 50% V_{CC}

TEST CIRCUIT



Test Circuit

DEFINITIONS

C_L = Load capacitance, 50pF; includes jig and probe capacitance

R_L = Load resistor, 500Ω

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators

Input pulses: PRR ≤ 10MHz

$t_r = t_f = 3ns$

74AC/ACT11112

Dual J-K Flip-Flop with Set and Reset; Negative Edge-Triggered

Product Specification

FEATURES

- **Output capability: ±24 mA**
- **CMOS (AC) and TTL (ACT) voltage level inputs**
- **50Ω incident wave switching**
- **Center-pin V_{CC} and ground configuration to minimize high-speed switching noise**
- **I_{CC} category: SSI**

DESCRIPTION

The 74AC/ACT11112 high-performance CMOS devices combine very high speed and high output drive comparable to the most advanced TTL families.

The 74AC/ACT11112 provides two J-K flip-flops with independent Data, Clock, Set and Reset inputs, and complementary nQ and $n\overline{Q}$ outputs.

Set ($n\overline{S}_D$) and Reset ($n\overline{R}_D$) are asynchronous active-Low inputs and operate independently of the Clock inputs.

Information at the J and K inputs is transferred to the outputs on the High-to-Low transition of the clock pulse. The J and K inputs must be stable one set-up time prior to the High-to-Low clock transition for predictable operation.

GENERAL INFORMATION

SYMBOL	PARAMETER	CONDITIONS T_A = 25°C; GND = 0V; V_{CC} = 5.0V	TYPICAL		UNIT
			AC	ACT	
t_{PLH}/ t_{PHL}	Propagation delay $n\overline{CP}$ to nQ or $n\overline{Q}$	C_L = 50pF	3.8	4.5	ns
C_{PD}	Power dissipation capacitance per flip-flop[1]	f = 1MHz; C_L = 50pF	37	39	pF
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	3.5	3.5	pF
I_{LATCH}	Latch-up current	Per Jedec JC40.2 Standard 17	500	500	mA
f_{MAX}	Maximum clock frequency	C_L = 50pF	175	175	MHz

Note:

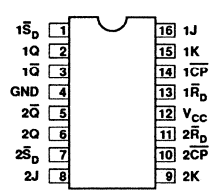
1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_I + \Sigma (C_L \times V_{CC}^2 \times f_O)$ where:
   f_I = input frequency in MHz, C_L = output load capacitance in pF,
   f_O = output frequency in MHz, V_{CC} = supply voltage in V,
   $\Sigma (C_L \times V_{CC}^2 \times f_O)$ = sum of outputs

ORDERING INFORMATION

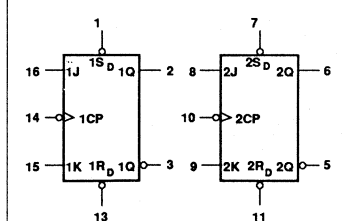
PACKAGES	TEMPERATURE RANGE	ORDER CODE
16-pin plastic DIP (300mil-wide)	-40°C to +85°C	74AC11112N 74ACT11112N
16-pin plastic SO (150mil-wide)	-40°C to +85°C	74AC11112D 74ACT11112D

PIN CONFIGURATION

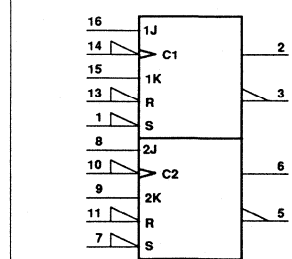
N and D Packages



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
16, 8	1J - 2J	Data inputs
15, 9	1K - 2K	Data inputs
2, 6	1Q - 2Q	Data outputs
3, 5	$\overline{1Q}$ - $\overline{2Q}$	Data outputs (complements of Q_n outputs)
1, 7	$1\overline{S}_D$ - $2\overline{S}_D$	Set inputs (active Low)
13, 11	$1\overline{R}_D$ - $2\overline{R}_D$	Reset inputs (active Low)
14, 10	$1\overline{CP}$ - $2\overline{CP}$	Clock inputs
4	GND	Ground (0V)
12	V_{CC}	Positive supply voltage

FUNCTION TABLE

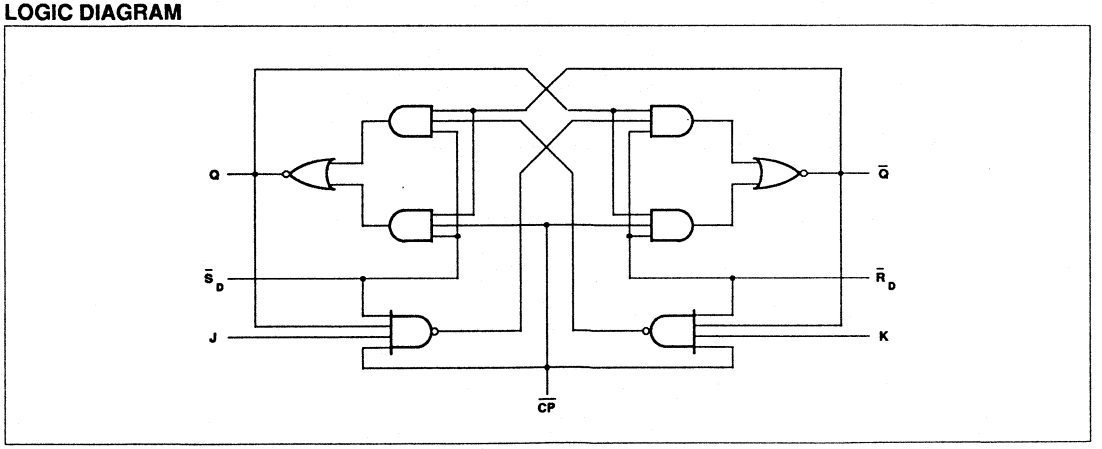
OPERATING MODE	INPUTS					OUTPUTS	
	$\overline{S}_D$	$\overline{R}_D$	$\overline{CP}$	J	K	Q	$\overline{Q}$
Asynchronous set	L	H	X	X	X	H	L
Asynchronous reset (clear)	H	L	X	X	X	L	H
Undetermined[1]	L	L	X	X	X	H	H
Toggle	H	H	↓	h	h	$\overline{q}$	q
Load "0" (reset)	H	H	↓	l	h	L	H
Load "1" (set)	H	H	↓	h	l	H	L
No change – hold	H	H	↓	l	l	q	$\overline{q}$
No change – hold	H	H	H	X	X	Q	$\overline{Q}$

H = High voltage level steady state
h = High voltage level one set-up time prior to the High-to-Low clock transition
L = Low voltage level steady state
l = Low voltage level one set-up time prior to the High-to-Low clock transition
X = Don't care
q = Lower case letters indicate the state of the referenced output prior to the High-to-Low clock transition
↓ = High-to-Low clock transition

NOTE:

1. This configuration is nonstable; that is, it will not persist when either Set or Reset returns to its inactive (High) level.

LOGIC DIAGRAM



RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	74AC11112			74ACT11112			UNIT
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	DC supply voltage	3.0[1]	5.0	5.5	4.5	5.0	5.5	V
V_I	Input voltage	0		V_{CC}	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	0		V_{CC}	V
$\Delta t/\Delta v$	Input transition rise or fall rate	0		10	0		10	ns/V
T_A	Operating free-air temperature	-40		+85	-40		+85	°C

NOTE:

1. No electrical or switching characteristics are specified at V_{CC} < 3V. Operation between 2V and 3V is not recommended, but within that range, a device output will maintain a previously established logic state.

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	TEST CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 to+7.0	V
I_{IK} or V_I	DC input diode current[2]	$V_I < 0$	-20	mA
		$V_I > V_{CC}$	20	
	DC input voltage		-0.5 to V_{CC} +0.5	V
I_{OK} or V_O	DC output diode current[2]	$V_O < 0$	-50	mA
		$V_O > V_{CC}$	50	
	DC output voltage		-0.5 to V_{CC} +0.5	V
I_O	DC output source or sink current per output pin	V_O = 0 to V_{CC}	±50	mA
I_{CC} or I_{GND}	DC V_{CC} current		±100	mA
	DC ground current		±100	
T_{STG}	Storage temperature		-65 to 150	°C
P_{TOT}	Power dissipation per package Plastic DIP	Above 70°C:derate linearly by 8mW/K	500	mW
	Power dissipation per package	Above 70°C:derate linearly by 6mW/K	400	mW

NOTES:

1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		V_{CC}	74AC11112				74ACT11112				UNIT
					T_A = +25°C		T_A = -40°C to +85°C		T_A = +25°C		T_A = -40°C to +85°C		
				V	Min	Max	Min	Max	Min	Max	Min	Max	
V_{IH}	High-level input voltage			3.0	2.10		2.10						V
				4.5	3.15		3.15		2.0		2.0		
				5.5	3.85		3.85		2.0		2.0		
V_{IL}	Low-level input voltage			3.0		0.90		0.90					V
				4.5		1.35		1.35		0.8		0.8	
				5.5		1.65		1.65		0.8		0.8	
V_{OH}	High-level output voltage	V_I = V_{IL} or V_{IH}	I_{OH} = -50μA	3.0	2.9		2.9						V
				4.5	4.4		4.4		4.4		4.4		
				5.5	5.4		5.4		5.4		5.4		
			I_{OH} = -4mA	3.0	2.58		2.48						
			I_{OH} = -24mA	4.5	3.94		3.8		3.94		3.8		
				5.5	4.94		4.8		4.94		4.8		
			I_{OH} = -75mA[1]	5.5			3.85				3.85		
V_{OL}	Low-level output voltage	V_I = V_{IL} or V_{IH}	I_{OL} = 50μA	3.0		0.1		0.1					V
				4.5		0.1		0.1		0.1		0.1	
				5.5		0.1		0.1		0.1		0.1	
			I_{OL} = 12mA	3.0		0.36		0.44					
			I_{OL} = 24mA	4.5		0.36		0.44		0.36		0.44	
				5.5		0.36		0.44		0.36		0.44	
			I_{OL} = 75mA[1]	5.5				1.65				1.65	
I_I	Input leakage current	V_I = V_{CC} or GND		5.5		±0.1		±1.0		±0.1		±1.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC} or GND, I_O = 0		5.5		4.0		40		4.0		40	μA
ΔI_{CC}	Supply current, TTL inputs High[2]	One input at 3.4V, other inputs at V_{CC} or GND		5.5						0.9		1.0	mA

NOTES:
1. Not more than one output should be tested at a time, and the duration of the test should not exceed 10ms.
2. This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0V or V_{CC}.

AC ELECTRICAL CHARACTERISTICS AT 3.3V ±0.3V

SYMBOL	PARAMETER	WAVEFORM	74AC11112					UNIT
			T_A = +25°C			T_A = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	1	100	150		100		MHz
t_{PLH} t_{PHL}	Propagation delay $n\overline{CP}$ to nQ , $n\overline{Q}$	1	1.5 1.5	5.4 6.0	7.1 7.9	1.5 1.5	7.6 8.5	ns
t_{PLH} t_{PHL}	Propagation delay $n\overline{S}_D$, $n\overline{R}_D$ to nQ , $n\overline{Q}$	2	1.5 1.5	4.9 7.0	6.7 9.2	1.5 1.5	7.3 9.9	ns
t_S	Setup time, High or Low nJ or nK to $n\overline{CP}$	1	5.0			5.0		ns
t_H	Hold time, High or Low $n\overline{CP}$ to nJ or nK	1	0.5			0.5		ns
t_W	Clock pulse width High or Low	1	5.0			5.0		ns
t_W	$n\overline{S}_D$ or $n\overline{R}_D$ pulse width, Low	2	4.0			4.0		ns
t_{REC}	Recovery time $n\overline{S}_D$ or $n\overline{R}_D$ to $n\overline{CP}$	3	2.5			2.5		ns

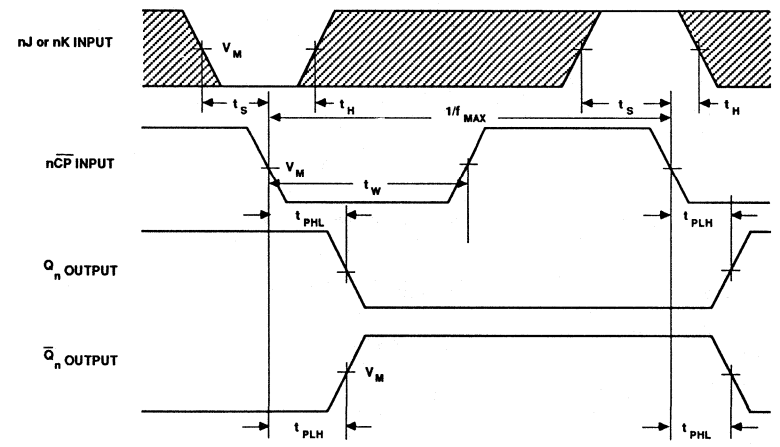
AC ELECTRICAL CHARACTERISTICS AT 5.0V ±0.5V

SYMBOL	PARAMETER	WAVEFORM	74AC11112					UNIT
			T_A = +25°C			T_A = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	1	125	175		125		MHz
t_{PLH} t_{PHL}	Propagation delay $n\overline{CP}$ to nQ , $n\overline{Q}$	1	1.5 1.5	3.4 4.2	5.1 6.3	1.5 1.5	5.6 7.0	ns
t_{PLH} t_{PHL}	Propagation delay $n\overline{S}_D$, $n\overline{R}_D$ to nQ , $n\overline{Q}$	2	1.5 1.5	3.3 4.6	5.1 6.7	1.5 1.5	5.4 7.3	ns
t_S	Setup time, High or Low nJ or nK to $n\overline{CP}$	1	3.5			3.5		ns
t_H	Hold time, High or Low $n\overline{CP}$ to nJ or nK	1	1.0			1.0		ns
t_W	Clock pulse width High or Low	1	4.0			4.0		ns
t_W	$n\overline{S}_D$ or $n\overline{R}_D$ pulse width, Low	2	3.0			3.0		ns
t_{REC}	Recovery time $n\overline{S}_D$ or $n\overline{R}_D$ to $n\overline{CP}$	3	2.0			2.0		ns

AC ELECTRICAL CHARACTERISTICS AT 5.0V ±0.5V

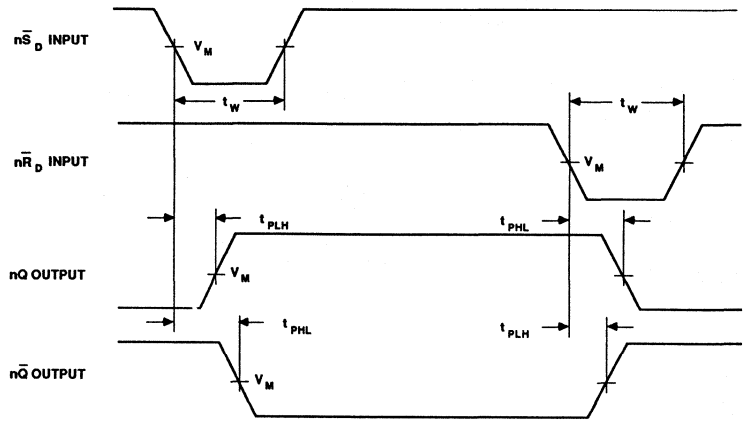
SYMBOL	PARAMETER	WAVEFORM	74ACT11112					UNIT
			T_A = +25°C			T_A = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	1	125	175		125		MHz
t_{PLH} t_{PHL}	Propagation delay $n\overline{CP}$ to nQ , $n\overline{Q}$	1	1.5 1.5	4.2 4.7	7.0 7.4	1.5 1.5	7.7 8.4	ns
t_{PLH} t_{PHL}	Propagation delay $n\overline{S}_D$, $n\overline{R}_D$ to nQ , $n\overline{Q}$	2	1.5 1.5	3.6 4.6	6.3 7.4	1.5 1.5	6.8 8.0	ns
t_S	Setup time, High or Low nJ or nK to $n\overline{CP}$	1	3.5			3.5		ns
t_H	Hold time, High or Low $n\overline{CP}$ to nJ or nK	1	1.5			1.5		ns
t_W	Clock pulse width High or Low	1	4.0			4.0		ns
t_W	$n\overline{S}_D$ or $n\overline{R}_D$ pulse width, Low	2	4.0			4.0		ns
t_{REC}	Recovery time $n\overline{S}_D$ or $n\overline{R}_D$ to $n\overline{CP}$	3	2.0			2.0		ns

AC WAVEFORMS

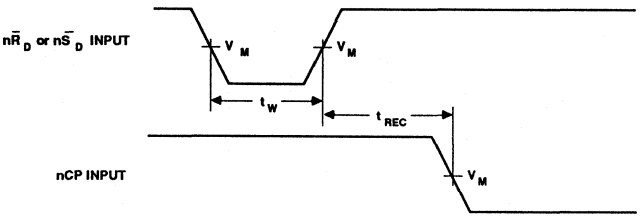


Waveform 1. Waveforms Showing Clock to Output Delays, Data Setup, and Clock Pulse Width

AC WAVEFORMS (Continued)



Waveform 2. Waveforms Showing Set and Reset to Output Delays, Set and Reset Pulse Widths

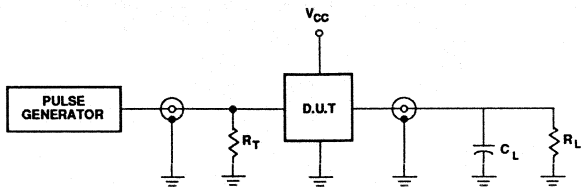


Waveform 3. Waveforms Showing Recovery Time

WAVEFORM CONDITIONS

	INPUTS	OUTPUTS
AC	V_{IN} = GND to V_{CC}, V_M = 50% V_{CC}	V_{OUT} = V_{OL} to V_{OH}
ACT	V_{IN} = GND to 3.0V, V_M = 1.5V	V_M = 50% V_{CC}

TEST CIRCUIT



Test Circuit

DEFINITIONS

C_L = Load capacitance, 50pF; includes jig and probe capacitance

R_L = Load resistor, 500Ω

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators

Input pulses: PRR ≤ 10MHz

$t_r = t_f$ = 3ns

74AC/ACT11132

Quad 2-Input NAND Schmitt-Trigger

AC11132: Preliminary Specification
ACT11132: Objective Specification

FEATURES

- **Output capability: ±24 mA**
- **CMOS (AC) and TTL (ACT) voltage level inputs**
- **50Ω incident wave switching**
- **Center-pin V_{CC} and ground configuration to minimize high-speed switching noise**
- **I_{CC} category: SSI**

DESCRIPTION

The 74AC/ACT11132 high-performance CMOS devices combine very high speed and high output drive comparable to the most advanced TTL families.

The 74AC/ACT11132 provides four separate 2-input NAND gate functions which are capable of transforming slowly changing input signals into sharply defined, jitter-free output signals. In addition, they have greater noise margin than conventional NAND gates.

GENERAL INFORMATION

SYMBOL	PARAMETER	CONDITIONS T_A = 25°C; GND = 0V; V_{CC} = 5.0V	TYPICAL		UNIT
			AC	ACT	
t_{PLH}/t_{PHL}	Propagation delay A, B, to $\overline{Y}$	C_L = 50pF	5.2	7.9	ns
C_{PD}	Power dissipation capacitance per gate[1]	f = 1MHz; C_L = 50pF	27	30	pF
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	3.5	3.5	pF
I_{LATCH}	Latch-up current	Per Jedec JC40.2 Standard 17	500	500	mA

Note:

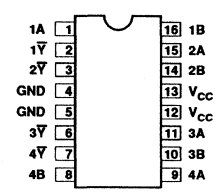
1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_I + \Sigma (C_L \times V_{CC}^2 \times f_O)$ where:
   f_I = input frequency in MHz, C_L = output load capacitance in pF,
   f_O = output frequency in MHz, V_{CC} = supply voltage in V,
   $\Sigma (C_L \times V_{CC}^2 \times f_O)$ = sum of outputs

ORDERING INFORMATION

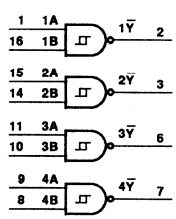
PACKAGES	TEMPERATURE RANGE	ORDER CODE
16-pin plastic DIP (300mil-wide)	-40°C to +85°C	74AC11132N 74ACT11132N
16-pin plastic SO (150mil-wide)	-40°C to +85°C	74AC11132D 74ACT11132D

PIN CONFIGURATION

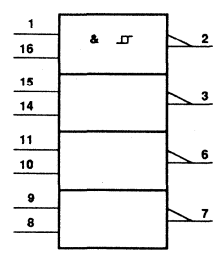
N and D Packages



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
1, 15, 11, 9	1A - 4A	Data inputs
16, 14, 10, 8	1B - 4B	Data inputs
2, 3, 6, 7	$1\overline{Y}$ - $4\overline{Y}$	Data outputs
4, 5	GND	Ground (0V)
12, 13	V_{CC}	Positive supply voltage

FUNCTION TABLE

INPUTS		OUTPUT
nA	nB	$n\overline{Y}$
L	L	H
L	H	H
H	L	H
H	H	L

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	74AC11132			74ACT11132			UNIT
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	DC supply voltage	3.0[1]	5.0	5.5	4.5	5.0	5.5	V
V_I	Input voltage	0		V_{CC}	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	0		V_{CC}	V
$\Delta t/\Delta v$	Input transition rise or fall rate	0		100	0		100	ns/V
T_A	Operating free-air temperature	-40		+85	-40		+85	°C

NOTE:

1. No electrical or switching characteristics are specified at $V_{CC} < 3V$. Operation between 2V and 3V is not recommended, but within that range, a device output will maintain a previously established logic state.

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	TEST CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 to+7.0	V
I_{IK} or V_I	DC input diode current[2]	$V_I < 0$	-20	mA
		$V_I > V_{CC}$	20	
	DC input voltage		-0.5 to V_{CC} +0.5	V
I_{OK} or V_O	DC output diode current[2]	$V_O < 0$	-50	mA
		$V_O > V_{CC}$	50	
	DC output voltage		-0.5 to V_{CC} +0.5	V
I_O	DC output source or sink current per output pin	V_O = 0 to V_{CC}	±50	mA
I_{CC} or I_{GND}	DC V_{CC} current		±100	mA
	DC ground current		±100	
T_{STG}	Storage temperature		-65 to 150	°C
P_{TOT}	Power dissipation per package Plastic DIP	Above 70°C:derate linearly by 8mW/K	500	mW
	Power dissipation per package Plastic surface mount (SO)	Above 70°C:derate linearly by 6mW/K	400	mW

NOTES:

1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		V_{CC}	74AC11132				74ACT11132				UNIT
					T_A = +25°C		T_A = -40°C to +85°C		T_A = +25°C		T_A = -40°C to +85°C		
				V	Min	Max	Min	Max	Min	Max	Min	Max	
V_{T+}	Positive-going threshold			3.0		2.2		2.2					V
				4.5		3.2		3.2		2.0		2.0	
				5.5		3.9		3.9		2.0		2.0	
V_{T-}	Negative-going threshold			3.0	0.5		0.5						V
				4.5	0.9		0.9			0.8		0.8	
				5.5	1.1		1.1			0.8		0.8	
ΔV_T	Hysteresis ($V_{T+} - V_{T-}$)			3.0	0.3	1.2	0.3	1.2					V
				4.5	0.4	1.4	0.4	1.4	0.4	1.2	0.4	1.2	
				5.5	0.5	1.6	0.5	1.6	0.4	1.2	0.4	1.2	
V_{IH}	High-level input voltage			3.0	2.10		2.10						V
				4.5	3.15		3.15		2.0		2.0		
				5.5	3.85		3.85		2.0		2.0		
V_{IL}	Low-level input voltage			3.0		0.90		0.90					V
				4.5		1.35		1.35		0.8		0.8	
				5.5		1.65		1.65		0.8		0.8	
V_{OH}	High-level output voltage	V_I = V_{IL} or V_{IH}	I_{OH} = -50μA	3.0	2.9		2.9						V
				4.5	4.4		4.4		4.4		4.4		
				5.5	5.4		5.4		5.4		5.4		
			I_{OH} = -4mA	3.0	2.58		2.48						
			I_{OH} = -24mA	4.5	3.94		3.8		3.94		3.8		
				5.5	4.94		4.8		4.94		4.8		
			I_{OH} = -75mA[1]	5.5			3.85				3.85		
V_{OL}	Low-level output voltage	V_I = V_{IL} or V_{IH}	I_{OL} = 50μA	3.0		0.1		0.1					V
				4.5		0.1		0.1		0.1		0.1	
				5.5		0.1		0.1		0.1		0.1	
			I_{OL} = 12mA	3.0		0.36		0.44					
			I_{OL} = 24mA	4.5		0.36		0.44		0.36		0.44	
				5.5		0.36		0.44		0.36		0.44	
			I_{OL} = 75mA[1]	5.5				1.65				1.65	
I_I	Input leakage current	V_I = V_{CC} or GND		5.5		±0.1		±1.0		±0.1		±1.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC} or GND, I_O = 0		5.5		4.0		40		4.0		40	μA
ΔI_{CC}	Supply current, TTL inputs High[2]	One input at 3.4V, other inputs at V_{CC} or GND		5.5						0.9		1.0	mA

NOTES:

1. Not more than one output should be tested at a time, and the duration of the test should not exceed 10ms.
2. This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0V or V_{CC}.

AC ELECTRICAL CHARACTERISTICS AT 3.3V ±0.3V

SYMBOL	PARAMETER	WAVEFORM	74AC11132					UNIT
			T_A = +25°C			T_A = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay nA, nB to n$\overline{Y}$	1	1.5 1.5	6.9 7.6	9.0 9.5	1.5 1.5	9.7 10.4	ns

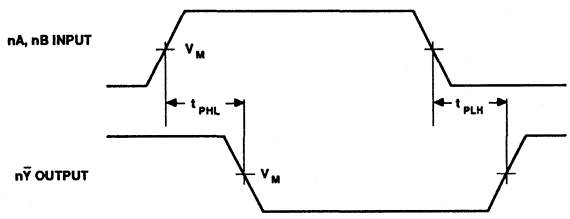
AC ELECTRICAL CHARACTERISTICS AT 5.0V ±0.5V

SYMBOL	PARAMETER	WAVEFORM	74AC11132					UNIT
			T_A = +25°C			T_A = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay nA, nB to n$\overline{Y}$	1	1.5 1.5	4.9 5.4	6.6 7.0	1.5 1.5	7.1 7.6	ns

AC ELECTRICAL CHARACTERISTICS AT 5.0V ±0.5V

SYMBOL	PARAMETER	WAVEFORM	74ACT11132					UNIT
			T_A = +25°C			T_A = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay nA, nB to n$\overline{Y}$	1	1.5 1.5			1.5 1.5		ns

AC WAVEFORMS

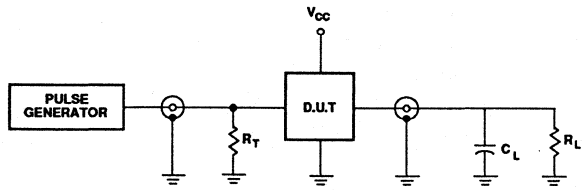


Waveform 1. Waveforms Showing the Input (nA, nB) to Output (n$\overline{Y}$) Propagation Delays

WAVEFORM CONDITIONS

	INPUTS	OUTPUTS
AC	V_{IN} = GND to V_{CC}, V_M = 50% V_{CC}	V_{OUT} = V_{OL} to V_{OH}
ACT	V_{IN} = GND to 3.0V, V_M = 1.5V	V_M = 50% V_{CC}

TEST CIRCUIT



Test Circuit

DEFINITIONS

C_L = Load capacitance, 50pF; includes jig and probe capacitance

R_L = Load resistor, 500Ω

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators

Input pulses: PRR ≤ 10MHz

$t_r = t_f$ = 3ns

74AC/ACT11138

3-to-8 Line Decoder/ Demultiplexer; Active-Low

Product Specification

FEATURES

- **Demultiplexing capability**
- **Multiple input enable for easy expansion**
- **Ideal for memory chip select decoding**
- **Inverting outputs**
- **Output capability: ±24 mA**
- **CMOS (AC) and TTL (ACT) voltage level inputs**
- **50Ω incident wave switching**
- **Center-pin V_{CC} and ground configuration to minimize high-speed switching noise**
- **I_{CC} category: MSI**

DESCRIPTION

The 74AC/ACT11138 high-performance CMOS devices combine very high speed and high output drive comparable to the most advanced TTL families.

The 74AC/ACT11138 decoders accept three binary weighted inputs (A_0, A_1, A_2) and when enabled, provide eight mutually exclusive, active-Low outputs ($\overline{Y}_0$ - $\overline{Y}_7$). The devices feature three enable inputs; two active-Low ($\overline{E}_1$, $\overline{E}_2$) and one active-High (E_3). Every output will be High unless $\overline{E}_1$ and $\overline{E}_2$ are Low and E_3 is High. This multiple enable function allows easy parallel expansion of the devices to a 1-of-32 (5 lines to 32 lines) decoder with just four '11138's and one inverter.

The devices can be used as eight output demultiplexers by using one of the active-Low enable inputs as the data input and the remaining enable inputs as strobes.

GENERAL INFORMATION

SYMBOL	PARAMETER	CONDITIONS T_A = 25°C; GND = 0V; V_{CC} = 5.0V	TYPICAL		UNIT
			AC	ACT	
t_{PLH}/ t_{PHL}	Propagation delay A_n to $\overline{Y}_n$	C_L = 50pF	6.0	6.1	ns
C_{PD}	Power dissipation capacitance[1]	f = 1MHz; C_L = 50pF	56	61	pF
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	3.5	3.5	pF
I_{LATCH}	Latch-up current	Per Jedec JC40.2 Standard 17	500	500	mA

Note:

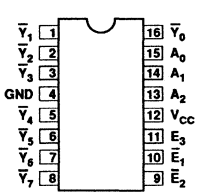
1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_I + \Sigma (C_L \times V_{CC}^2 \times f_O)$ where:
   f_I = input frequency in MHz, C_L = output load capacitance in pF,
   f_O = output frequency in MHz, V_{CC} = supply voltage in V,
   $\Sigma (C_L \times V_{CC}^2 \times f_O)$ = sum of outputs

ORDERING INFORMATION

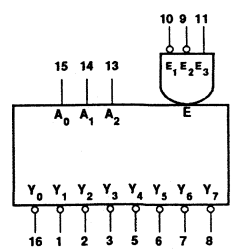
PACKAGES	TEMPERATURE RANGE	ORDER CODE
16-pin plastic DIP (300mil-wide)	-40°C to +85°C	74AC11138N 74ACT11138N
16-pin plastic SO (150mil-wide)	-40°C to +85°C	74AC11138D 74ACT11138D

PIN CONFIGURATION

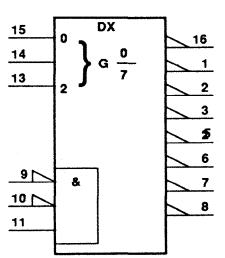
N and D Packages



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



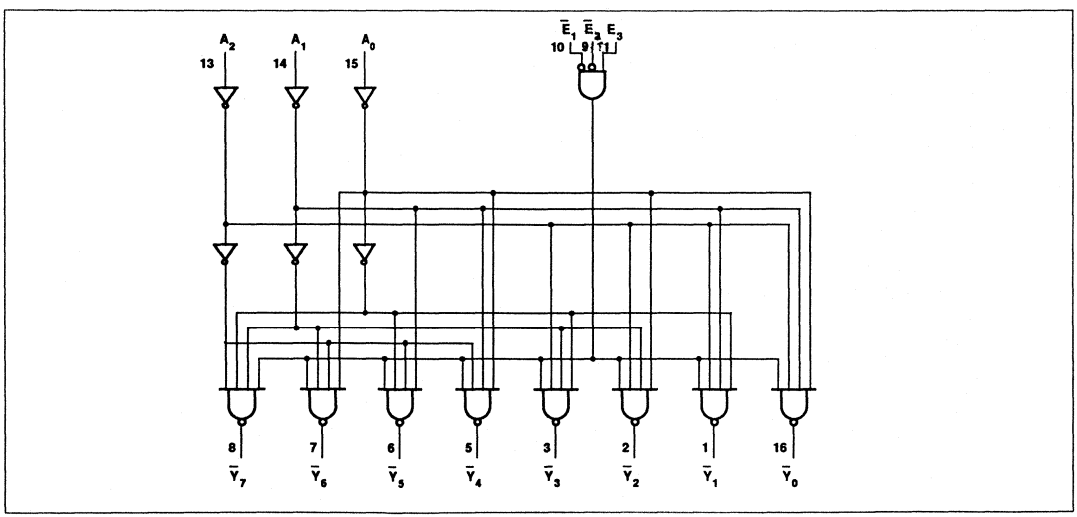
PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
15, 14, 13	A_0 to A_2	Address inputs
10, 9	$\overline{E}_1$, $\overline{E}_2$	Enable inputs (active Low)
11	E_3	Enable input (active High)
16, 8, 7, 6, 5, 3, 2, 1	$\overline{Y}_0$ to $\overline{Y}_7$	Outputs
4	GND	Ground (0V)
12	V_{CC}	Positive supply voltage

FUNCTION TABLE

INPUTS						OUTPUTS							
$\overline{E}_1$	$\overline{E}_2$	E_3	A_0	A_1	A_2	$\overline{Y}_0$	$\overline{Y}_1$	$\overline{Y}_2$	$\overline{Y}_3$	$\overline{Y}_4$	$\overline{Y}_5$	$\overline{Y}_6$	$\overline{Y}_7$
H	X	X	X	X	X	H	H	H	H	H	H	H	H
X	H	X	X	X	X	H	H	H	H	H	H	H	H
X	X	L	X	X	X	H	H	H	H	H	H	H	H
L	L	H	L	L	L	L	H	H	H	H	H	H	H
L	L	H	H	L	L	H	L	H	H	H	H	H	H
L	L	H	L	H	L	H	H	L	H	H	H	H	H
L	L	H	H	H	L	H	H	H	L	H	H	H	H
L	L	H	L	L	H	H	H	H	H	L	H	H	H
L	L	H	H	L	H	H	H	H	H	H	L	H	H
L	L	H	L	H	H	H	H	H	H	H	H	L	H
L	L	H	H	H	H	H	H	H	H	H	H	H	L

LOGIC DIAGRAM



RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	74AC11138			74ACT11138			UNIT
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	DC supply voltage	3.0[1]	5.0	5.5	4.5	5.0	5.5	V
V_I	Input voltage	0		V_{CC}	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	0		V_{CC}	V
$\Delta t/\Delta v$	Input transition rise or fall rate	0		10	0		10	ns/V
T_A	Operating free-air temperature	-40		+85	-40		+85	°C

NOTE:
1. No electrical or switching characteristics are specified at V_{CC} < 3V. Operation between 2V and 3V is not recommended, but within that range, a device output will maintain a previously established logic state.

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	TEST CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 to+7.0	V
I_{IK} or V_I	DC input diode current[2]	$V_I < 0$	-20	mA
		$V_I > V_{CC}$	20	
	DC input voltage		-0.5 to V_{CC} +0.5	V
I_{OK} or V_O	DC output diode current[2]	$V_O < 0$	-50	mA
		$V_O > V_{CC}$	50	
	DC output voltage		-0.5 to V_{CC} +0.5	V
I_O	DC output source or sink current per output pin	V_O = 0 to V_{CC}	±50	mA
I_{CC} or I_{GND}	DC V_{CC} current		±200	mA
	DC ground current		±200	
T_{STG}	Storage temperature		-65 to 150	°C
P_{TOT}	Power dissipation per package Plastic DIP	Above 70°C:derate linearly by 8mW/K	500	mW
	Power dissipation per package Plastic surface mount (SO)	Above 70°C:derate linearly by 6mW/K	400	mW

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		V_{CC}	74AC11138				74ACT11138				UNIT
					T_A = +25°C		T_A = -40°C to +85°C		T_A = +25°C		T_A = -40°C to +85°C		
				V	Min	Max	Min	Max	Min	Max	Min	Max	
V_{IH}	High-level input voltage			3.0	2.10		2.10						V
				4.5	3.15		3.15		2.0		2.0		
				5.5	3.85		3.85		2.0		2.0		
V_{IL}	Low-level input voltage			3.0		0.90		0.90					V
				4.5		1.35		1.35		0.8		0.8	
				5.5		1.65		1.65		0.8		0.8	
V_{OH}	High-level output voltage	V_I = V_{IL} or V_{IH}	I_{OH} = -50μA	3.0	2.9		2.9						V
				4.5	4.4		4.4		4.4		4.4		
				5.5	5.4		5.4		5.4		5.4		
			I_{OH} = -4mA	3.0	2.58		2.48						
			I_{OH} = -24mA	4.5	3.94		3.8		3.94		3.8		
				5.5	4.94		4.8		4.94		4.8		
			I_{OH} = -75mA[1]	5.5			3.85				3.85		
V_{OL}	Low-level output voltage	V_I = V_{IL} or V_{IH}	I_{OL} = 50μA	3.0		0.1		0.1					V
				4.5		0.1		0.1		0.1		0.1	
				5.5		0.1		0.1		0.1		0.1	
			I_{OL} = 12mA	3.0		0.36		0.44					
			I_{OL} = 24mA	4.5		0.36		0.44		0.36		0.44	
				5.5		0.36		0.44		0.36		0.44	
			I_{OL} = 75mA[1]	5.5				1.65				1.65	
I_I	Input leakage current	V_I = V_{CC} or GND		5.5		±0.1		±1.0		±0.1		±1.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC} or GND, I_O = 0		5.5		8.0		80		8.0		80	μA
ΔI_{CC}	Supply current, TTL inputs High[2]	One input at 3.4V, other inputs at V_{CC} or GND		5.5						0.9		1.0	mA

NOTES:
1. Not more than one output should be tested at a time, and the duration of the test should not exceed 10ms.
2. This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0V or V_{CC}.

AC ELECTRICAL CHARACTERISTICS AT 3.3V ±0.3V

SYMBOL	PARAMETER	WAVEFORM	74AC11138					UNIT
			T_A = +25°C			T_A = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay A_n to $\overline{Y}_n$	1	1.5 1.5	8.3 8.9	10.2 10.9	1.5 1.5	11.4 12.2	ns
t_{PLH} t_{PHL}	Propagation delay E_3 to $\overline{Y}_n$	2	1.5 1.5	7.2 7.3	9.2 9.4	1.5 1.5	10.2 10.5	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{E}_n$ to $\overline{Y}_n$	2	1.5 1.5	8.2 8.3	10.4 10.4	1.5 1.5	11.5 11.6	ns

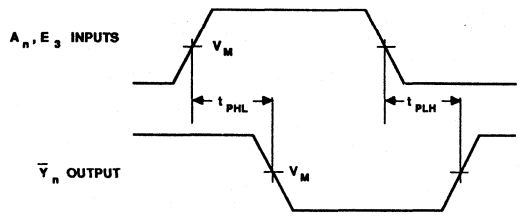
AC ELECTRICAL CHARACTERISTICS AT 5.0V ±0.5V

SYMBOL	PARAMETER	WAVEFORM	74AC11138					UNIT
			T_A = +25°C			T_A = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay A_n to $\overline{Y}_n$	1	1.5 1.5	5.7 6.2	7.3 7.9	1.5 1.5	8.1 8.8	ns
t_{PLH} t_{PHL}	Propagation delay E_3 to $\overline{Y}_n$	2	1.5 1.5	5.1 5.2	6.9 6.9	1.5 1.5	7.5 7.7	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{E}_n$ to $\overline{Y}_n$	2	1.5 1.5	5.8 5.6	7.6 7.5	1.5 1.5	8.3 8.3	ns

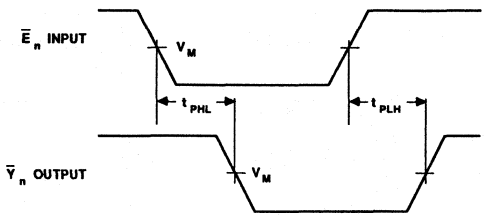
AC ELECTRICAL CHARACTERISTICS AT 5.0V ±0.5V

SYMBOL	PARAMETER	WAVEFORM	74ACT11138					UNIT
			T_A = +25°C			T_A = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay A_n to $\overline{Y}_n$	1	1.5 1.5	6.1 6.0	8.9 8.7	1.5 1.5	9.8 9.7	ns
t_{PLH} t_{PHL}	Propagation delay E_3 to $\overline{Y}_n$	2	1.5 1.5	5.5 6.0	8.0 7.9	1.5 1.5	8.9 8.9	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{E}_n$ to $\overline{Y}_n$	2	1.5 1.5	6.4 6.0	8.3 8.8	1.5 1.5	9.3 9.8	ns

AC WAVEFORMS



Waveform 1. Waveforms Showing the Inputs (A_n, E_3) to Output ($\overline{Y}_n$) Propagation Delays

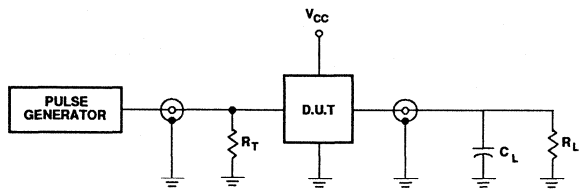


Waveform 2. Waveforms Showing the Input ($\overline{E}_n$) to Output ($\overline{Y}_n$) Propagation Delays

WAVEFORM CONDITIONS

	INPUTS	OUTPUTS
AC	V_{IN} = GND to V_{CC}, V_M = 50% V_{CC}	$V_{OUT} = V_{OL}$ to V_{OH}
ACT	V_{IN} = GND to 3.0V, V_M = 1.5V	V_M = 50% V_{CC}

TEST CIRCUIT



Test Circuit

DEFINITIONS

C_L = Load capacitance, 50pF; includes jig and probe capacitance

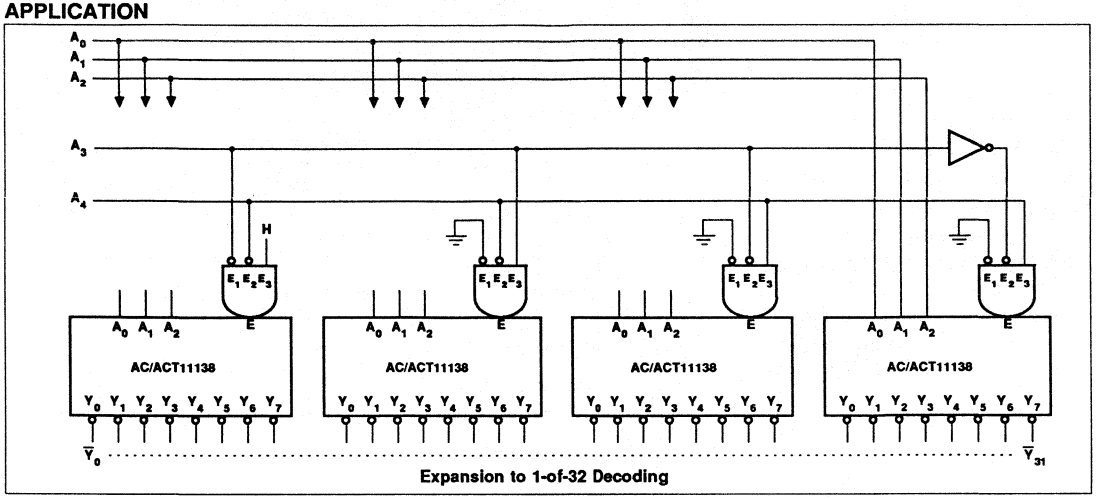
R_L = Load resistor, 500Ω

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators

Input pulses: PRR ≤ 10MHz

$t_r = t_f$ = 3ns

APPLICATION



Expansion to 1-of-32 Decoding

74AC/ACT11139

Dual 2-to-4 Line Decoder/ Demultiplexer; Active-Low

AC11139: Product Specification
ACT11139: Objective Specification

FEATURES

- **Demultiplexing capability**
- **Two independent 1-of-4 decoders**
- **Inverting outputs**
- **Output capability: ±24 mA**
- **CMOS (AC) and TTL (ACT) voltage level inputs**
- **50Ω incident wave switching**
- **Center-pin V_{CC} and ground configuration to minimize high-speed switching noise**
- **I_{CC} category: MSI**

DESCRIPTION

The 74AC/ACT11139 high-performance CMOS devices combine very high speed and high output drive comparable to the most advanced TTL families.

The 74AC/ACT11139 has two independent decoders, each accepting two binary weighted inputs (nA_0, nA_1) and providing four mutually exclusive active-Low outputs ($n\overline{Y}_0$ - $n\overline{Y}_3$). Each decoder has an active-Low Enable ($n\overline{E}$). When $\overline{E}$ is High, every output is forced High. The Enable can be used as the Data input for a 1-of-4 demultiplexer application.

GENERAL INFORMATION

SYMBOL	PARAMETER	CONDITIONS T_A = 25°C; GND = 0V; V_{CC} = 5.0V	TYPICAL		UNIT
			AC	ACT	
t_{PLH}/ t_{PHL}	Propagation delay nA_n to $n\overline{Y}_n$	C_L = 50pF	3.8	5.0	ns
C_{PD}	Power dissipation capacitance per decoder[1]	f = 1MHz; C_L = 50pF	46	52	pF
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	3.5	3.5	pF
I_{LATCH}	Latch-up current	Per Jedec JC40.2 Standard 17	500	500	mA

Note:

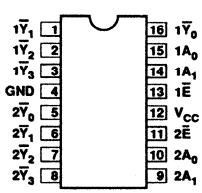
1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_I + \Sigma (C_L \times V_{CC}^2 \times f_O)$ where:
   f_I = input frequency in MHz, C_L = output load capacitance in pF,
   f_O = output frequency in MHz, V_{CC} = supply voltage in V,
   $\Sigma (C_L \times V_{CC}^2 \times f_O)$ = sum of outputs

ORDERING INFORMATION

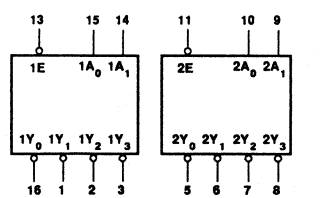
PACKAGES	TEMPERATURE RANGE	ORDER CODE
16-pin plastic DIP (300mil-wide)	-40°C to +85°C	74AC11139N 74ACT11139N
16-pin plastic SO (150mil-wide)	-40°C to +85°C	74AC11139D 74ACT11139D

PIN CONFIGURATION

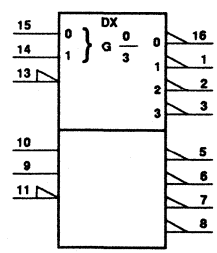
N and D Packages



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



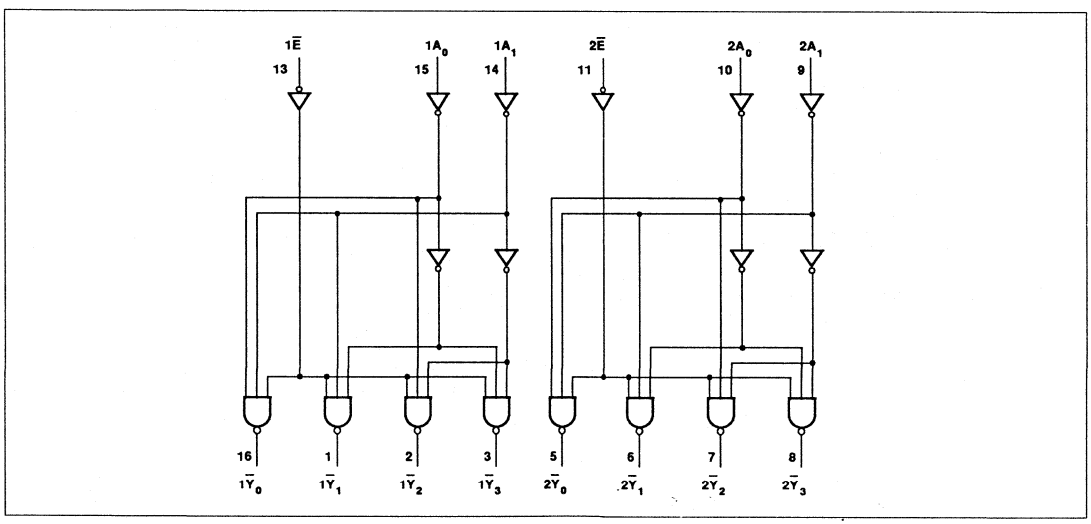
PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
15, 14	$1A_0$, $1A_1$	Address inputs, decoder 1
13	$1\overline{E}$	Enable input (active Low), decoder 1
16, 1, 2, 3	$1\overline{Y}_0$ to $1\overline{Y}_3$	Outputs, decoder 1
10, 9	$2A_0$, $2A_1$	Address inputs, decoder 2
11	$2\overline{E}$	Enable input (active Low), decoder 2
5, 6, 7, 8	$2\overline{Y}_0$ to $2\overline{Y}_3$	Outputs, decoder 2
4	GND	Ground (0V)
12	V_{CC}	Positive supply voltage

FUNCTION TABLE

INPUTS			OUTPUTS			
$\overline{E}$	A_0	A_1	$\overline{Y}_0$	$\overline{Y}_1$	$\overline{Y}_2$	$\overline{Y}_3$
H	X	X	H	H	H	H
L	L	L	L	H	H	H
L	H	L	H	L	H	H
L	L	H	H	H	L	H
L	H	H	H	H	H	L

LOGIC DIAGRAM



RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	74AC11139			74ACT11139			UNIT
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	DC supply voltage	3.0[1]	5.0	5.5	4.5	5.0	5.5	V
V_I	Input voltage	0		V_{CC}	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	0		V_{CC}	V
$\Delta t/\Delta v$	Input transition rise or fall rate	0		10	0		10	ns/V
T_A	Operating free-air temperature	-40		+85	-40		+85	°C

NOTE:
1. No electrical or switching characteristics are specified at V_{CC} < 3V. Operation between 2V and 3V is not recommended, but within that range, a device output will maintain a previously established logic state.

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	TEST CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 to+7.0	V
I_{IK} or V_I	DC input diode current[2]	$V_I < 0$	-20	mA
		$V_I > V_{CC}$	20	
	DC input voltage		-0.5 to V_{CC} +0.5	V
I_{OK} or V_O	DC output diode current[2]	$V_O < 0$	-50	mA
		$V_O > V_{CC}$	50	
	DC output voltage		-0.5 to V_{CC} +0.5	V
I_O	DC output source or sink current per output pin	V_O = 0 to V_{CC}	±50	mA
I_{CC} or I_{GND}	DC V_{CC} current		±200	mA
	DC ground current		±200	
T_{STG}	Storage temperature		-65 to 150	°C
P_{TOT}	Power dissipation per package Plastic DIP	Above 70°C:derate linearly by 8mW/K	500	mW
	Power dissipation per package Plastic surface mount (SO)	Above 70°C:derate linearly by 6mW/K	400	mW

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		V_{CC}	74AC11139				74ACT11139				UNIT
					T_A = +25°C		T_A = -40°C to +85°C		T_A = +25°C		T_A = -40°C to +85°C		
				V	Min	Max	Min	Max	Min	Max	Min	Max	
V_{IH}	High-level input voltage			3.0	2.10		2.10						V
				4.5	3.15		3.15		2.0		2.0		
				5.5	3.85		3.85		2.0		2.0		
V_{IL}	Low-level input voltage			3.0		0.90		0.90					V
				4.5		1.35		1.35		0.8		0.8	
				5.5		1.65		1.65		0.8		0.8	
V_{OH}	High-level output voltage	V_I = V_{IL} or V_{IH}	I_{OH} = -50μA	3.0	2.9		2.9						V
				4.5	4.4		4.4		4.4		4.4		
				5.5	5.4		5.4		5.4		5.4		
			I_{OH} = -4mA	3.0	2.58		2.48						
			I_{OH} = -24mA	4.5	3.94		3.8		3.94		3.8		
				5.5	4.94		4.8		4.94		4.8		
			I_{OH} = -75mA[1]	5.5			3.85				3.85		
V_{OL}	Low-level output voltage	V_I = V_{IL} or V_{IH}	I_{OL} = 50μA	3.0		0.1		0.1					V
				4.5		0.1		0.1		0.1		0.1	
				5.5		0.1		0.1		0.1		0.1	
			I_{OL} = 12mA	3.0		0.36		0.44					
			I_{OL} = 24mA	4.5		0.36		0.44		0.36		0.44	
				5.5		0.36		0.44		0.36		0.44	
			I_{OL} = 75mA[1]	5.5				1.65				1.65	
I_I	Input leakage current	V_I = V_{CC} or GND		5.5		±0.1		±1.0		±0.1		±1.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC} or GND, I_O = 0		5.5		8.0		80		8.0		80	μA
ΔI_{CC}	Supply current, TTL inputs High[2]	One input at 3.4V, other inputs at V_{CC} or GND		5.5						0.9		1.0	mA

NOTES:
1. Not more than one output should be tested at a time, and the duration of the test should not exceed 10ms.
2. This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0V or V_{CC}.

AC ELECTRICAL CHARACTERISTICS AT 3.3V ±0.3V

SYMBOL	PARAMETER	WAVEFORM	74AC11139					UNIT
			T_A = +25°C			T_A = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay nA_n to $n\overline{Y}_n$	1 and 2	1.5 1.5	5.3 6.0	8.1 8.4	1.5 1.5	9.0 9.4	ns
t_{PLH} t_{PHL}	Propagation delay $n\overline{E}$ to $n\overline{Y}_n$	2	1.5 1.5	5.3 5.6	6.9 7.4	1.5 1.5	7.6 8.1	ns

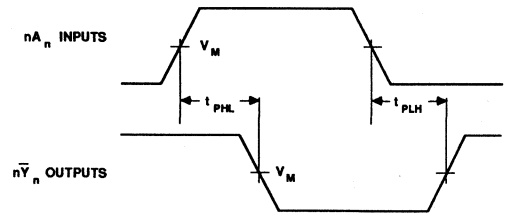
AC ELECTRICAL CHARACTERISTICS AT 5.0V ±0.5V

SYMBOL	PARAMETER	WAVEFORM	74AC11139					UNIT
			T_A = +25°C			T_A = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay nA_n to $n\overline{Y}_n$	1 and 2	1.5 1.5	3.5 4.1	6.0 6.3	1.5 1.5	6.6 6.9	ns
t_{PLH} t_{PHL}	Propagation delay $n\overline{E}$ to $n\overline{Y}_n$	2	1.5 1.5	3.8 4.0	5.2 5.6	1.5 1.5	5.7 6.2	ns

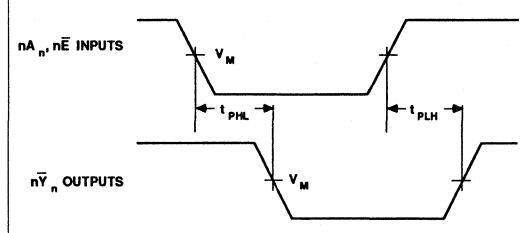
AC ELECTRICAL CHARACTERISTICS AT 5.0V ±0.5V

SYMBOL	PARAMETER	WAVEFORM	74ACT11139					UNIT
			T_A = +25°C			T_A = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay nA_n to $n\overline{Y}_n$	1 and 2	1.5 1.5			1.5 1.5		ns
t_{PLH} t_{PHL}	Propagation delay $n\overline{E}$ to $n\overline{Y}_n$	2	1.5 1.5			1.5 1.5		ns

AC WAVEFORMS



Waveform 1. Waveforms Showing the Inputs (nA_n) to Output ($n\overline{Y}_n$) Propagation Delays

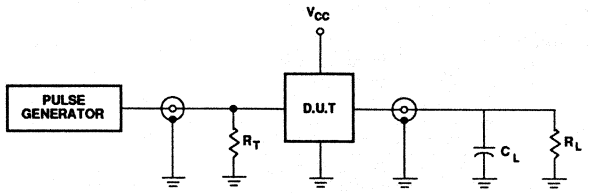


Waveform 2. Waveforms Showing the Inputs (nA_n, $n\overline{E}$) to Output ($n\overline{Y}_n$) Propagation Delays

WAVEFORM CONDITIONS

	INPUTS	OUTPUTS
AC	V_{IN} = GND to V_{CC}, V_M = 50% V_{CC}	V_{OUT} = V_{OL} to V_{OH}
ACT	V_{IN} = GND to 3.0V, V_M = 1.5V	V_M = 50% V_{CC}

TEST CIRCUIT



Test Circuit

DEFINITIONS

C_L = Load capacitance, 50pF; includes jig and probe capacitance

R_L = Load resistor, 500Ω

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators

Input pulses: PRR ≤ 10MHz

$t_r = t_f$ = 3ns

74AC/ACT11150

16-Input Multiplexer (3-State)

Objective Specification

FEATURES

- **Output capability: ±24 mA**
- **CMOS (AC) and TTL (ACT) voltage level inputs**
- **50Ω incident wave switching**
- **Center-pin V_{CC} and ground configuration to minimize high-speed switching noise**
- **I_{CC} category: MSI**

DESCRIPTION

The 74AC/ACT11150 high-performance CMOS devices combine very high speed and high output drive comparable to the most advanced TTL families.

The 74AC/ACT11150 provides a 16-to-1 multiplexer with four select lines and an output enable. The state of the Select (S_n) inputs determines the particular input line from which the data comes. The output Enable ($\overline{OE}$) input is active-Low. When $\overline{OE}$ is High, the Y output is in the High-impedance "OFF" state regardless of all other input conditions.

The device is the logic implementation of a single pole, 16 position switch where the position of the switch is determined by the logic levels supplied to the Select inputs.

GENERAL INFORMATION

SYMBOL	PARAMETER	CONDITIONS T_A = 25°C; GND = 0V; V_{CC} = 5.0V		TYPICAL AC	TYPICAL ACT	UNIT
t_{PLH}/t_{PHL}	Propagation delay I_n to Y	C_L = 50pF		5.6	7.4	ns
C_{PD}	Power dissipation capacitance[1]	f = 1MHz; C_L = 50pF	Enabled	53	60	pF
			Disabled	24	22	
C_{IN}	Input capacitance	V_I = 0V or V_{CC}		4.0	4.0	pF
C_{OUT}	Output capacitance	V_O = 0V or V_{CC}; Disabled		10.0	10.0	pF

Note:

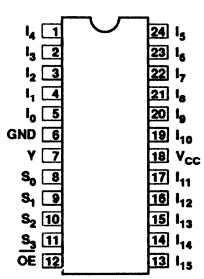
1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_I + \Sigma (C_L \times V_{CC}^2 \times f_O)$ where:
   f_I = input frequency in MHz, C_L = output load capacitance in pF,
   f_O = output frequency in MHz, V_{CC} = supply voltage in V,
   $\Sigma (C_L \times V_{CC}^2 \times f_O)$ = sum of outputs

ORDERING INFORMATION

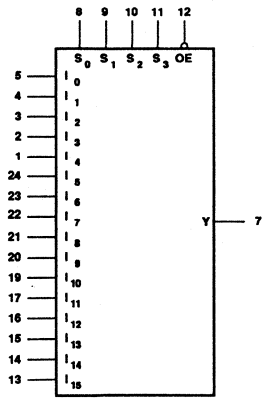
PACKAGES	TEMPERATURE RANGE	ORDER CODE
24-pin plastic DIP (300mil-wide)	-40°C to +85°C	74AC11150N 74ACT11150N
24-pin plastic SO (300mil-wide)	-40°C to +85°C	74AC11150D 74ACT11150D

PIN CONFIGURATION

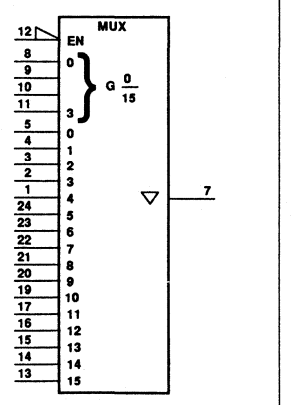
N and D Packages



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



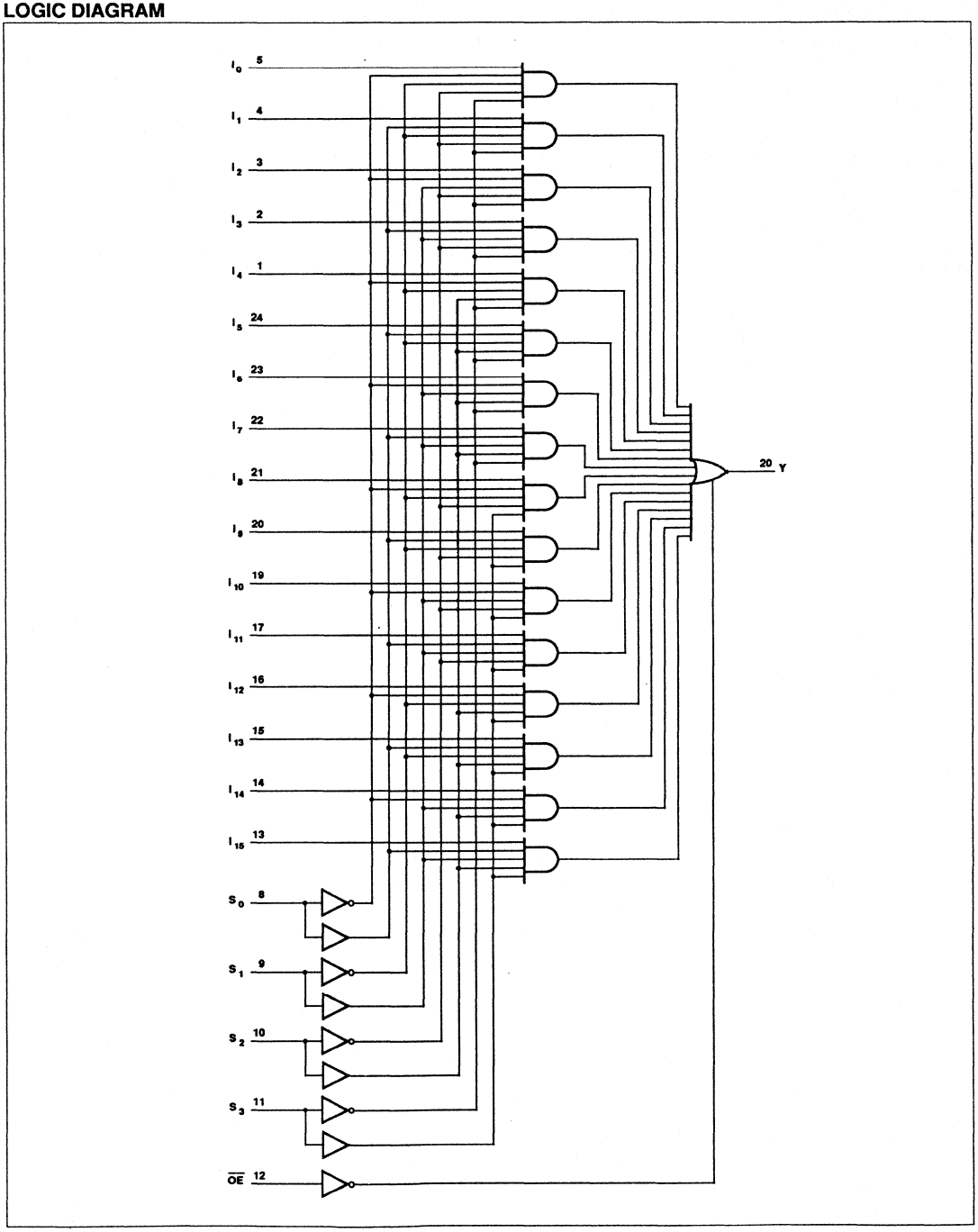
PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
12	$\overline{OE}$	Output enable input (active Low)
8, 9, 10, 11	S_0 - S_3	Select inputs
5, 4, 3, 2, 1, 24, 23, 22, 21, 20, 19, 17, 16, 15, 14, 13	I_0 - I_{15}	Data inputs
7	Y	3-State data output
6	GND	Ground (0V)
18	V_{CC}	Positive supply voltage

FUNCTION TABLE

INPUT						OUTPUT
$\overline{E}$	S_3	S_2	S_1	S_0	I_n	Y
L	L	L	L	L	I_0	I_0
L	L	L	L	H	I_1	I_1
L	L	L	H	L	I_2	I_2
L	L	L	H	H	I_3	I_3
L	L	H	L	L	I_4	I_4
L	L	H	L	H	I_5	I_5
L	L	H	H	L	I_6	I_6
L	L	H	H	H	I_7	I_7
L	H	L	L	L	I_8	I_8
L	H	L	L	H	I_9	I_9
L	H	L	H	L	I_{10}	I_{10}
L	H	L	H	H	I_{11}	I_{11}
L	H	H	L	L	I_{12}	I_{12}
L	H	H	L	H	I_{13}	I_{13}
L	H	H	H	L	I_{14}	I_{14}
L	H	H	H	H	I_{15}	I_{15}
H	X	X	X	X	X	Z

LOGIC DIAGRAM



RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	74AC11150			74ACT11150			UNIT
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	DC supply voltage	3.0[1]	5.0	5.5	4.5	5.0	5.5	V
V_I	Input voltage	0		V_{CC}	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	0		V_{CC}	V
$\Delta t/\Delta v$	Input transition rise or fall rate	0		10	0		10	ns/V
T_A	Operating free-air temperature	-40		+85	-40		+85	°C

NOTE:
1. No electrical or switching characteristics are specified at V_{CC} < 3V. Operation between 2V and 3V is not recommended, but within that range, a device output will maintain a previously established logic state.

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	TEST CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 to+7.0	V
I_{IK} or V_I	DC input diode current[2]	$V_I < 0$	-20	mA
		$V_I > V_{CC}$	20	
	DC input voltage		-0.5 to V_{CC} +0.5	V
I_{OK} or V_O	DC output diode current[2]	$V_O < 0$	-50	mA
		$V_O > V_{CC}$	50	
	DC output voltage		-0.5 to V_{CC} +0.5	V
I_O	DC output source or sink current per output pin	V_O = 0 to V_{CC}	±50	mA
I_{CC} or I_{GND}	DC V_{CC} current		±100	mA
	DC ground current		±100	
T_{STG}	Storage temperature		-65 to 150	°C
P_{TOT}	Power dissipation per package Plastic DIP	Above 70°C:derate linearly by 8mW/K	500	mW
	Power dissipation per package Plastic surface mount (SO)	Above 70°C:derate linearly by 6mW/K	400	mW

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		V_{CC}	74AC11150				74ACT11150				UNIT
					T_A = +25°C		T_A = -40°C to +85°C		T_A = +25°C		T_A = -40°C to +85°C		
				V	Min	Max	Min	Max	Min	Max	Min	Max	
V_{IH}	High-level input voltage			3.0	2.10		2.10						V
				4.5	3.15		3.15		2.0		2.0		
				5.5	3.85		3.85		2.0		2.0		
V_{IL}	Low-level input voltage			3.0		0.90		0.90					V
				4.5		1.35		1.35		0.8		0.8	
				5.5		1.65		1.65		0.8		0.8	
V_{OH}	High-level output voltage	V_I = V_{IL} or V_{IH}	I_{OH} = -50μA	3.0	2.9		2.9						V
				4.5	4.4		4.4		4.4		4.4		
				5.5	5.4		5.4		5.4		5.4		
			I_{OH} = -4mA	3.0	2.58		2.48						
			I_{OH} = -24mA	4.5	3.94		3.8		3.94		3.8		
				5.5	4.94		4.8		4.94		4.8		
			I_{OH} = -75mA[1]	5.5			3.85				3.85		
V_{OL}	Low-level output voltage	V_I = V_{IL} or V_{IH}	I_{OL} = 50μA	3.0		0.1		0.1					V
				4.5		0.1		0.1		0.1		0.1	
				5.5		0.1		0.1		0.1		0.1	
			I_{OL} = 12mA	3.0		0.36		0.44					
			I_{OL} = 24mA	4.5		0.36		0.44		0.36		0.44	
				5.5		0.36		0.44		0.36		0.44	
			I_{OL} = 75mA[1]	5.5				1.65				1.65	
I_I	Input leakage current	V_I = V_{CC} or GND		5.5		±0.1		±1.0		±0.1		±1.0	μA
I_{OZ}	3-State output off-state current	V_I = V_{IL} or V_{IH}, V_O = V_{CC} or GND		5.5		±0.5		±5.0		±0.5		±5.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC} or GND, I_O = 0		5.5		8.0		80		8.0		80	μA
ΔI_{CC}	Supply current, TTL inputs High[2]	One input at 3.4V, other inputs at V_{CC} or GND		5.5						0.9		1.0	mA

NOTES:
1. Not more than one output should be tested at a time, and the duration of the test should not exceed 10ms.
2. This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0V or V_{CC}.

74AC/ACT11151
8-Input Multiplexer

Product Specification

FEATURES

- **Output capability: ±24 mA**
- **CMOS (AC) and TTL (ACT) voltage level inputs**
- **50Ω incident wave switching**
- **Center-pin V_{CC} and ground configuration to minimize high-speed switching noise**
- **I_{CC} category: MSI**

DESCRIPTION

The 74AC/ACT11151 high-performance CMOS devices combine very high speed and high output drive comparable to the most advanced TTL families.

The 74AC/ACT11151 provides an 8-to-1 multiplexer with three select lines and a common enable. The state of the Select (S_n) inputs determines the particular input line from which the data comes. The Enable ($\overline{E}$) input is active-Low. When $\overline{E}$ is High, the Y output is forced Low and the $\overline{Y}$ is forced High regardless of all other input conditions.

The device is the logic implementation of a single pole, 8 position switch where the position of the switch is determined by the logic levels supplied to the Select inputs.

GENERAL INFORMATION

SYMBOL	PARAMETER	CONDITIONS T_A = 25°C; GND = 0V; V_{CC} = 5.0V	TYPICAL		UNIT
			AC	ACT	
t_{PLH}/t_{PHL}	Propagation delay I_n to Y or $\overline{Y}$	C_L = 50pF	4.0	5.2	ns
C_{PD}	Power dissipation capacitance[1]	f = 1MHz; C_L = 50pF	52	56	pF
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	3.5	3.5	pF
I_{LATCH}	Latch-up current	Per Jedec JC40.2 Standard 17	500	500	mA

Note:

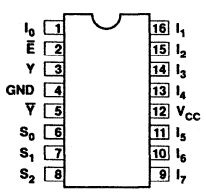
1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_I + \Sigma (C_L \times V_{CC}^2 \times f_O)$ where:
   f_I = input frequency in MHz, C_L = output load capacitance in pF,
   f_O = output frequency in MHz, V_{CC} = supply voltage in V,
   $\Sigma (C_L \times V_{CC}^2 \times f_O)$ = sum of outputs

ORDERING INFORMATION

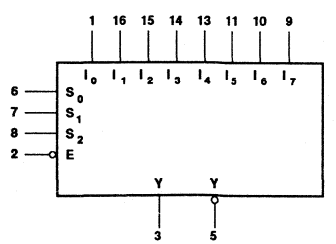
PACKAGES	TEMPERATURE RANGE	ORDER CODE
16-pin plastic DIP (300mil-wide)	-40°C to +85°C	74AC11151N 74ACT11151N
16-pin plastic SO (150mil-wide)	-40°C to +85°C	74AC11151D 74ACT11151D

PIN CONFIGURATION

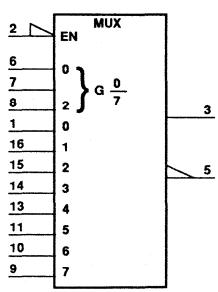
N and D Packages



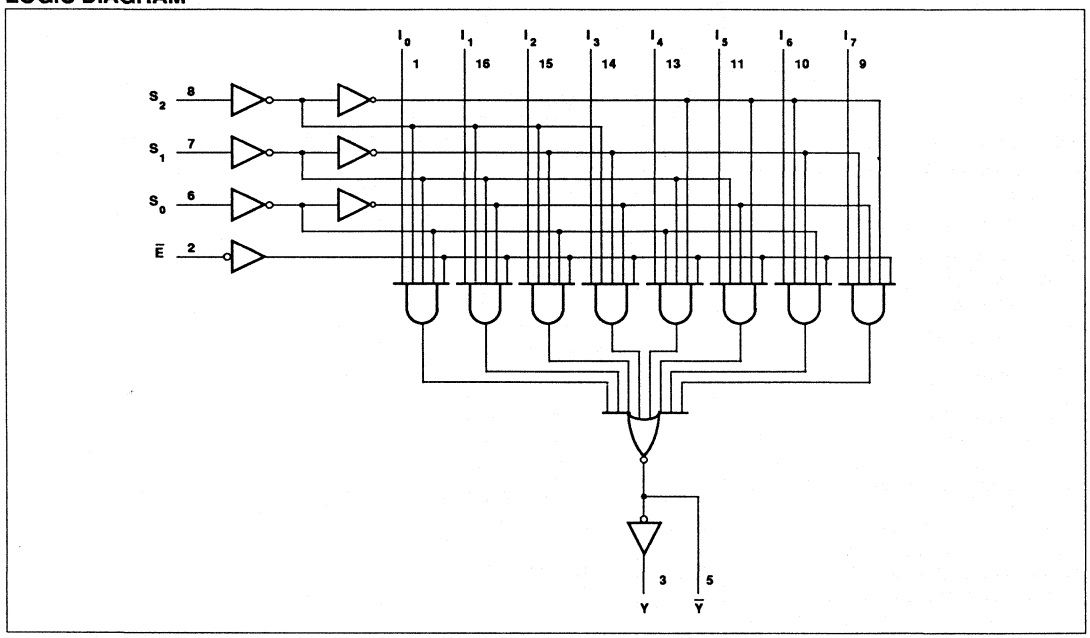
LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



LOGIC DIAGRAM



PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
6, 7, 8	S_n	Select inputs
2	$\overline{E}$	Enable input
1, 16, 15, 14 13, 11, 10, 9	$I_0 - I_7$	Data inputs
3, 5	Y, $\overline{Y}$	Data outputs
4	GND	Ground (0V)
12	V_{CC}	Positive supply voltage

FUNCTION TABLE

INPUTS				OUTPUTS	
S_2	S_1	S_0	E	Y	$\overline{Y}$
X	X	X	H	L	H
L	L	L	L	I_0	$\overline{I}_0$
L	L	H	L	I_1	$\overline{I}_1$
L	H	L	L	I_2	$\overline{I}_2$
L	H	H	L	I_3	$\overline{I}_3$
H	L	L	L	I_4	$\overline{I}_4$
H	L	H	L	I_5	$\overline{I}_5$
H	H	L	L	I_6	$\overline{I}_6$
H	H	H	L	I_7	$\overline{I}_7$

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	74AC11151			74ACT11151			UNIT
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	DC supply voltage	3.0[1]	5.0	5.5	4.5	5.0	5.5	V
V_I	Input voltage	0		V_{CC}	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	0		V_{CC}	V
$\Delta t/\Delta v$	Input transition rise or fall rate	0		10	0		10	ns/V
T_A	Operating free-air temperature	-40		+85	-40		+85	°C

NOTE:
1. No electrical or switching characteristics are specified at V_{CC} < 3V. Operation between 2V and 3V is not recommended, but within that range, a device output will maintain a previously established logic state.

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	TEST CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 to+7.0	V
I_{IK} or V_I	DC input diode current[2]	$V_I < 0$	-20	mA
		$V_I > V_{CC}$	20	
	DC input voltage		-0.5 to V_{CC} +0.5	V
I_{OK} or V_O	DC output diode current[2]	$V_O < 0$	-50	mA
		$V_O > V_{CC}$	50	
	DC output voltage		-0.5 to V_{CC} +0.5	V
I_O	DC output source or sink current per output pin	V_O = 0 to V_{CC}	±50	mA
I_{CC} or I_{GND}	DC V_{CC} current		±100	mA
	DC ground current		±100	
T_{STG}	Storage temperature		-65 to 150	°C
P_{TOT}	Power dissipation per package Plastic DIP	Above 70°C:derate linearly by 8mW/K	500	mW
	Power dissipation per package Plastic surface mount (SO)	Above 70°C:derate linearly by 6mW/K	400	mW

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		V_{CC}	74AC11151				74ACT11151				UNIT
					T_A = +25°C		T_A = -40°C to +85°C		T_A = +25°C		T_A = -40°C to +85°C		
				V	Min	Max	Min	Max	Min	Max	Min	Max	
V_{IH}	High-level input voltage			3.0	2.10		2.10						V
				4.5	3.15		3.15		2.0		2.0		
				5.5	3.85		3.85		2.0		2.0		
V_{IL}	Low-level input voltage			3.0		0.90		0.90					V
				4.5		1.35		1.35		0.8		0.8	
				5.5		1.65		1.65		0.8		0.8	
V_{OH}	High-level output voltage	V_I = V_{IL} or V_{IH}	I_{OH} = -50μA	3.0	2.9		2.9						V
				4.5	4.4		4.4		4.4		4.4		
				5.5	5.4		5.4		5.4		5.4		
			I_{OH} = -4mA	3.0	2.58		2.48						
			I_{OH} = -24mA	4.5	3.94		3.8		3.94		3.8		
				5.5	4.94		4.8		4.94		4.8		
			I_{OH} = -75mA[1]	5.5			3.85				3.85		
V_{OL}	Low-level output voltage	V_I = V_{IL} or V_{IH}	I_{OL} = 50μA	3.0		0.1		0.1					V
				4.5		0.1		0.1		0.1		0.1	
				5.5		0.1		0.1		0.1		0.1	
			I_{OL} = 12mA	3.0		0.36		0.44					
			I_{OL} = 24mA	4.5		0.36		0.44		0.36		0.44	
				5.5		0.36		0.44		0.36		0.44	
			I_{OL} = 75mA[1]	5.5				1.65				1.65	
I_I	Input leakage current	V_I = V_{CC} or GND		5.5		±0.1		±1.0		±0.1		±1.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC} or GND, I_O = 0		5.5		8.0		80		8.0		80	μA
ΔI_{CC}	Supply current, TTL inputs High[2]	One input at 3.4V, other inputs at V_{CC} or GND		5.5						0.9		1.0	mA

NOTES:
1. Not more than one output should be tested at a time, and the duration of the test should not exceed 10ms.
2. This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0V or V_{CC}.

AC ELECTRICAL CHARACTERISTICS AT 3.3V ±0.3V

SYMBOL	PARAMETER	WAVEFORM	74AC11151					UNIT
			T_A = +25°C			T_A = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay I_n to Y	1	1.9 1.9	6.5 6.4	8.1 8.1	1.9 1.9	9.2 8.9	ns
t_{PLH} t_{PHL}	Propagation delay I_n to $\overline{Y}$	1	1.7 1.9	6.1 6.4	7.7 8.0	1.7 1.9	8.6 8.8	ns
t_{PLH} t_{PHL}	Propagation delay S to Y	1	3.2 3.4	8.9 8.9	10.7 10.8	3.2 3.4	12.0 12.1	ns
t_{PLH} t_{PHL}	Propagation delay S to $\overline{Y}$	1	3.2 3.1	8.6 8.7	10.3 10.7	3.2 3.1	11.6 12.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{E}$ to Y	2	1.3 1.6	4.0 4.5	5.5 5.9	1.3 1.6	6.0 6.5	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{E}$ to $\overline{Y}$	2	2.0 1.7	5.2 4.7	6.7 6.2	2.0 1.7	7.4 6.7	ns

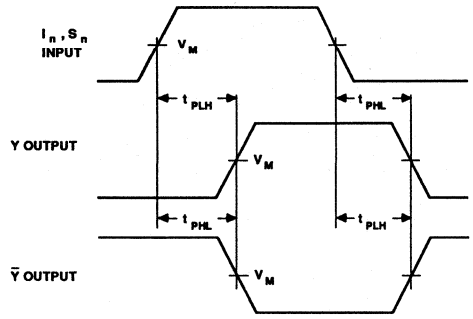
AC ELECTRICAL CHARACTERISTICS AT 5.0V ±0.5V

SYMBOL	PARAMETER	WAVEFORM	74AC11151					UNIT
			T_A = +25°C			T_A = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay I_n to Y	1	1.5 1.5	4.1 4.0	5.8 5.7	1.5 1.5	6.5 6.4	ns
t_{PLH} t_{PHL}	Propagation delay I_n to $\overline{Y}$	1	1.4 1.6	3.7 4.1	5.5 5.8	1.4 1.6	6.0 6.4	ns
t_{PLH} t_{PHL}	Propagation delay S to Y	1	2.5 2.7	5.4 5.6	7.3 7.5	2.5 2.7	8.3 8.5	ns
t_{PLH} t_{PHL}	Propagation delay S to $\overline{Y}$	1	2.6 2.6	5.3 5.4	7.2 7.4	2.6 2.6	8.1 8.4	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{E}$ to Y	2	1.1 1.4	2.7 3.1	4.2 4.6	1.1 1.4	4.6 5.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{E}$ to $\overline{Y}$	2	1.7 1.4	3.5 3.1	5.1 4.6	1.7 1.4	5.6 5.0	ns

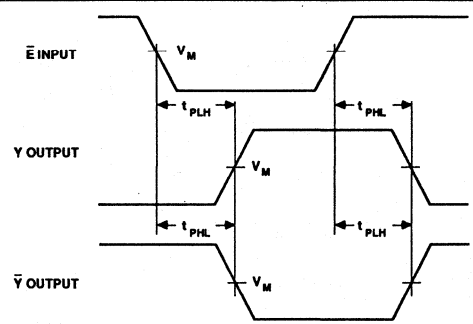
AC ELECTRICAL CHARACTERISTICS AT 5.0V ±0.5V

SYMBOL	PARAMETER	WAVEFORM	74ACT11151					UNIT
			T_A = +25°C			T_A = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay I_n to Y	1	3.2 2.2	5.7 5.2	7.5 8.0	3.2 2.2	8.3 8.8	ns
t_{PLH} t_{PHL}	Propagation delay I_n to $\overline{Y}$	1	2.1 2.7	4.7 5.1	7.3 6.9	2.1 2.7	7.8 7.6	ns
t_{PLH} t_{PHL}	Propagation delay S to Y	1	3.6 3.1	6.8 6.7	9.9 9.5	3.6 3.1	11.0 10.5	ns
t_{PLH} t_{PHL}	Propagation delay S to $\overline{Y}$	1	2.9 2.7	6.3 6.3	9.0 9.3	2.9 2.7	10.0 10.4	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{E}$ to Y	2	1.5 2.1	3.7 4.0	5.8 5.6	1.5 2.1	6.3 6.2	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{E}$ to $\overline{Y}$	2	2.5 1.7	4.4 4.1	6.1 6.4	2.5 1.7	6.7 6.9	ns

AC WAVEFORMS



Waveform 1. Waveforms Showing the Data Inputs (nI_0, nI_1) and Select Input (S_n) to Output (Y, $\overline{Y}$) Propagation Delays

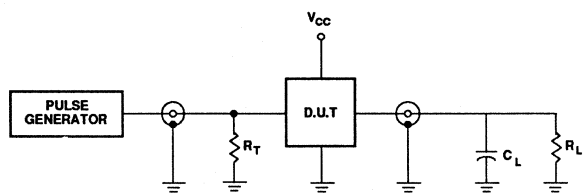


Waveform 2. Waveforms Showing the Enable Input ($\overline{E}$) to Output (Y, $\overline{Y}$) Propagation Delays

WAVEFORM CONDITIONS

	INPUTS	OUTPUTS
AC	V_{IN} = GND to V_{CC}, V_M = 50% V_{CC}	V_{OUT} = V_{OL} to V_{OH}
ACT	V_{IN} = GND to 3.0V, V_M = 1.5V	V_M = 50% V_{CC}

TEST CIRCUIT



Test Circuit

DEFINITIONS

C_L = Load capacitance, 50pF; includes jig and probe capacitance

R_L = Load resistor, 500Ω

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators

Input pulses: PRR ≤ 10MHz

$t_r = t_f$ = 3ns

74AC/ACT11153

Dual 4-Input Multiplexer

Objective Specification

FEATURES

- **Separate Output Enable inputs for each section**
- **Common Select inputs**
- **Output capability: ±24 mA**
- **CMOS (AC) and TTL (ACT) voltage level inputs**
- **50Ω incident wave switching**
- **Center-pin V_{CC} and ground configuration to minimize high-speed switching noise**
- **I_{CC} category: MSI**

DESCRIPTION

The 74AC/ACT11153 high-performance CMOS devices combine very high speed and high output drive comparable to the most advanced TTL families.

The 74AC/ACT11153 device provides two identical 4-input multiplexers with non-inverting outputs which select two bits from four sources selected by common select inputs (S_0, S_1). When the individual Enable ($1\overline{E}$, $2\overline{E}$) inputs of the 4-input multiplexers are High, the outputs are forced Low.

The 74AC/ACT11153 devices are the logic implementation of a 2-pole, 4-position switch; the position of the switch being determined by the logic levels supplied to the two select inputs.

The '11153 is the non-inverting version of the '11352.

GENERAL INFORMATION

SYMBOL	PARAMETER	CONDITIONS T_A = 25°C; GND = 0V; V_{CC} = 5.0V	TYPICAL		UNIT
			AC	ACT	
t_{PLH}/ t_{PHL}	Propagation delay $1I_n$, $2I_n$ to nY	C_L = 50pF	4.6	5.4	ns
C_{PD}	Power dissipation capacitance per multiplexer[1]	f = 1MHz; C_L = 50pF	39	40	pF
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	3.5	3.5	pF
I_{LATCH}	Latch-up current	Per Jedec JC40.2 Standard 17	500	500	mA

Note:

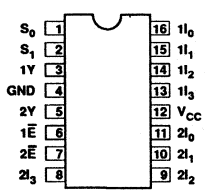
1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_I + \Sigma (C_L \times V_{CC}^2 \times f_O)$ where:
   f_I = input frequency in MHz, C_L = output load capacitance in pF,
   f_O = output frequency in MHz, V_{CC} = supply voltage in V,
   $\Sigma (C_L \times V_{CC}^2 \times f_O)$ = sum of outputs

ORDERING INFORMATION

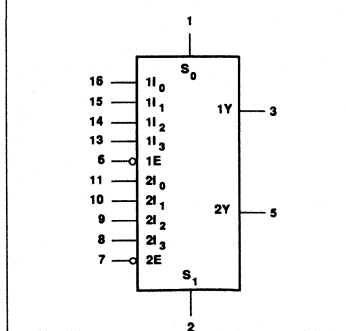
PACKAGES	TEMPERATURE RANGE	ORDER CODE
16-pin plastic DIP (300mil-wide)	-40°C to +85°C	74AC11153N 74ACT11153N
16-pin plastic SO (150mil-wide)	-40°C to +85°C	74AC11153D 74ACT11153D

PIN CONFIGURATION

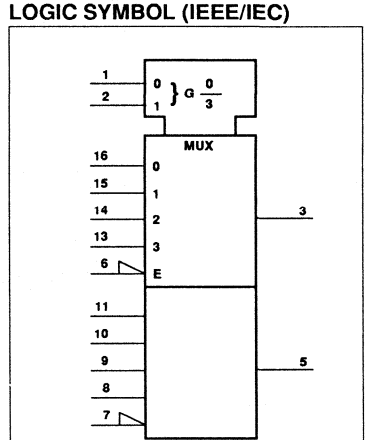
N and D Packages



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



PIN DESCRIPTION

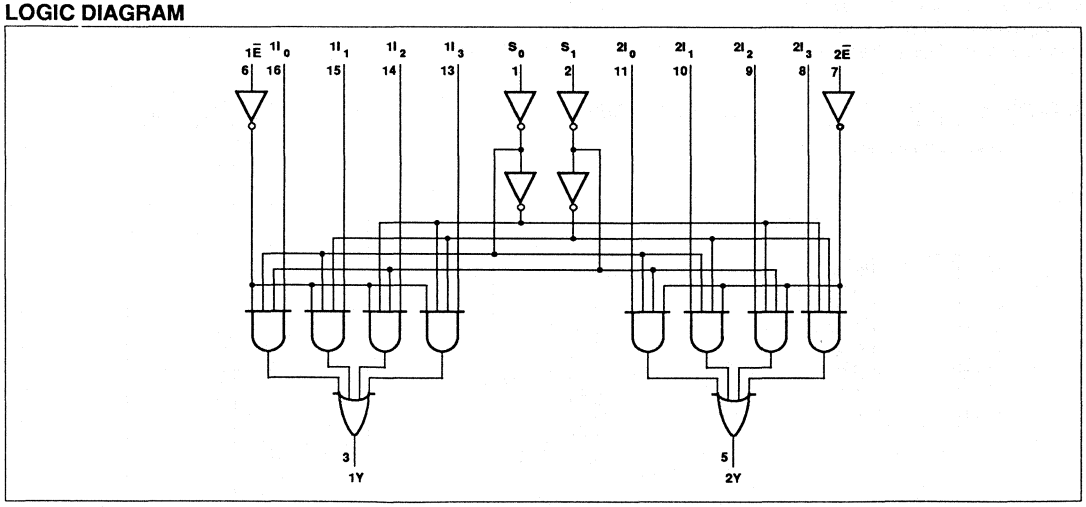
PIN NUMBER	SYMBOL	NAME AND FUNCTION
1, 2	S_0, S_1	Common select inputs
16, 15, 14, 13	$1I_0$ - $1I_3$	Port A data inputs
11, 10, 9, 8	$2I_0$ - $2I_3$	Port B data inputs
6	$1\overline{E}$	Port A enable input (active Low)
7	$2\overline{E}$	Port B enable input (active Low)
3, 5	1Y, 2Y	Data outputs
4	GND	Ground (0V)
12	V_{CC}	Positive supply voltage

FUNCTION TABLE

INPUTS							OUTPUT
$n\overline{E}$	S_0	S_1	nI_0	nI_1	nI_2	nI_3	nY
H	X	X	X	X	X	X	L
L	L	L	L	X	X	X	L
L	L	L	H	X	X	X	H
L	H	L	X	L	X	X	L
L	H	L	X	H	X	X	H
L	L	H	X	X	L	X	L
L	L	H	X	X	H	X	H
L	H	H	X	X	X	L	L
L	H	H	X	X	X	H	H

H = High voltage level steady state
L = Low voltage level steady state
X = Don't care

LOGIC DIAGRAM



RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	74AC11153			74ACT11153			UNIT
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	DC supply voltage	3.0[1]	5.0	5.5	4.5	5.0	5.5	V
V_I	Input voltage	0		V_{CC}	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	0		V_{CC}	V
$\Delta t/\Delta v$	Input transition rise or fall rate	0		10	0		10	ns/V
T_A	Operating free-air temperature	-40		+85	-40		+85	°C

NOTE:

1. No electrical or switching characteristics are specified at V_{CC} < 3V. Operation between 2V and 3V is not recommended, but within that range, a device output will maintain a previously established logic state.

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	TEST CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 to+7.0	V
I_{IK} or V_I	DC input diode current[2]	$V_I < 0$	-20	mA
		$V_I > V_{CC}$	20	
	DC input voltage		-0.5 to V_{CC} +0.5	V
I_{OK} or V_O	DC output diode current[2]	$V_O < 0$	-50	mA
		$V_O > V_{CC}$	50	
	DC output voltage		-0.5 to V_{CC} +0.5	V
I_O	DC output source or sink current per output pin	V_O = 0 to V_{CC}	±50	mA
I_{CC} or I_{GND}	DC V_{CC} current		±100	mA
	DC ground current		±100	
T_{STG}	Storage temperature		-65 to 150	°C
P_{TOT}	Power dissipation per package Plastic DIP	Above 70°C:derate linearly by 8mW/K	500	mW
	Power dissipation per package Plastic surface mount (SO)	Above 70°C:derate linearly by 6mW/K	400	mW

NOTES:

1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		V_{CC}	74AC11153				74ACT11153				UNIT
					T_A = +25°C		T_A = -40°C to +85°C		T_A = +25°C		T_A = -40°C to +85°C		
				V	Min	Max	Min	Max	Min	Max	Min	Max	
V_{IH}	High-level input voltage			3.0	2.10		2.10						V
				4.5	3.15		3.15		2.0		2.0		
				5.5	3.85		3.85		2.0		2.0		
V_{IL}	Low-level input voltage			3.0		0.90		0.90					V
				4.5		1.35		1.35		0.8		0.8	
				5.5		1.65		1.65		0.8		0.8	
V_{OH}	High-level output voltage	V_I = V_{IL} or V_{IH}	I_{OH} = -50μA	3.0	2.9		2.9						V
				4.5	4.4		4.4		4.4		4.4		
				5.5	5.4		5.4		5.4		5.4		
			I_{OH} = -4mA	3.0	2.58		2.48						
			I_{OH} = -24mA	4.5	3.94		3.8		3.94		3.8		
				5.5	4.94		4.8		4.94		4.8		
			I_{OH} = -75mA[1]	5.5			3.85				3.85		
V_{OL}	Low-level output voltage	V_I = V_{IL} or V_{IH}	I_{OL} = 50μA	3.0		0.1		0.1					V
				4.5		0.1		0.1		0.1		0.1	
				5.5		0.1		0.1		0.1		0.1	
			I_{OL} = 12mA	3.0		0.36		0.44					
			I_{OL} = 24mA	4.5		0.36		0.44		0.36		0.44	
				5.5		0.36		0.44		0.36		0.44	
			I_{OL} = 75mA[1]	5.5				1.65				1.65	
I_I	Input leakage current	V_I = V_{CC} or GND		5.5		±0.1		±1.0		±0.1		±1.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC} or GND, I_O = 0		5.5		8.0		80		8.0		80	μA
ΔI_{CC}	Supply current, TTL inputs High[2]	One input at 3.4V, other inputs at V_{CC} or GND		5.5						0.9		1.0	mA

NOTES:
1. Not more than one output should be tested at a time, and the duration of the test should not exceed 10ms.
2. This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0V or V_{CC}.

74AC/ACT11154

4-to-16 Line Decoder/ Demultiplexer; Active Low

Objective Specification

FEATURES

- **Decodes 4 binary coded inputs into one of 16 mutually exclusive outputs**
- **Performs the demultiplexing function by distributing data from one input line to any one of 16 outputs**
- **Output capability: ±24 mA**
- **CMOS (AC) and TTL (ACT) voltage level inputs**
- **50Ω incident wave switching**
- **Center-pin V_{CC} and ground configuration to minimize high-speed switching noise**
- **I_{CC} category: MSI**

DESCRIPTION

The 74AC/ACT11154 high-performance CMOS devices combine very high speed and high output drive comparable to the most advanced TTL families.

The 74AC/ACT11154 device decodes four binary-coded inputs into one of sixteen mutually exclusive outputs when both the Enable inputs ($\overline{E}_1$ and $\overline{E}_2$) are Low. The demultiplexing function is performed by using the 4 input lines to address the output line, passing data from one of the Enable inputs with the other Enable input Low. When either Enable input is High, all outputs are High.

GENERAL INFORMATION

SYMBOL	PARAMETER	CONDITIONS T_A = 25°C; GND = 0V V_{CC} = 5.0V	TYPICAL		UNIT
			AC	ACT	
t_{PLH}/t_{PHL}	Propagation delay A_n to $\overline{Y}_n$	C_L = 50pF	5.5	7.0	ns
C_{PD}	Power dissipation capacitance[1]	f = 1MHz; C_L = 50pF	50	55	pF
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	4.0	4.0	pF
I_{LATCH}	Latch-up current	Per Jedec JC40.2 Standard 17	500	500	mA

Note:

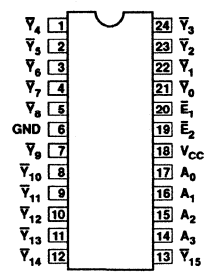
1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_I + \Sigma (C_L \times V_{CC}^2 \times f_O)$ where:
   f_I = input frequency in MHz, C_L = output load capacitance in pF,
   f_O = output frequency in MHz, V_{CC} = supply voltage in V,
   $\Sigma (C_L \times V_{CC}^2 \times f_O)$ = sum of outputs

ORDERING INFORMATION

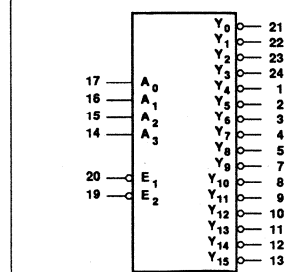
PACKAGES	TEMPERATURE RANGE	ORDER CODE
24-pin plastic DIP (300mil-wide)	-40°C to +85°C	74AC11154N 74ACT11154N
24-pin plastic SO (150mil-wide)	-40°C to +85°C	74AC11154D 74ACT11154D

PIN CONFIGURATION

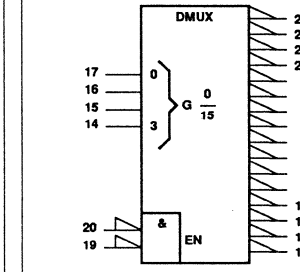
N and D Packages



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
19, 20	$\overline{E}_1, \overline{E}_2$	Enable inputs (active Low)
17, 16, 15, 14	$A_0 - A_3$	Address inputs
21, 22, 23, 24, 1, 2, 3, 4, 5, 7, 8, 9, 10, 11, 12, 13	$\overline{Y}_0 - \overline{Y}_{15}$	Outputs
6	GND	Ground (0V)
18	V_{CC}	Positive supply voltage

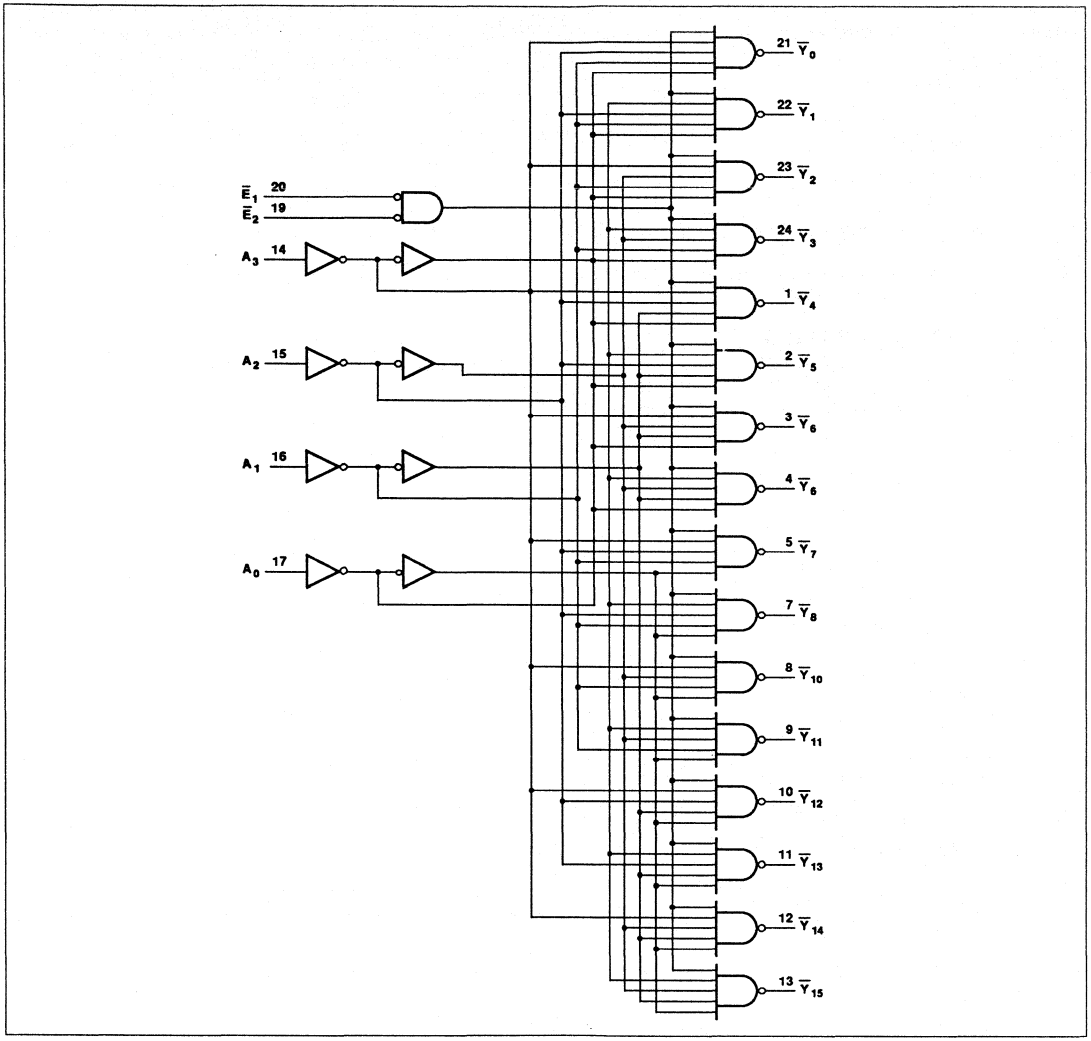
FUNCTION TABLE

INPUTS						OUTPUTS															
$\overline{E}_1$	$\overline{E}_2$	A_3	A_2	A_1	A_0	$\overline{Y}_0$	$\overline{Y}_1$	$\overline{Y}_2$	$\overline{Y}_3$	$\overline{Y}_4$	$\overline{Y}_5$	$\overline{Y}_6$	$\overline{Y}_7$	$\overline{Y}_8$	$\overline{Y}_9$	$\overline{Y}_{10}$	$\overline{Y}_{11}$	$\overline{Y}_{12}$	$\overline{Y}_{13}$	$\overline{Y}_{14}$	$\overline{Y}_{15}$
L	L	L	L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	H	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	H	L	L	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H
L	L	L	H	L	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H
L	L	L	H	H	L	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H
L	L	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H
L	L	H	L	L	L	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H
L	L	H	L	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H
L	L	H	L	H	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H
L	L	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H
L	L	H	H	L	L	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H
L	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H
L	L	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H
L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L
L	H	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
H	L	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
H	H	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H

H = Highvoltage level,
L = Low voltage level,
X = Don't care

4-Line to 16-Line Decoders/Demultiplexers; Active Low

LOGIC DIAGRAM



RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	74AC11154			74ACT11154			UNIT
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	DC supply voltage	3.0[1]	5.0	5.5	4.5	5.0	5.5	V
V_I	Input voltage	0		V_{CC}	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	0		V_{CC}	V
$\Delta t/\Delta v$	Input transition rise or fall rate	0		10	0		10	ns/V
T_A	Operating free-air temperature	-40		+85	-40		+85	°C

NOTE:

1. No electrical or switching characteristics are specified at V_{CC} < 3V. Operation between 2V and 3V is not recommended, but within that range, a device output will maintain a previously established logic state.

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	TEST CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 to+7.0	V
I_{IK} or V_I	DC input diode current[2]	$V_I < 0$	-20	mA
		$V_I > V_{CC}$	20	
	DC input voltage		-0.5 to V_{CC} +0.5	V
I_{OK} or V_O	DC output diode current[2]	$V_O < 0$	-50	mA
		$V_O > V_{CC}$	50	
	DC output voltage		-0.5 to V_{CC} +0.5	V
I_O	DC output source or sink current per output pin	V_O = 0 to V_{CC}	±50	mA
I_{CC} or I_{GND}	DC V_{CC} current		±400	mA
	DC ground current		±400	
T_{STG}	Storage temperature		-65 to 150	°C
P_{TOT}	Power dissipation per package Plastic DIP	Above 70°C:derate linearly by 8mW/K	500	mW
	Power dissipation per package Plastic surface mount (SO)	Above 70°C:derate linearly by 6mW/K	400	mW

NOTES:

1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		V_{CC}	74AC11154				74ACT11154				UNIT
					T_A = +25°C		T_A = -40°C to +85°C		T_A = +25°C		T_A = -40°C to +85°C		
				V	Min	Max	Min	Max	Min	Max	Min	Max	
V_{IH}	High-level input voltage			3.0	2.10		2.10						V
				4.5	3.15		3.15		2.0		2.0		
				5.5	3.85		3.85		2.0		2.0		
V_{IL}	Low-level input voltage			3.0		0.90		0.90					V
				4.5		1.35		1.35		0.8		0.8	
				5.5		1.65		1.65		0.8		0.8	
V_{OH}	High-level output voltage	V_I = V_{IL} or V_{IH}	I_{OH} = -50μA	3.0	2.9		2.9						V
				4.5	4.4		4.4		4.4		4.4		
				5.5	5.4		5.4		5.4		5.4		
			I_{OH} = -4mA	3.0	2.58		2.48						
			I_{OH} = -24mA	4.5	3.94		3.8		3.94		3.8		
				5.5	4.94		4.8		4.94		4.8		
			I_{OH} = -75mA[1]	5.5			3.85				3.85		
V_{OL}	Low-level output voltage	V_I = V_{IL} or V_{IH}	I_{OL} = 50μA	3.0		0.1		0.1					V
				4.5		0.1		0.1		0.1		0.1	
				5.5		0.1		0.1		0.1		0.1	
			I_{OL} = 12mA	3.0		0.36		0.44					
			I_{OL} = 24mA	4.5		0.36		0.44		0.36		0.44	
				5.5		0.36		0.44		0.36		0.44	
			I_{OL} = 75mA[1]	5.5				1.65				1.65	
I_I	Input leakage current	V_I = V_{CC} or GND		5.5		±0.1		±1.0		±0.1		±1.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC} or GND, I_O = 0		5.5		8.0		80		8.0		80	μA
ΔI_{CC}	Supply current, TTL inputs High[2]	One input at 3.4V, other inputs at V_{CC} or GND		5.5						0.9		1.0	mA

NOTES:

1. Not more than one output should be tested at a time, and the duration of the test should not exceed 10ms.
2. This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0V or V_{CC}.

74AC/ACT11157

Quad 2-Input Multiplexer

Objective Specification

FEATURES

- **Output capability: ±24 mA**
- **CMOS (AC) and TTL (ACT) voltage level inputs**
- **50Ω incident wave switching**
- **Center-pin V_{CC} and ground configuration to minimize high-speed switching noise**
- **I_{CC} category: MSI**

DESCRIPTION

The 74AC/ACT11157 high-performance CMOS devices combine very high speed and high output drive comparable to the most advanced TTL families.

The 74AC/ACT11157 provides four 2-to-1 multiplexers with a common selector and a common enable. The state of the Select (S) input determines the particular input from which the data comes. The Enable ($\overline{E}$) input is active-Low. When $\overline{E}$ is High, all of the outputs (Y) are forced Low regardless of all other input conditions.

The device is the logic implementation of a 4-pole, 2 position switch where the position of the switch is determined by the logic levels supplied to the Select input.

GENERAL INFORMATION

SYMBOL	PARAMETER	CONDITIONS T_A = 25°C; GND = 0V; V_{CC} = 5.0V	TYPICAL		UNIT
			AC	ACT	
t_{PLH}/t_{PHL}	Propagation delay nI_0, nI_1 to nY	C_L = 50pF	4.0	5.0	ns
C_{PD}	Power dissipation capacitance per mulitplexer[1]	f = 1MHz; C_L = 50pF	26	26	pF
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	4.0	4.0	pF
I_{LATCH}	Latch-up current	Per Jedec JC40.2 Standard 17	500	500	mA

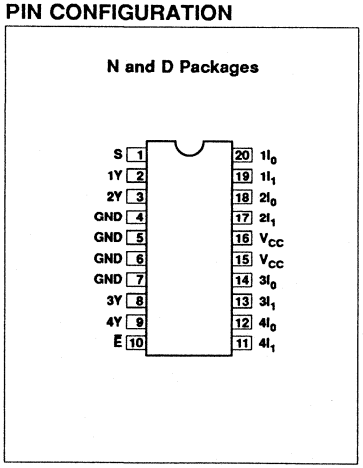
Note:

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_I + \Sigma (C_L \times V_{CC}^2 \times f_O)$ where:
   f_I = input frequency in MHz, C_L = output load capacitance in pF,
   f_O = output frequency in MHz, V_{CC} = supply voltage in V,
   $\Sigma (C_L \times V_{CC}^2 \times f_O)$ = sum of outputs

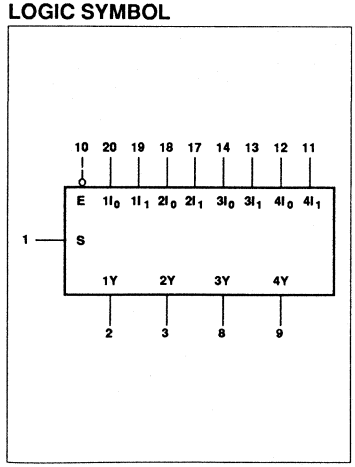
ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE
20-pin plastic DIP (300mil-wide)	-40°C to +85°C	74AC11157N 74ACT11157N
20-pin plastic SO (300mil-wide)	-40°C to +85°C	74AC11157D 74ACT11157D

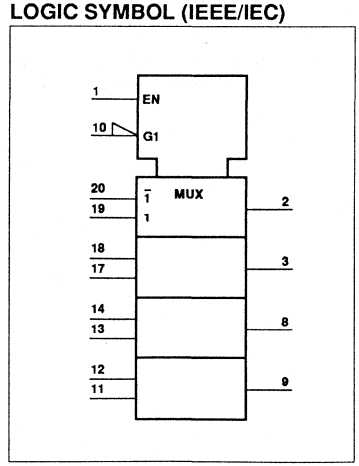
PIN CONFIGURATION



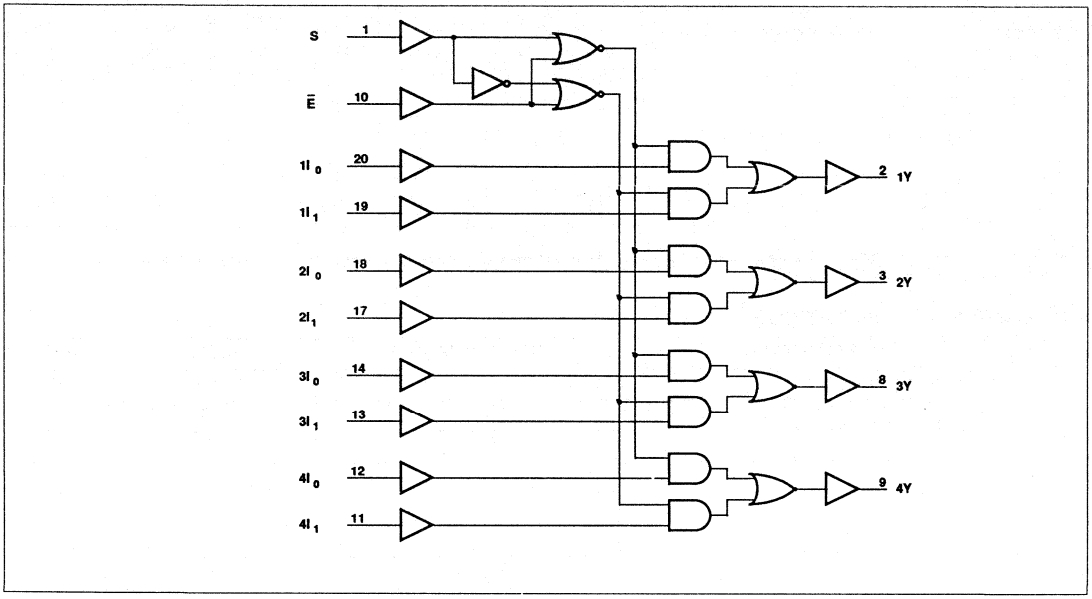
LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



LOGIC DIAGRAM



PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
1	S	Common select input
20, 18, 14, 12	$1I_0$ - $4I_0$	Data inputs
19, 17, 13, 11	$1I_1$ - $4I_1$	Data inputs
2, 3, 8, 9	1Y - 4Y	Data outputs
10	$\overline{E}$	Output enable input
4, 5, 6, 7	GND	Ground (0V)
15, 16	V_{CC}	Positive supply voltage

FUNCTION TABLE

ENABLE	SELECT INPUT	DATA INPUTS		OUTPUT
$\overline{E}$	S	nI_0	nI_1	nY
H	X	X	X	L
L	L	L	X	L
L	L	H	X	H
L	H	X	L	L
L	H	X	H	H

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	74AC11157			74ACT11157			UNIT
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	DC supply voltage	3.0[1]	5.0	5.5	4.5	5.0	5.5	V
V_I	Input voltage	0		V_{CC}	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	0		V_{CC}	V
$\Delta t/\Delta v$	Input transition rise or fall rate	0		10	0			ns/V
T_A	Operating free-air temperature	-40		+85	-40		+85	°C

NOTE:
1. No electrical or switching characteristics are specified at $V_{CC} < 3V$. Operation between 2V and 3V is not recommended, but within that range, a device output will maintain a previously established logic state.

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	TEST CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 to+7.0	V
I_{IK} or V_I	DC input diode current[2]	$V_I < 0$	-20	mA
		$V_I > V_{CC}$	20	
	DC input voltage		-0.5 to V_{CC} +0.5	V
I_{OK} or V_O	DC output diode current[2]	$V_O < 0$	-50	mA
		$V_O > V_{CC}$	50	
	DC output voltage		-0.5 to V_{CC} +0.5	V
I_O	DC output source or sink current per output pin	V_O = 0 to V_{CC}	±50	mA
I_{CC} or I_{GND}	DC V_{CC} current		±100	mA
	DC ground current		±100	
T_{STG}	Storage temperature		-65 to 150	°C
P_{TOT}	Power dissipation per package Plastic DIP	Above 70°C:derate linearly by 8mW/K	500	mW
	Power dissipation per package Plastic surface mount (SO)	Above 70°C:derate linearly by 6mW/K	400	mW

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		V_{CC}	74AC11157				74ACT11157				UNIT
					T_A = +25°C		T_A = -40°C to +85°C		T_A = +25°C		T_A = -40°C to +85°C		
				V	Min	Max	Min	Max	Min	Max	Min	Max	
V_{IH}	High-level input voltage			3.0	2.10		2.10						V
				4.5	3.15		3.15		2.0		2.0		
				5.5	3.85		3.85		2.0		2.0		
V_{IL}	Low-level input voltage			3.0		0.90		0.90					V
				4.5		1.35		1.35		0.8		0.8	
				5.5		1.65		1.65		0.8		0.8	
V_{OH}	High-level output voltage	V_I = V_{IL} or V_{IH}	I_{OH} = -50µA	3.0	2.9		2.9						V
				4.5	4.4		4.4		4.4		4.4		
				5.5	5.4		5.4		5.4		5.4		
			I_{OH} = -4mA	3.0	2.58		2.48						
			I_{OH} = -24mA	4.5	3.94		3.8		3.94		3.8		
				5.5	4.94		4.8		4.94		4.8		
			I_{OH} = -75mA[1]	5.5			3.85				3.85		
V_{OL}	Low-level output voltage	V_I = V_{IL} or V_{IH}	I_{OL} = 50µA	3.0		0.1		0.1					V
				4.5		0.1		0.1		0.1		0.1	
				5.5		0.1		0.1		0.1		0.1	
			I_{OL} = 12mA	3.0		0.36		0.44					
			I_{OL} = 24mA	4.5		0.36		0.44		0.36		0.44	
				5.5		0.36		0.44		0.36		0.44	
			I_{OL} = 75mA[1]	5.5				1.65				1.65	
I_I	Input leakage current	V_I = V_{CC} or GND		5.5		±0.1		±1.0		±0.1		±1.0	µA
I_{CC}	Quiescent supply current	V_I = V_{CC} or GND, I_O = 0		5.5		8.0		80		8.0		80	µA
ΔI_{CC}	Supply current, TTL inputs High[2]	One input at 3.4V, other inputs at V_{CC} or GND		5.5						0.9		1.0	mA

NOTES:
1. Not more than one output should be tested at a time, and the duration of the test should not exceed 10ms.
2. This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0V or V_{CC}.

74AC/ACT11158

Quad 2-Input Multiplexer; INV

AC11158: Product Specification
ACT11158: Preliminary Specification

FEATURES

- **Output capability: ±24 mA**
- **CMOS (AC) and TTL (ACT) voltage level inputs**
- **50Ω incident wave switching**
- **Center-pin V_{CC} and ground configuration to minimize high-speed switching noise**
- **I_{CC} category: MSI**

DESCRIPTION

The 74AC/ACT11158 high-performance CMOS devices combine very high speed and high output drive comparable to the most advanced TTL families.

The 74AC/ACT11158 provides four 2-to-1 multiplexers with a common selector and a common enable. The state of the Select (S) input determines the particular register from which the data comes. The Enable ($\overline{E}$) input is active-Low. When $\overline{E}$ is High, all of the inverting outputs ($\overline{Y}$) are forced High regardless of all other input conditions.

The device is the logic implementation of a 4-pole, 2 position switch where the position of the switch is determined by the logic levels supplied to the Select input.

GENERAL INFORMATION

SYMBOL	PARAMETER	CONDITIONS T_A = 25°C; GND = 0V; V_{CC} = 5.0V	TYPICAL		UNIT
			AC	ACT	
t_{PLH}/ t_{PHL}	Propagation delay nI_0, nI_1 to $n\overline{Y}$	C_L = 50pF	3.9	5.5	ns
C_{PD}	Power dissipation capacitance per mulitplexer[1]	f = 1MHz; C_L = 50pF	33	.5	pF
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	4.0	4.0	pF
I_{LATCH}	Latch-up current	Per Jedec JC40.2 Standard 17	500	500	mA

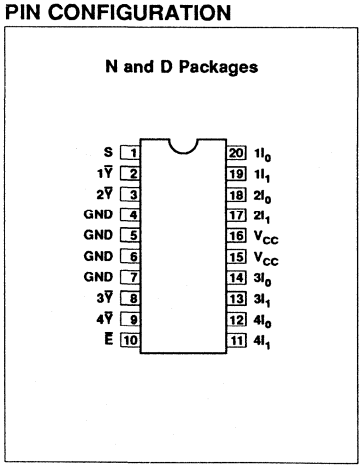
Note:

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_I + \Sigma (C_L \times V_{CC}^2 \times f_O)$ where:
   f_I = input frequency in MHz, C_L = output load capacitance in pF,
   f_O = output frequency in MHz, V_{CC} = supply voltage in V,
   $\Sigma (C_L \times V_{CC}^2 \times f_O)$ = sum of outputs

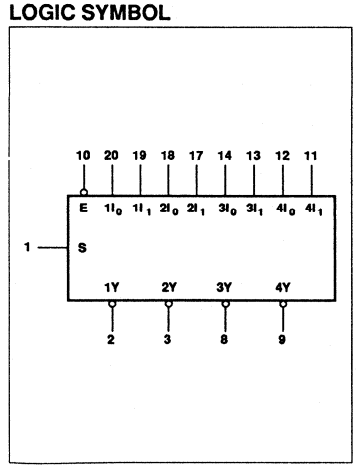
ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE
20-pin plastic DIP (300mil-wide)	-40°C to +85°C	74AC11158N 74ACT11158N
20-pin plastic SO (300mil-wide)	-40°C to +85°C	74AC11158D 74ACT11158D

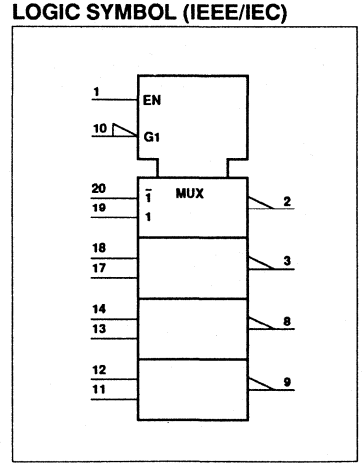
PIN CONFIGURATION



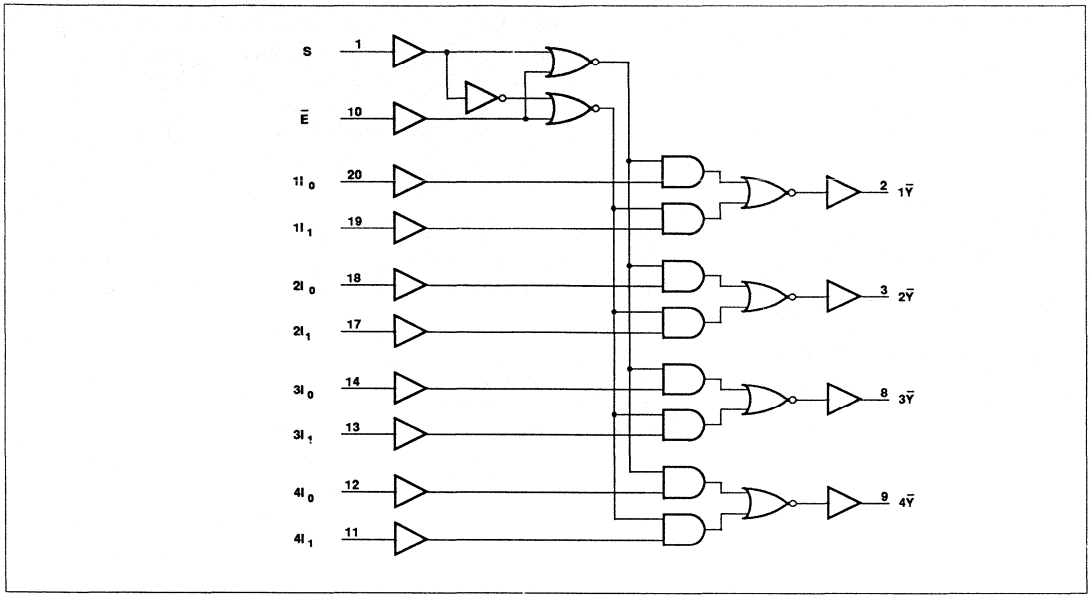
LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



LOGIC DIAGRAM



PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
1	S	Common select input
20, 18, 14, 12	nI_0 - nI_0	Data inputs
19, 17, 13, 11	nI_1 - nI_1	Data inputs
2, 3, 8, 9	$1\overline{Y}$ - $4\overline{Y}$	Data outputs
10	$\overline{E}$	Output enable input
4, 5, 6, 7	GND	Ground (0V)
15, 16	V_{CC}	Positive supply voltage

FUNCTION TABLE

ENABLE	SELECT INPUT	DATA INPUTS		OUTPUT
$\overline{E}$	S	nI_0	nI_1	$n\overline{Y}$
H	X	X	X	H
L	L	L	X	H
L	L	H	X	L
L	H	X	L	H
L	H	X	H	L

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		74AC11158			74ACT11158			UNIT
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	DC supply voltage		3.0[1]	5.0	5.5	4.5	5.0	5.5	V
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
$\Delta t/\Delta v$	Input transition rise or fall rate	Data	0		10	0			ns/V
		Select and Enable	0		5	0			
T_A	Operating free-air temperature		-40		+85	-40		+85	°C

NOTE:

1. No electrical or switching characteristics are specified at $V_{CC} < 3V$. Operation between 2V and 3V is not recommended, but within that range, a device output will maintain a previously established logic state.

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	TEST CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 to+7.0	V
I_{IK} or V_I	DC input diode current[2]	$V_I < 0$	-20	mA
		$V_I > V_{CC}$	20	
	DC input voltage		-0.5 to V_{CC} +0.5	V
I_{OK} or V_O	DC output diode current[2]	$V_O < 0$	-50	mA
		$V_O > V_{CC}$	50	
	DC output voltage		-0.5 to V_{CC} +0.5	V
I_O	DC output source or sink current per output pin	V_O = 0 to V_{CC}	±50	mA
I_{CC} or I_{GND}	DC V_{CC} current		±100	mA
	DC ground current		±100	
T_{STG}	Storage temperature		-65 to 150	°C
P_{TOT}	Power dissipation per package Plastic DIP	Above 70°C:derate linearly by 8mW/K	500	mW
	Power dissipation per package Plastic surface mount (SO)	Above 70°C:derate linearly by 6mW/K	400	mW

NOTES:

1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		V_{CC}	74AC11158				74ACT11158				UNIT
					T_A = +25°C		T_A = -40°C to +85°C		T_A = +25°C		T_A = -40°C to +85°C		
				V	Min	Max	Min	Max	Min	Max	Min	Max	
V_{IH}	High-level input voltage			3.0	2.10		2.10						V
				4.5	3.15		3.15		2.0		2.0		
				5.5	3.85		3.85		2.0		2.0		
V_{IL}	Low-level input voltage			3.0		0.90		0.90					V
				4.5		1.35		1.35		0.8		0.8	
				5.5		1.65		1.65		0.8		0.8	
V_{OH}	High-level output voltage	V_I = V_{IL} or V_{IH}	I_{OH} = -50μA	3.0	2.9		2.9						V
				4.5	4.4		4.4		4.4		4.4		
				5.5	5.4		5.4		5.4		5.4		
			I_{OH} = -4mA	3.0	2.58		2.48						
			I_{OH} = -24mA	4.5	3.94		3.8		3.94		3.8		
				5.5	4.94		4.8		4.94		4.8		
			I_{OH} = -75mA[1]	5.5			3.85				3.85		
V_{OL}	Low-level output voltage	V_I = V_{IL} or V_{IH}	I_{OL} = 50μA	3.0		0.1		0.1					V
				4.5		0.1		0.1		0.1		0.1	
				5.5		0.1		0.1		0.1		0.1	
			I_{OL} = 12mA	3.0		0.36		0.44					
			I_{OL} = 24mA	4.5		0.36		0.44		0.36		0.44	
				5.5		0.36		0.44		0.36		0.44	
			I_{OL} = 75mA[1]	5.5				1.65				1.65	
I_I	Input leakage current	V_I = V_{CC} or GND		5.5		±0.1		±1.0		±0.1		±1.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC} or GND, I_O = 0		5.5		8.0		80		8.0		80	μA
ΔI_{CC}	Supply current, TTL inputs High[2]	One input at 3.4V, other inputs at V_{CC} or GND		5.5						0.9		1.0	mA

NOTES:
1. Not more than one output should be tested at a time, and the duration of the test should not exceed 10ms.
2. This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0V or V_{CC}.

AC ELECTRICAL CHARACTERISTICS AT 3.3V ±0.3V

SYMBOL	PARAMETER	WAVEFORM	74AC11158					UNIT
			T_A = +25°C			T_A = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay nI_0, nI_1 to $n\overline{Y}$	1	1.5 1.5	5.8 5.9	7.3 7.6	1.5 1.5	8.0 8.4	ns
t_{PLH} t_{PHL}	Propagation delay S to $n\overline{Y}$	1	1.5 1.5	6.5 6.8	8.0 8.4	1.5 1.5	8.8 9.3	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{E}$ to $n\overline{Y}$	2	1.5 1.5	5.7 6.3	7.1 7.8	1.5 1.5	8.0 8.7	ns

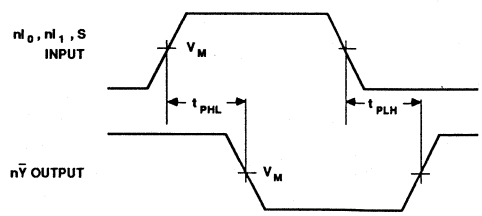
AC ELECTRICAL CHARACTERISTICS AT 5.0V ±0.5V

SYMBOL	PARAMETER	WAVEFORM	74AC11158					UNIT
			T_A = +25°C			T_A = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay nI_0, nI_1 to $n\overline{Y}$	1	1.5 1.5	3.6 3.9	5.4 5.6	1.5 1.5	5.8 6.4	ns
t_{PLH} t_{PHL}	Propagation delay S to $n\overline{Y}$	1	1.5 1.5	4.1 4.4	5.9 6.2	1.5 1.5	6.4 6.9	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{E}$ to $n\overline{Y}$	2	1.5 1.5	3.7 4.2	5.4 5.9	1.5 1.5	5.9 6.5	ns

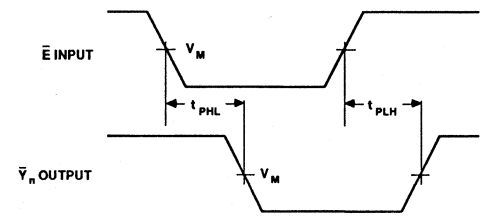
AC ELECTRICAL CHARACTERISTICS AT 5.0V ±0.5V

SYMBOL	PARAMETER	WAVEFORM	74ACT11158					UNIT
			T_A = +25°C			T_A = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay nI_0, nI_1 to $n\overline{Y}$	1	1.5 1.5			1.5 1.5		ns
t_{PLH} t_{PHL}	Propagation delay S to $n\overline{Y}$	1	1.5 1.5			1.5 1.5		ns
t_{PLH} t_{PHL}	Propagation delay $\overline{E}$ to $n\overline{Y}$	2	1.5 1.5			1.5 1.5		ns

AC WAVEFORMS



Waveform 1. Waveforms Showing the Data Inputs (nI_0, nI_1) and Select Input (S) to Output ($n\overline{Y}$) Propagation Delays

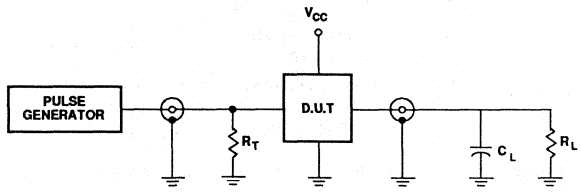


Waveform 2. Waveforms Showing the Enable Input ($\overline{E}$) to Output ($n\overline{Y}$) Propagation Delays

WAVEFORM CONDITIONS

	INPUTS	OUTPUTS
AC	V_{IN} = GND to V_{CC}, V_M = 50% V_{CC}	V_{OUT} = V_{OL} to V_{OH}
ACT	V_{IN} = GND to 3.0V, V_M = 1.5V	V_M = 50% V_{CC}

TEST CIRCUIT



Test Circuit

DEFINITIONS

C_L = Load capacitance, 50pF; includes jig and probe capacitance

R_L = Load resistor, 500Ω

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators

Input pulses: PRR ≤ 10MHz

$t_r = t_f$ = 3ns

74AC/ACT11160

Synchronous Presettable Synchronous BCD Decade Counter; Asynchronous Reset

AC11160: Product Specification
ACT11160: Objective Specification

FEATURES

- **Synchronous counting and loading**
- **Two count enable inputs for n-bit cascading**
- **Positive edge-triggered clock**
- **Asynchronous reset**
- **Output capability: ±24mA**
- **CMOS (AC) and TTL (ACT) voltage level inputs**
- **50Ω incident wave switching**
- **Center-pin V_{CC} and ground configuration to minimize high-speed switching noise**
- **I_{CC} category: MSI**

DESCRIPTION

The 74AC/ACT11160 high-performance CMOS devices combine very high speed and high output drive comparable to the most advanced TTL families.

The 74AC/ACT11160 4-bit synchronous presettable decade counters feature an internal carry look-ahead and can be used for high-speed counting. Synchronous operation is provided by having all flip-flops clocked simultaneously on the positive-going edge of the clock.

GENERAL INFORMATION

SYMBOL	PARAMETER	CONDITIONS T_A = 25°C; GND = 0V; V_{CC} = 5.0V	TYPICAL		UNIT
			AC	ACT	
t_{PLH}/ t_{PHL}	Propagation delay CP_n to Q_n ($\overline{PE}$ = High)	C_L = 50pF	6.9	8.3	ns
C_{PD}	Power dissipation capacitance[1]	f = 1MHz; C_L = 50pF	48	54	pF
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	4.0	4.0	pF
I_{LATCH}	Latch-up current	Per Jedec JC40.2 Standard 17	500	500	mA
f_{MAX}	Maximum clock frequency	C_L = 50pF	140	125	MHz

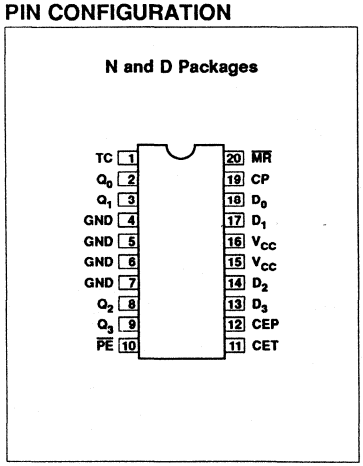
Note:

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_I + \Sigma (C_L \times V_{CC}^2 \times f_O)$ where:
   f_I = input frequency in MHz, C_L = output load capacitance in pF,
   f_O = output frequency in MHz, V_{CC} = supply voltage in V,
   $\Sigma (C_L \times V_{CC}^2 \times f_O)$ = sum of outputs

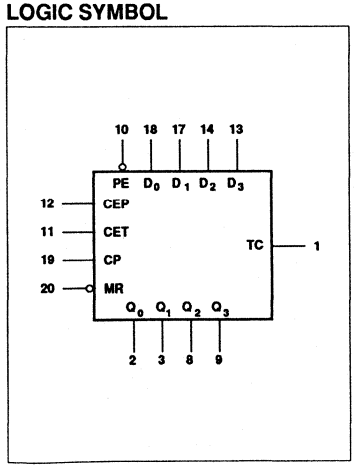
ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE
20-pin plastic DIP (300mil-wide)	-40°C to +85°C	74AC11160N 74ACT11160N
20-pin plastic SO (300mil-wide)	-40°C to +85°C	74AC11160D 74ACT11160D

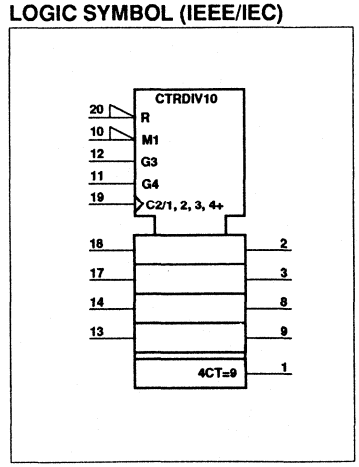
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



Synchronous Presettable Synchronous BCD Decade Counter; Asynchronous Reset

74AC/ACT11160

The outputs of the counters may be preset to High or Low levels. A Low level at the Parallel Enable ($\overline{PE}$) input disables the counting action and causes the data at the D_0 - D_3 inputs to be loaded into the counter on the rising edge of the clock. Preset takes place regardless of the levels at Count Enable (CEP, CET) inputs.

A Low level at the Master Reset ($\overline{MR}$) input sets all four outputs of the flip-flops (Q_0 - Q_3) to Low levels, regardless of the levels at CP, $\overline{PE}$, CET, and CEP inputs (thus providing an asynchronous clear function).

The carry look-ahead simplifies serial cascading of the counters. Both Count Enable inputs (CEP and CET) must be High to count. The CET input is fed forward to enable the Terminal Count (TC) output. The TC output thus enabled will produce a High output pulse of a duration approximately equal to the High level output of Q_0. This pulse can be used to enable the next cascaded stage.

PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
20	$\overline{MR}$	Asynchronous master reset (active Low)
19	CP	Clock input (Low-to-High, edge-triggered)
18, 17, 14, 13	D_0 - D_3	Data inputs
12	CEP	Count enable input
10	$\overline{PE}$	Parallel enable input (active Low)
11	CET	Count enable carry input
18, 17, 14, 13	Q_0 - Q_3	Counter outputs
1	TC	Terminal count output
4, 5, 6, 7	GND	Ground (0V)
15, 16	V_{CC}	Positive supply voltage

FUNCTION TABLE

OPERATING MODE	INPUTS						OUTPUTS	
	$\overline{MR}$	CP	CEP	CET	$\overline{PE}$	D_n	Q_n	TC
Reset (clear)	L	X	X	X	X	X	L	L
Parallel load	H	↑	X	X	l	l	L	L
	H	↑	X	X	l	h	H	(1)
Count	H	↑	h	h	h	X	count	(1)
Hold (do nothing)	H	X	l	X	h	X	q_n	(1)
	H	X	X	l	h	X	q_n	L

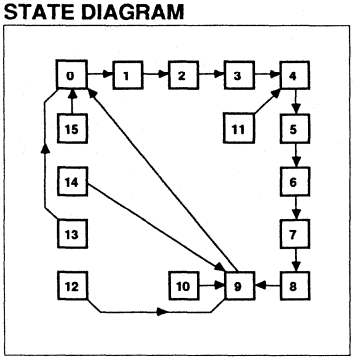
H = High voltage level
L = Low voltage level
h = High voltage level one setup time prior to the Low-to High clock transition
l = Low voltage level one setup time prior to the Low-to High clock transition
X = Don't care
q = State of the referenced output prior to the Low-to High clock transition
↑ = Low-to-High clock transition

NOTE:
1. The TC output is High when CET is High and the counter is at Terminal Count (HLLH).

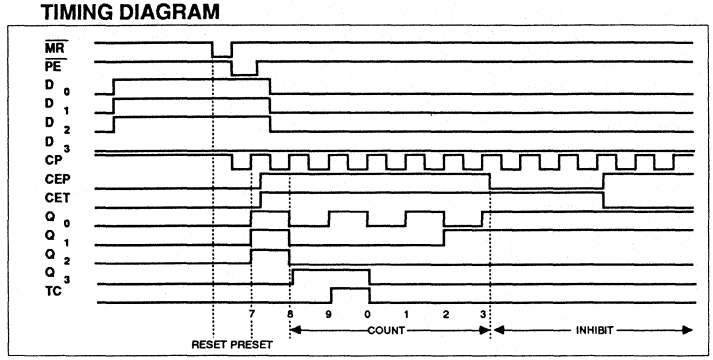
Synchronous Presettable Synchronous BCD Decade Counter; Asynchronous Reset

74AC/ACT11160

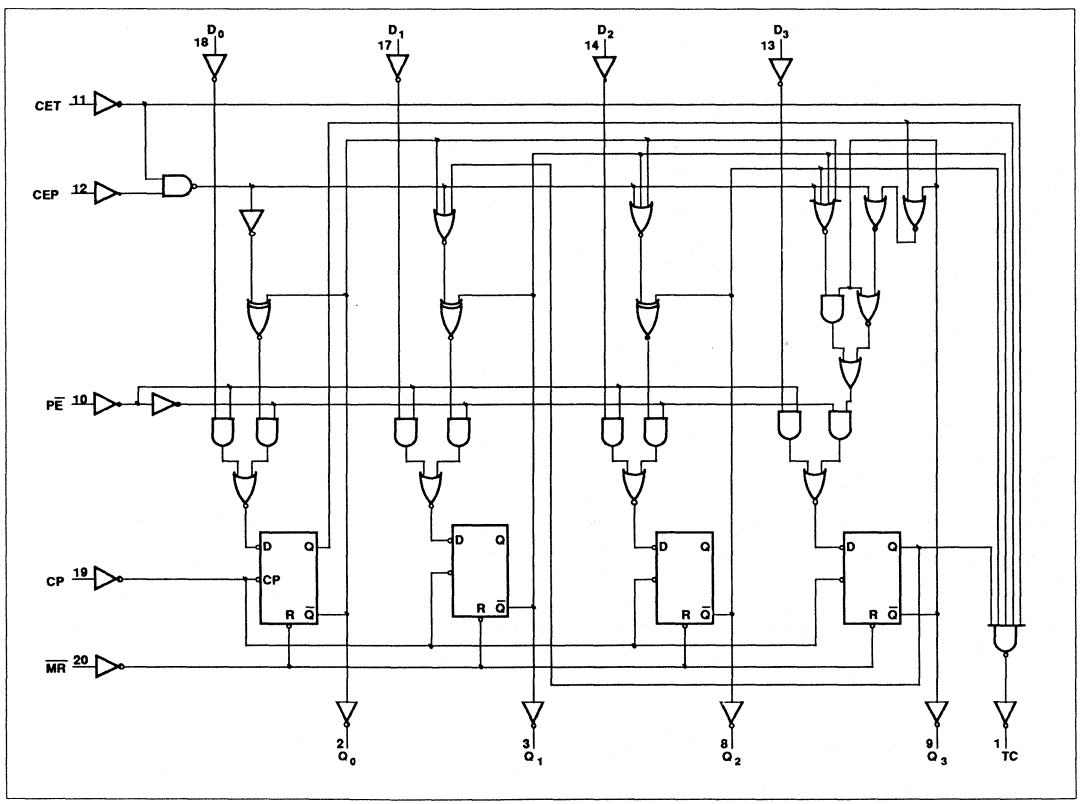
STATE DIAGRAM



TIMING DIAGRAM



LOGIC DIAGRAM



RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	74AC11160			74ACT11160			UNIT
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	DC supply voltage	3.0[1]	5.0	5.5	4.5	5.0	5.5	V
V_I	Input voltage	0		V_{CC}	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	0		V_{CC}	V
$\Delta t/\Delta v$	Input transition rise or fall rate	0		10	0		10	ns/V
T_A	Operating free-air temperature	-40		+85	-40		+85	°C

NOTE:
1. No electrical or switching characteristics are specified at $V_{CC} < 3V$. Operation between 2V and 3V is not recommended, but within that range, a device output will maintain a previously established logic state.

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	TEST CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 to+7.0	V
I_{IK} or V_I	DC input diode current[2]	$V_I < 0$	-20	mA
		$V_I > V_{CC}$	20	
	DC input voltage		-0.5 to V_{CC} +0.5	V
I_{OK} or V_O	DC output diode current[2]	$V_O < 0$	-50	mA
		$V_O > V_{CC}$	50	
	DC output voltage		-0.5 to V_{CC} +0.5	V
I_O	DC output source or sink current per output pin	V_O = 0 to V_{CC}	±50	mA
I_{CC} or I_{GND}	DC V_{CC} current		±125	mA
	DC ground current		±125	
T_{STG}	Storage temperature		-65 to 150	°C
P_{TOT}	Power dissipation per package Plastic DIP	Above 70°C:derate linearly by 8mW/K	500	mW
	Power dissipation per package Plastic surface mount (SO)	Above 70°C:derate linearly by 6mW/K	400	mW

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

Synchronous Presettable Synchronous BCD Decade Counter; Asynchronous Reset

74AC/ACT11160

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		V_{CC}	74AC11160				74ACT11160				UNIT
					T_A = +25°C		T_A = -40°C to +85°C		T_A = +25°C		T_A = -40°C to +85°C		
				V	Min	Max	Min	Max	Min	Max	Min	Max	
V_{IH}	High-level input voltage			3.0	2.10		2.10						V
				4.5	3.15		3.15		2.0		2.0		
				5.5	3.85		3.85		2.0		2.0		
V_{IL}	Low-level input voltage			3.0		0.90		0.90					V
				4.5		1.35		1.35		0.8		0.8	
				5.5		1.65		1.65		0.8		0.8	
V_{OH}	High-level output voltage	V_I = V_{IL} or V_{IH}	I_{OH} = -50μA	3.0	2.9		2.9						V
				4.5	4.4		4.4		4.4		4.4		
				5.5	5.4		5.4		5.4		5.4		
			I_{OH} = -4mA	3.0	2.58		2.48						
			I_{OH} = -24mA	4.5	3.94		3.8		3.94		3.8		
				5.5	4.94		4.8		4.94		4.8		
			I_{OH} = -75mA[1]	5.5			3.85				3.85		
V_{OL}	Low-level output voltage	V_I = V_{IL} or V_{IH}	I_{OL} = 50μA	3.0		0.1		0.1					V
				4.5		0.1		0.1		0.1		0.1	
				5.5		0.1		0.1		0.1		0.1	
			I_{OL} = 12mA	3.0		0.36		0.44					
			I_{OL} = 24mA	4.5		0.36		0.44		0.36		0.44	
				5.5		0.36		0.44		0.36		0.44	
			I_{OL} = 75mA[1]	5.5				1.65				1.65	
I_I	Input leakage current	V_I = V_{CC} or GND		5.5		±0.1		±1.0		±0.1		±1.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC} or GND, I_O = 0		5.5		8.0		80		8.0		80	μA
ΔI_{CC}	Supply current, TTL inputs High[2]	One input at 3.4V, other inputs at V_{CC} or GND		5.5						0.9		1.0	mA

NOTES:
1. Not more than one output should be tested at a time, and the duration of the test should not exceed 10ms.
2. This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0V or V_{CC}.

Synchronous Presettable Synchronous BCD Decade Counter; Asynchronous Reset

74AC/ACT11160

AC ELECTRICAL CHARACTERISTICS AT 3.3V ±0.3V

SYMBOL	PARAMETER	WAVEFORM	74AC11160					UNIT
			T_A = +25°C			T_A = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	1	66	90		66		MHz
t_{PLH} t_{PHL}	Propagation delay CP to Q_n ($\overline{PE}$ = "H")	1	1.5 1.5	9.0 10.6	11.2 13.4	1.5 1.5	12.5 15.1	ns
t_{PLH} t_{PHL}	Propagation delay CP to Q_n ($\overline{PE}$ = "L")	1	1.5 1.5	8.6 10.1	10.8 12.8	1.5 1.5	12.1 14.4	ns
t_{PLH} t_{PHL}	Propagation delay CP to TC	1	1.5 1.5	11.2 12.2	13.6 15.1	1.5 1.5	15.2 17.2	ns
t_{PLH} t_{PHL}	Propagation delay CET to TC	3	1.5 1.5	6.0 6.8	7.6 8.9	1.5 1.5	8.3 9.9	ns
t_{PHL}	Propagation delay $\overline{MR}$ to Q_n	2	1.5	12.0	15.2	1.5	17.3	ns
t_{PHL}	Propagation delay $\overline{MR}$ to TC	2	1.5	14.1	17.3	1.5	19.7	ns
t_S	Setup time, High or Low D_n to CP	4	6.5			6.5		ns
t_H	Hold time, High or Low D_n to CP	4	1.0			1.0		ns
t_S	Setup time, High or Low $\overline{PE}$ to CP	4	6.5			6.5		ns
t_H	Hold time, High or Low $\overline{PE}$ to CP	4	1.0			1.0		ns
t_S	Setup time, High or Low CEP or CET to CP	5	6.0			6.0		ns
t_H	Hold time, High or Low CEP or CET to CP	5	1.0			1.0		ns
t_W	Clock pulse width (load) High or Low	1	7.5			7.5		ns
t_W	Clock pulse width (count) High or Low	1	7.5			7.5		ns
t_W	$\overline{MR}$ pulse width, Low	2	6.0			6.0		ns
t_{REC}	Recovery time $\overline{MR}$ to CP	2	6.0			6.0		ns

AC ELECTRICAL CHARACTERISTICS AT 5.0V ±0.5V

SYMBOL	PARAMETER	WAVEFORM	74AC11160					UNIT
			T_A = +25°C			T_A = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	1	110	140		110		MHz
t_{PLH} t_{PHL}	Propagation delay CP to Q_n ($\overline{PE}$ = "H")	1	1.5 1.5	6.3 7.4	8.0 9.8	1.5 1.5	8.9 11.2	ns
t_{PLH} t_{PHL}	Propagation delay CP to Q_n ($\overline{PE}$ = "L")	1	1.5 1.5	6.0 7.1	7.5 9.4	1.5 1.5	8.4 10.7	ns
t_{PLH} t_{PHL}	Propagation delay CP to TC	1	1.5 1.5	7.8 8.5	9.5 10.6	1.5 1.5	10.7 12.1	ns
t_{PLH} t_{PHL}	Propagation delay CET to TC	3	1.5 1.5	4.2 5.0	5.5 6.7	1.5 1.5	6.0 7.5	ns
t_{PHL}	Propagation delay $\overline{MR}$ to Q_n	2	1.5	8.2	10.7	1.5	12.1	ns
t_{PHL}	Propagation delay $\overline{MR}$ to TC	2	1.5	9.9	12.2	1.5	13.8	ns
t_S	Setup time, High or Low D_n to CP	4	3.5			3.5		ns
t_H	Hold time, High or Low D_n to CP	4	1.0			1.0		ns
t_S	Setup time, High or Low $\overline{PE}$ to CP	4	6.5			6.5		ns
t_H	Hold time, High or Low $\overline{PE}$ to CP	4	1.0			1.0		ns
t_S	Setup time, High or Low CEP or CET to CP	5	4.5			4.5		ns
t_H	Hold time, High or Low CEP or CET to CP	5	1.0			1.0		ns
t_W	Clock pulse width (load) High or Low	1	4.5			4.5		ns
t_W	Clock pulse width (count) High or Low	1	4.5			4.5		ns
t_W	$\overline{MR}$ pulse width, Low	2	4.5			4.5		ns
t_{REC}	Recovery time $\overline{MR}$ to CP	2	6.0			6.0		ns

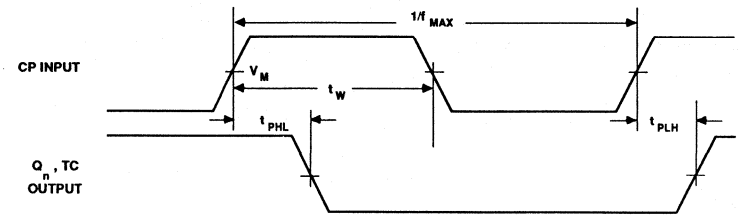
Synchronous Presettable Synchronous BCD Decade Counter; Asynchronous Reset

74AC/ACT11160

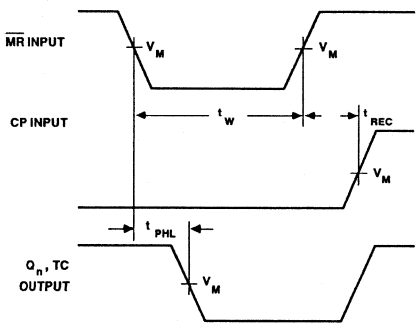
AC ELECTRICAL CHARACTERISTICS AT 5.0V ±0.5V

SYMBOL	PARAMETER	WAVEFORM	74ACT11160					UNIT
			T_A = +25°C			T_A = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	1						MHz
t_{PLH} t_{PHL}	Propagation delay CP to Q_n ($\overline{PE}$ = "H")	1	1.5 1.5			1.5 1.5		ns
t_{PLH} t_{PHL}	Propagation delay CP to Q_n ($\overline{PE}$ = "L")	1	1.5 1.5			1.5 1.5		ns
t_{PLH} t_{PHL}	Propagation delay CP to TC	1	1.5 1.5			1.5 1.5		ns
t_{PLH} t_{PHL}	Propagation delay CET to TC	3	1.5 1.5			1.5 1.5		ns
t_{PHL}	Propagation delay $\overline{MR}$ to Q_n	2	1.5			1.5		ns
t_{PHL}	Propagation delay $\overline{MR}$ to TC	2	1.5			1.5		ns
t_S	Setup time, High or Low D_n to CP	4						ns
t_H	Hold time, High or Low D_n to CP	4						ns
t_S	Setup time, High or Low $\overline{PE}$ to CP	4						ns
t_H	Hold time, High or Low $\overline{PE}$ to CP	4						ns
t_S	Setup time, High or Low CEP or CET to CP	5						ns
t_H	Hold time, High or Low CEP or CET to CP	5						ns
t_W	Clock pulse width (load) High or Low	1						ns
t_W	Clock pulse width (count) High or Low	1						ns
t_W	$\overline{MR}$ pulse width, Low	2						ns
t_{REC}	Recovery time $\overline{MR}$ to CP	2						ns

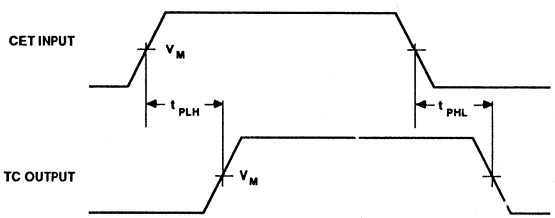
AC WAVEFORMS



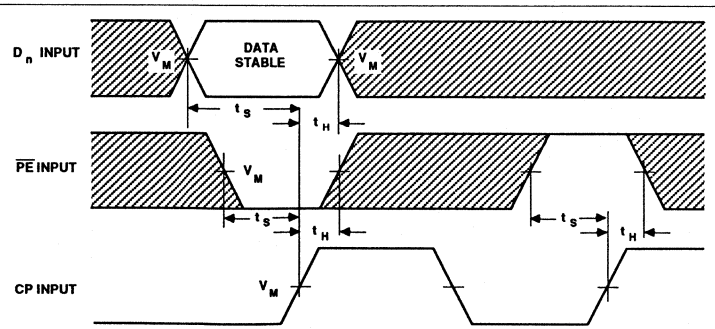
Waveform 1. Waveforms Showing Clock to Outputs Propagation Delays and Clock Pulse Width



Waveform 2. Waveforms Showing the Master Reset ($\overline{MR}$) Pulse Width, the Master Reset to Output (Qn, TC) Propagation Delays, and the Master Reset to Clock (CP) Recovery Time



Waveform 3. Waveforms Showing the Input (CET) to Output (TC) Propagation Delays

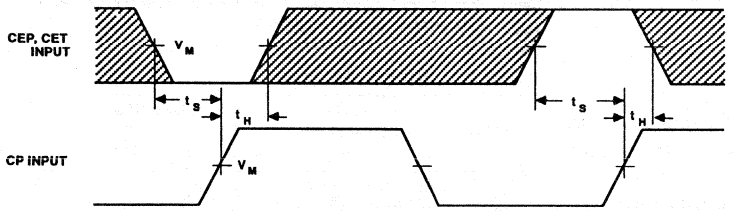


Waveform 4. Waveforms Showing the Data Set-up and Hold Times for the Input (D_n) and Parallel Enable Input $\overline{PE}$

Synchronous Presettable Synchronous BCD Decade Counter; Asynchronous Reset

74AC/ACT11160

AC WAVEFORMS (Continued)

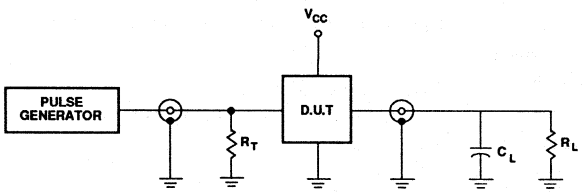


Waveform 5. Waveforms Showing CEP and CET Set-up and Hold Times

WAVEFORM CONDITIONS

	INPUTS	OUTPUTS
AC	V_{IN} = GND to V_{CC}, V_M = 50% V_{CC}	$V_{OUT} = V_{OL}$ to V_{OH}
ACT	V_{IN} = GND to 3.0V, V_M = 1.5V	V_M = 50% V_{CC}

TEST CIRCUIT



Test Circuit

DEFINITIONS

C_L = Load capacitance, 50pF; includes jig and probe capacitance

R_L = Load resistor, 500Ω

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators

Input pulses: PRR ≤ 10MHz

$t_r = t_f$ = 3ns

74AC/ACT11161

Synchronous Presettable Synchronous 4-Bit Binary Counter; Asynchronous Reset

Objective Specification

FEATURES

- **Synchronous counting and loading**
- **Two count enable inputs for n-bit cascading**
- **Positive edge-triggered clock**
- **Asynchronous reset**
- **Output capability: ±24mA**
- **CMOS (AC) and TTL (ACT) voltage level inputs**
- **50Ω incident wave switching**
- **Center-pin V_{CC} and ground configuration to minimize high-speed switching noise**
- **I_{CC} category: MSI**

DESCRIPTION

The 74AC/ACT11161 high-performance CMOS devices combine very high speed and high output drive comparable to the most advanced TTL families.

The 74AC/ACT11161 4-bit synchronous presettable binary counters feature an internal carry look-ahead and can be used for high-speed counting. Synchronous operation is provided by having all flip-flops clocked simultaneously on the positive-going edge of the clock.

GENERAL INFORMATION

SYMBOL	PARAMETER	CONDITIONS T_A = 25°C; GND = 0V; V_{CC} = 5.0V	TYPICAL AC	TYPICAL ACT	UNIT
t_{PLH}/ t_{PHL}	Propagation delay CP_n to Q_n ($\overline{PE}$ = High)	C_L = 50pF	7.5	8.8	ns
C_{PD}	Power dissipation capacitance[1]	f = 1MHz; C_L = 50pF	54	60	pF
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	4.0	4.0	pF
I_{LATCH}	Latch-up current	Per Jedec JC40.2 Standard 17	500	500	mA
f_{MAX}	Maximum clock frequency	C_L = 50pF	125	125	MHz

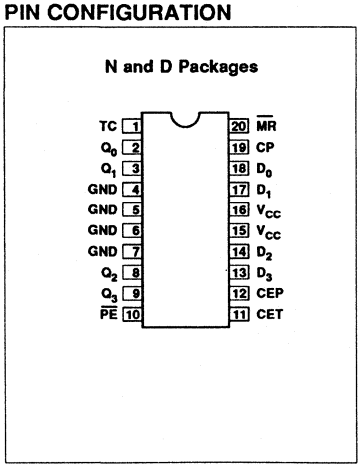
Note:

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_I + \Sigma (C_L \times V_{CC}^2 \times f_O)$ where:
   f_I = input frequency in MHz, C_L = output load capacitance in pF,
   f_O = output frequency in MHz, V_{CC} = supply voltage in V,
   $\Sigma (C_L \times V_{CC}^2 \times f_O)$ = sum of outputs

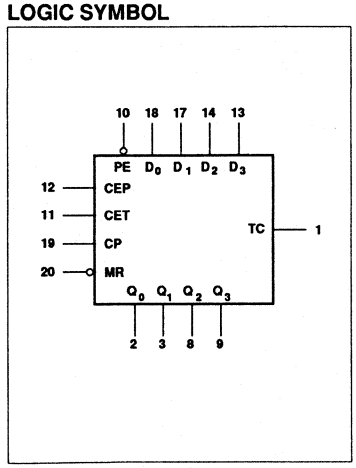
ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE
20-pin plastic DIP (300mil-wide)	-40°C to +85°C	74AC11161N 74ACT11161N
20-pin plastic SO (300mil-wide)	-40°C to +85°C	74AC11161D 74ACT11161D

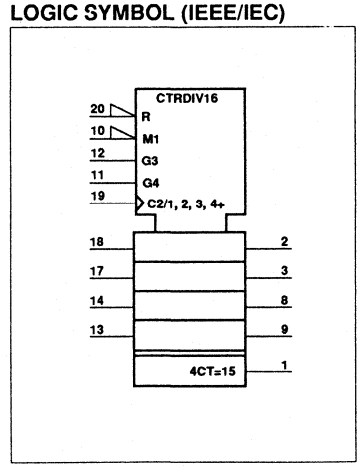
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



Synchronous Presettable Synchronous 4-Bit Binary Counter; Asynchronous Reset

74AC/ACT11161

The outputs of the counters may be preset to High or Low levels. A Low level at the Parallel Enable ($\overline{PE}$) input disables the counting action and causes the data at the D_0 - D_3 inputs to be loaded into the counter on the rising edge of the clock. Preset takes place regardless of the levels at Count Enable (CEP, CET) inputs.

A Low level at the Master Reset ($\overline{MR}$) input sets all four outputs of the flip-flops (Q_0 - Q_3) to Low levels, regardless of the levels at CP, $\overline{PE}$, CET, and CEP inputs (thus providing an asynchronous clear function).

The carry look-ahead simplifies serial cascading of the counters. Both Count Enable inputs (CEP and CET) must be High to count. The CET input is fed forward to enable the Terminal Count (TC) output. The TC output thus enabled will produce a High output pulse of a duration approximately equal to the High level output of Q_0. This pulse can be used to enable the next cascaded stage.

PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
20	$\overline{MR}$	Asynchronous master reset (active Low)
19	CP	Clock input (Low-to-High, edge-triggered)
18, 17, 14, 13	D_0 - D_3	Data inputs
12	CEP	Count enable input
10	$\overline{PE}$	Parallel enable input (active Low)
11	CET	Count enable carry input
18, 17, 14, 13	Q_0 - Q_3	Counter outputs
1	TC	Terminal count output
4, 5, 6, 7	GND	Ground (0V)
15, 16	V_{CC}	Positive supply voltage

FUNCTION TABLE

OPERATING MODE	INPUTS						OUTPUTS	
	$\overline{MR}$	CP	CEP	CET	$\overline{PE}$	D_n	Q_n	TC
Reset (clear)	L	X	X	X	X	X	L	L
Parallel load	H	↑	X	X	l	l	L	L
	H	↑	X	X	l	h	H	(1)
Count	H	↑	h	h	h	X	count	(1)
Hold (do nothing)	H	X	l	X	h	X	q_n	(1)
	H	X	X	l	h	X	q_n	L

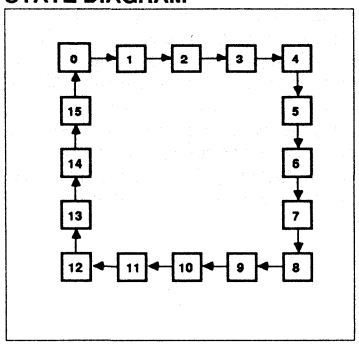
H = High voltage level
L = Low voltage level
h = High voltage level one setup time prior to the Low-to High clock transition
l = Low voltage level one setup time prior to the Low-to High clock transition
X = Don't care
q = State of the referenced output prior to the Low-to High clock transition
↑ = Low-to-High clock transition

NOTE:
1. The TC output is High when CET is High and the counter is at Terminal Count (HHHH).

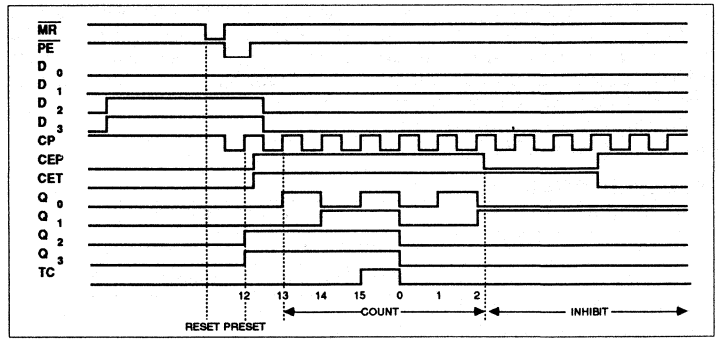
Synchronous Presettable Synchronous 4-Bit Binary Counter; Asynchronous Reset

74AC/ACT11161

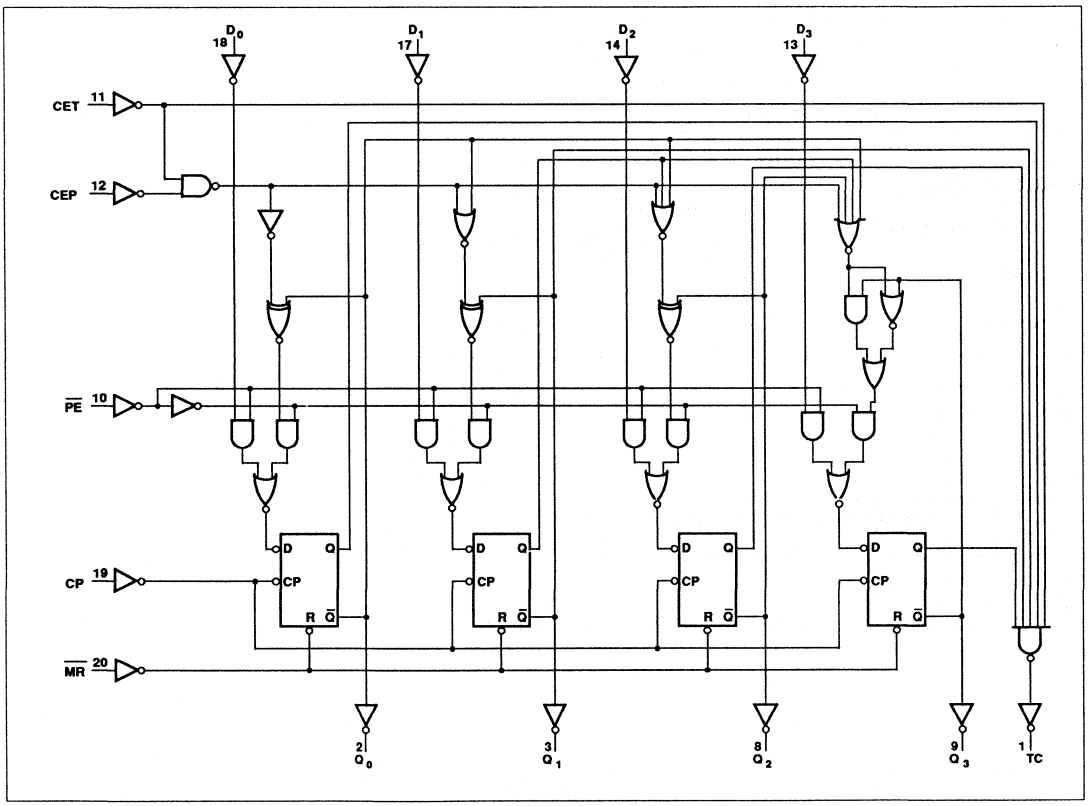
STATE DIAGRAM



TIMING DIAGRAM



LOGIC DIAGRAM



RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	74AC11161			74ACT11161			UNIT
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	DC supply voltage	3.0[1]	5.0	5.5	4.5	5.0	5.5	V
V_I	Input voltage	0		V_{CC}	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	0		V_{CC}	V
$\Delta t/\Delta v$	Input transition rise or fall rate	0		10	0		10	ns/V
T_A	Operating free-air temperature	-40		+85	-40		+85	°C

NOTE:

1. No electrical or switching characteristics are specified at $V_{CC} < 3V$. Operation between 2V and 3V is not recommended, but within that range, a device output will maintain a previously established logic state.

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	TEST CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 to+7.0	V
I_{IK} or V_I	DC input diode current[2]	$V_I < 0$	-20	mA
		$V_I > V_{CC}$	20	
	DC input voltage		-0.5 to V_{CC} +0.5	V
I_{OK} or V_O	DC output diode current[2]	$V_O < 0$	-50	mA
		$V_O > V_{CC}$	50	
	DC output voltage		-0.5 to V_{CC} +0.5	V
I_O	DC output source or sink current per output pin	V_O = 0 to V_{CC}	±50	mA
I_{CC} or I_{GND}	DC V_{CC} current		±125	mA
	DC ground current		±125	
T_{STG}	Storage temperature		-65 to 150	°C
P_{TOT}	Power dissipation per package Plastic DIP	Above 70°C:derate linearly by 8mW/K	500	mW
	Power dissipation per package Plastic surface mount (SO)	Above 70°C:derate linearly by 6mW/K	400	mW

NOTES:

1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		V_{CC}	74AC11161				74ACT11161				UNIT
					T_A = +25°C		T_A = -40°C to +85°C		T_A = +25°C		T_A = -40°C to +85°C		
				V	Min	Max	Min	Max	Min	Max	Min	Max	
V_{IH}	High-level input voltage			3.0	2.10		2.10						V
				4.5	3.15		3.15		2.0		2.0		
				5.5	3.85		3.85		2.0		2.0		
V_{IL}	Low-level input voltage			3.0		0.90		0.90					V
				4.5		1.35		1.35		0.8		0.8	
				5.5		1.65		1.65		0.8		0.8	
V_{OH}	High-level output voltage	V_I = V_{IL} or V_{IH}	I_{OH} = -50μA	3.0	2.9		2.9						V
				4.5	4.4		4.4		4.4		4.4		
				5.5	5.4		5.4		5.4		5.4		
			I_{OH} = -4mA	3.0	2.58		2.48						
			I_{OH} = -24mA	4.5	3.94		3.8		3.94		3.8		
				5.5	4.94		4.8		4.94		4.8		
			I_{OH} = -75mA[1]	5.5			3.85				3.85		
V_{OL}	Low-level output voltage	V_I = V_{IL} or V_{IH}	I_{OL} = 50μA	3.0		0.1		0.1					V
				4.5		0.1		0.1		0.1		0.1	
				5.5		0.1		0.1		0.1		0.1	
			I_{OL} = 12mA	3.0		0.36		0.44					
			I_{OL} = 24mA	4.5		0.36		0.44		0.36		0.44	
				5.5		0.36		0.44		0.36		0.44	
			I_{OL} = 75mA[1]	5.5				1.65				1.65	
I_I	Input leakage current	V_I = V_{CC} or GND		5.5		±0.1		±1.0		±0.1		±1.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC} or GND, I_O = 0		5.5		8.0		80		8.0		80	μA
ΔI_{CC}	Supply current, TTL inputs High[2]	One input at 3.4V, other inputs at V_{CC} or GND		5.5						0.9		1.0	mA

NOTES:
1. Not more than one output should be tested at a time, and the duration of the test should not exceed 10ms.
2. This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0V or V_{CC}.

74AC/ACT11162

Synchronous Presettable BCD Decade Counter; Synchronous Reset

AC11162: Product Specification
ACT11162: Objective Specification

FEATURES

- **Synchronous counting and loading**
- **Two count enable inputs for n-bit cascading**
- **Positive edge-triggered clock**
- **Synchronous reset**
- **Output capability: ±24mA**
- **CMOS (AC) and TTL (ACT) voltage level inputs**
- **50Ω incident wave switching**
- **Center-pin V_{CC} and ground configuration to minimize high-speed switching noise**
- **I_{CC} category: MSI**

DESCRIPTION

The 74AC/ACT11162 high-performance CMOS devices combine very high speed and high output drive comparable to the most advanced TTL families.

The 74AC/ACT11162 4-bit synchronous presettable decade counters feature an internal carry look-ahead and can be used for high-speed counting. Synchronous operation is provided by having all flip-flops clocked simultaneously on the positive-going edge of the clock.

GENERAL INFORMATION

SYMBOL	PARAMETER	CONDITIONS T_A = 25°C; GND = 0V; V_{CC} = 5.0V	TYPICAL		UNIT
			AC	ACT	
t_{PLH}/ t_{PHL}	Propagation delay CP_n to Q_n ($\overline{PE}$ = High)	C_L = 50pF	6.9	8.8	ns
C_{PD}	Power dissipation capacitance[1]	f = 1MHz; C_L = 50pF	54	60	pF
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	4.0	4.0	pF
I_{LATCH}	Latch-up current	Per Jedec JC40.2 Standard 17	500	500	mA
f_{MAX}	Maximum clock frequency	C_L = 50pF	140	125	MHz

Note:

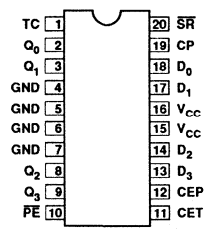
1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_I + \Sigma (C_L \times V_{CC}^2 \times f_O)$ where:
   f_I = input frequency in MHz, C_L = output load capacitance in pF,
   f_O = output frequency in MHz, V_{CC} = supply voltage in V,
   $\Sigma (C_L \times V_{CC}^2 \times f_O)$ = sum of outputs

ORDERING INFORMATION

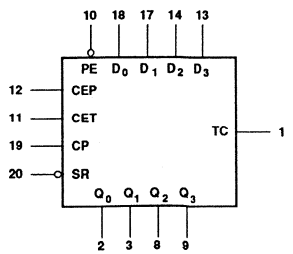
PACKAGES	TEMPERATURE RANGE	ORDER CODE
20-pin plastic DIP (300mil-wide)	-40°C to +85°C	74AC11162N 74ACT11162N
20-pin plastic SO (300mil-wide)	-40°C to +85°C	74AC11162D 74ACT11162D

PIN CONFIGURATION

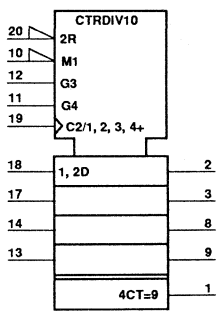
N and D Packages



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



Synchronous Presettable BCD Decade Counter; Synchronous Reset

74AC/ACT11162

The outputs of the counters may be preset to High or Low levels. A Low level at the Parallel Enable ($\overline{PE}$) input disables the counting action and causes the data at the D_0 - D_3 inputs to be loaded into the counter on the rising edge of the clock. Preset takes place regardless of the levels at Count Enable (CEP, CET) inputs.

A Low level at the Reset ($\overline{SR}$) input sets all four outputs of the flip-flops (Q_0 - Q_3) to Low levels after the next positive-going transition on the clock (CP) input. This action occurs regardless of the levels at $\overline{PE}$, CET, and CEP inputs. This synchronous reset feature enables the designer to modify the maximum count with only one external NAND gate.

The carry look-ahead simplifies serial cascading of the counters. Both Count Enable inputs (CEP and CET) must be High to count. The CET input is fed forward to enable the Terminal Count (TC) output. The TC output thus enabled will produce a High output pulse of a duration approximately equal to the High level output of Q_0. This pulse can be used to enable the next cascaded stage.

PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
20	$\overline{SR}$	Synchronous reset (active Low)
19	CP	Clock input (Low-to-High edge-triggered)
18, 17, 14, 13	D_0 - D_3	Data inputs
12	CEP	Count enable input
10	$\overline{PE}$	Parallel enable input (active Low)
11	CET	Count enable carry input
18, 17, 14, 13	Q_0 - Q_3	Counter outputs
1	TC	Terminal count output
4, 5, 6, 7	GND	Ground (0V)
15, 16	V_{CC}	Positive supply voltage

FUNCTION TABLE

OPERATING MODE	INPUTS						OUTPUTS	
	$\overline{SR}$	CP	CEP	CET	$\overline{PE}$	D_n	Q_n	TC
Reset (clear)	l	↑	X	X	X	X	L	L
Parallel load	h	↑	X	X	l	l	L	L
	h	↑	X	X	l	h	H	(1)
Count	h	↑	h	h	h	X	count	(1)
Hold (do nothing)	h	X	l	X	h	X	q_n	(1)
	h	X	X	l	h	X	q_n	L

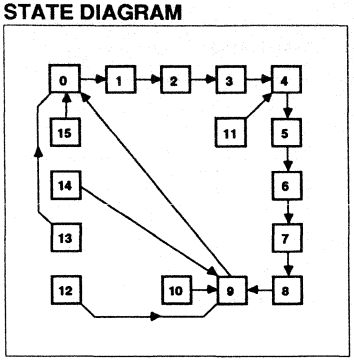
H = High voltage level
L = Low voltage level
h = High voltage level one setup time prior to the Low-to High clock transition
l = Low voltage level one setup time prior to the Low-to High clock transition
X = Don't care
q = State of the referenced output prior to the Low-to High clock transition
↑ = Low-to-High clock transition

NOTE:
1. The TC output is High when CET is High and the counter is at Terminal Count (HLLH).

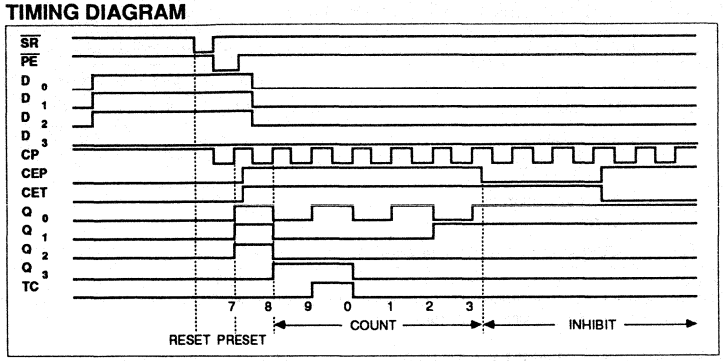
Synchronous Presettable BCD Decade Counter; Synchronous Reset

74AC/ACT11162

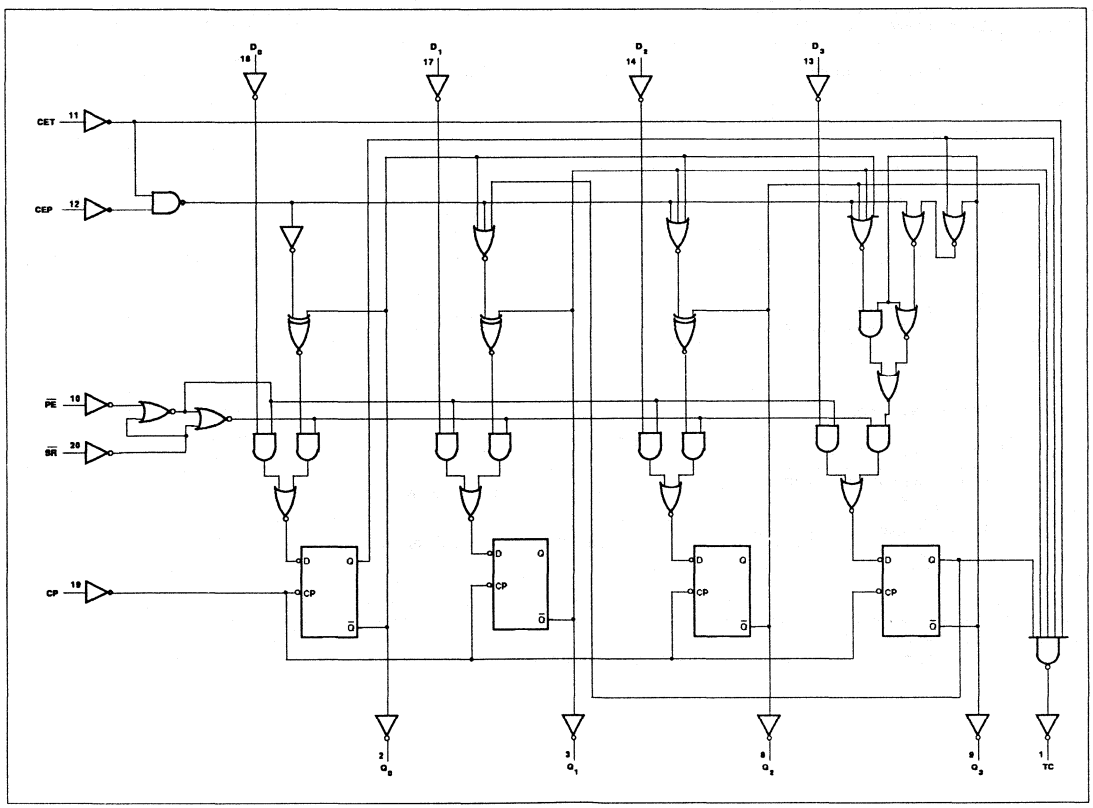
STATE DIAGRAM



TIMING DIAGRAM



LOGIC DIAGRAM



RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	74AC11162			74ACT11162			UNIT
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	DC supply voltage	3.0[1]	5.0	5.5	4.5	5.0	5.5	V
V_I	Input voltage	0		V_{CC}	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	0		V_{CC}	V
$\Delta t/\Delta v$	Input transition rise or fall rate	0		10	0		10	ns/V
T_A	Operating free-air temperature	-40		+85	-40		+85	°C

NOTE:

1. No electrical or switching characteristics are specified at $V_{CC} < 3V$. Operation between 2V and 3V is not recommended, but within that range, a device output will maintain a previously established logic state.

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	TEST CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 to+7.0	V
I_{IK} or V_I	DC input diode current[2]	$V_I < 0$	-20	mA
		$V_I > V_{CC}$	20	
	DC input voltage		-0.5 to V_{CC} +0.5	V
I_{OK} or V_O	DC output diode current[2]	$V_O < 0$	-50	mA
		$V_O > V_{CC}$	50	
	DC output voltage		-0.5 to V_{CC} +0.5	V
I_O	DC output source or sink current per output pin	V_O = 0 to V_{CC}	±50	mA
I_{CC} or I_{GND}	DC V_{CC} current		±125	mA
	DC ground current		±125	
T_{STG}	Storage temperature		-65 to 150	°C
P_{TOT}	Power dissipation per package Plastic DIP	Above 70°C:derate linearly by 8mW/K	500	mW
	Power dissipation per package Plastic surface mount (SO)	Above 70°C:derate linearly by 6mW/K	400	mW

NOTES:

1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		V_{CC}	74AC11162				74ACT11162				UNIT
					T_A = +25°C		T_A = -40°C to +85°C		T_A = +25°C		T_A = -40°C to +85°C		
				V	Min	Max	Min	Max	Min	Max	Min	Max	
V_{IH}	High-level input voltage			3.0	2.10		2.10						V
				4.5	3.15		3.15		2.0		2.0		
				5.5	3.85		3.85		2.0		2.0		
V_{IL}	Low-level input voltage			3.0		0.90		0.90					V
				4.5		1.35		1.35		0.8		0.8	
				5.5		1.65		1.65		0.8		0.8	
V_{OH}	High-level output voltage	V_I = V_{IL} or V_{IH}	I_{OH} = -50μA	3.0	2.9		2.9						V
				4.5	4.4		4.4		4.4		4.4		
				5.5	5.4		5.4		5.4		5.4		
			I_{OH} = -4mA	3.0	2.58		2.48						
			I_{OH} = -24mA	4.5	3.94		3.8		3.94		3.8		
				5.5	4.94		4.8		4.94		4.8		
			I_{OH} = -75mA[1]	5.5			3.85				3.85		
V_{OL}	Low-level output voltage	V_I = V_{IL} or V_{IH}	I_{OL} = 50μA	3.0		0.1		0.1					V
				4.5		0.1		0.1		0.1		0.1	
				5.5		0.1		0.1		0.1		0.1	
			I_{OL} = 12mA	3.0		0.36		0.44					
			I_{OL} = 24mA	4.5		0.36		0.44		0.36		0.44	
				5.5		0.36		0.44		0.36		0.44	
			I_{OL} = 75mA[1]	5.5				1.65				1.65	
I_I	Input leakage current	V_I = V_{CC} or GND		5.5		±0.1		±1.0		±0.1		±1.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC} or GND, I_O = 0		5.5		8.0		80		8.0		80	μA
ΔI_{CC}	Supply current, TTL inputs High[2]	One input at 3.4V, other inputs at V_{CC} or GND		5.5						0.9		1.0	mA

NOTES:
1. Not more than one output should be tested at a time, and the duration of the test should not exceed 10ms.
2. This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0V or V_{CC}.

AC ELECTRICAL CHARACTERISTICS AT 3.3V ±0.3V

SYMBOL	PARAMETER	WAVEFORM	74AC11162					UNIT
			T_A = +25°C			T_A = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	1	66	90		66		MHz
t_{PLH} t_{PHL}	Propagation delay CP to Q_n ($\overline{PE}$ = "H")	1	1.5 1.5	8.7 10.2	11.7 14.4	1.5 1.5	13.2 16.0	ns
t_{PLH} t_{PHL}	Propagation delay CP to Q_n ($\overline{PE}$ = "L")	1	1.5 1.5	8.7 10.4	11.2 14.1	1.5 1.5	12.6 16.0	ns
t_{PLH} t_{PHL}	Propagation delay CP to TC	1	1.5 1.5	10.5 12.1	14.1 15.8	1.5 1.5	15.9 18.0	ns
t_{PLH} t_{PHL}	Propagation delay CET to TC	2	1.5 1.5	5.8 6.9	7.6 9.9	1.5 1.5	8.5 11.0	ns
t_S	Setup time, High or Low D_n to CP	3	6.0			6.0		ns
t_H	Hold time, High or Low D_n to CP	3	1.0			1.0		ns
t_S	Setup time, High or Low $\overline{PE}$ to CP	3	6.0			6.0		ns
t_H	Hold time, High or Low $\overline{PE}$ to CP	3	1.0			1.0		ns
t_S	Setup time, High or Low CEP or CET to CP	4	7.5			7.5		ns
t_H	Hold time, High or Low CEP or CET to CP	4	1.0			1.0		ns
t_W	Clock pulse width (load) High or Low	1	7.5			7.5		ns
t_W	Clock pulse width (count) High or Low	1	7.5			7.5		ns
t_S	Setup time, High or Low $\overline{SR}$ to CP	3	7.5			7.5		ns
t_H	Hold time, High or Low $\overline{SR}$ to CP	3	1.0			1.0		ns

Synchronous Presettable BCD Decade Counter; Synchronous Reset

74AC/ACT11162

AC ELECTRICAL CHARACTERISTICS AT 5.0V ±0.5V

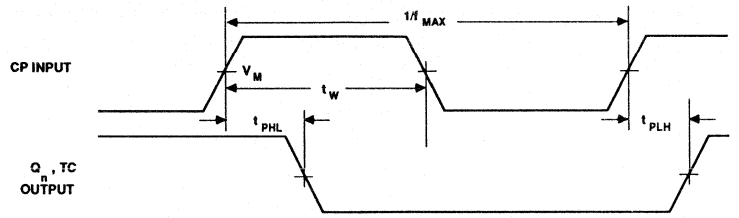
SYMBOL	PARAMETER	WAVEFORM	74AC11162					UNIT
			T_A = +25°C			T_A = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	1	110	140		110		MHz
t_{PLH} t_{PHL}	Propagation delay CP to Q_n ($\overline{PE}$ = "H")	1	1.5 1.5	6.4 7.4	8.4 10.5	1.5 1.5	9.5 11.9	ns
t_{PLH} t_{PHL}	Propagation delay CP to Q_n ($\overline{PE}$ = "L")	1	1.5 1.5	6.0 7.2	7.9 10.1	1.5 1.5	9.0 11.5	ns
t_{PLH} t_{PHL}	Propagation delay CP to TC	1	1.5 1.5	7.7 8.3	10.1 11.1	1.5 1.5	11.2 12.6	ns
t_{PLH} t_{PHL}	Propagation delay CET to TC	2	1.5 1.5	4.0 5.0	5.5 7.4	1.5 1.5	6.0 10.2	ns
t_S	Setup time, High or Low D_n to CP	3	4.0			4.0		ns
t_H	Hold time, High or Low D_n to CP	3	1.0			1.0		ns
t_S	Setup time, High or Low $\overline{PE}$ to CP	3	5.0			5.0		ns
t_H	Hold time, High or Low $\overline{PE}$ to CP	3	1.0			1.0		ns
t_S	Setup time, High or Low CEP or CET to CP	4	6.0			6.0		ns
t_H	Hold time, High or Low CEP or CET to CP	4	1.0			1.0		ns
t_W	Clock pulse width (load) High or Low	1	4.5			4.5		ns
t_W	Clock pulse width (count) High or Low	1	4.5			4.5		ns
t_S	Setup time, High or Low $\overline{SR}$ to CP	3	4.5			4.5		ns
t_H	Hold time, High or Low $\overline{SR}$ to CP	3	1.0			1.0		ns

AC ELECTRICAL CHARACTERISTICS AT 5.0V ±0.5V

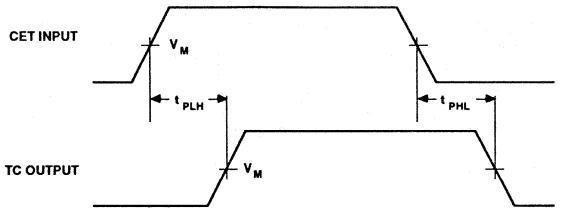
SYMBOL	PARAMETER	WAVEFORM	74ACT11162					UNIT
			T_A = +25°C			T_A = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	1						MHz
t_{PLH} t_{PHL}	Propagation delay CP to Q_n ($\overline{PE}$ = "H")	1	1.5 1.5			1.5 1.5		ns
t_{PLH} t_{PHL}	Propagation delay CP to Q_n ($\overline{PE}$ = "L")	1	1.5 1.5			1.5 1.5		ns
t_{PLH} t_{PHL}	Propagation delay CP to TC	1	1.5 1.5			1.5 1.5		ns
t_{PLH} t_{PHL}	Propagation delay CET to TC	2	1.5 1.5			1.5 1.5		ns
t_S	Setup time, High or Low D_n to CP	3						ns
t_H	Hold time, High or Low D_n to CP	3						ns
t_S	Setup time, High or Low $\overline{PE}$ to CP	3						ns
t_H	Hold time, High or Low $\overline{PE}$ to CP	3						ns
t_S	Setup time, High or Low CEP or CET to CP	4						ns
t_H	Hold time, High or Low CEP or CET to CP	4						ns
t_W	Clock pulse width (load) High or Low	1						ns
t_W	Clock pulse width (count) High or Low	1						ns
t_S	Setup time, High or Low $\overline{SR}$ to CP	3						ns
t_H	Hold time, High or Low $\overline{SR}$ to CP	3						ns

Synchronous Presettable BCD Decade Counter; Synchronous Reset

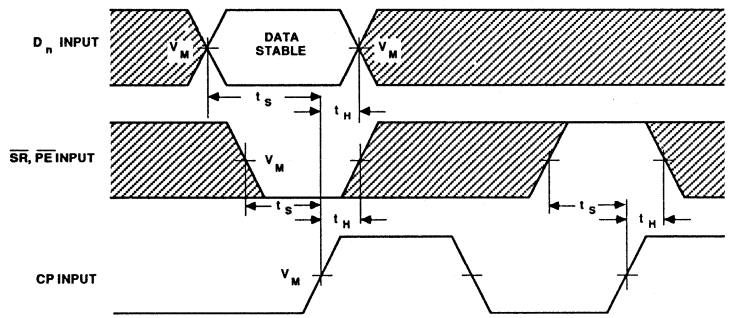
AC WAVEFORMS



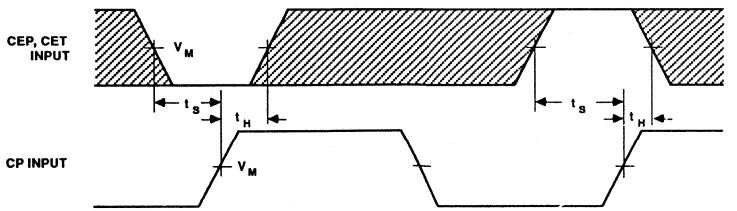
Waveform 1. Waveforms Showing Clock to Outputs Propagation Delays, and Clock Pulse Width



Waveform 2. Waveforms Showing the Input (CET) to Output (TC) Propagation Delays



Waveform 3. Waveforms Showing the Data Set-up and Hold Times for the Input (D_n), Parallel Enable Input ($\overline{PE}$), and Synchronous Reset Input ($\overline{SR}$).



Waveform 4. Waveforms Showing CEP and CET Set-up and Hold Times

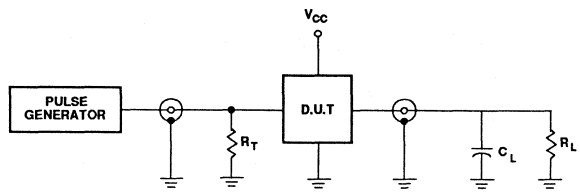
Synchronous Presettable BCD Decade Counter; Synchronous Reset

74AC/ACT11162

WAVEFORM CONDITIONS

	INPUTS	OUTPUTS
AC	V_{IN} = GND to V_{CC}, V_M = 50% V_{CC}	V_{OUT} = V_{OL} to V_{OH}
ACT	V_{IN} = GND to 3.0V, V_M = 1.5V	V_M = 50% V_{CC}

TEST CIRCUIT



Test Circuit

DEFINITIONS

C_L = Load capacitance, 50pF; includes jig and probe capacitance

R_L = Load resistor, 500Ω

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators

Input pulses: PRR ≤ 10MHz

$t_r = t_f$ = 3ns

74AC/ACT11163

Synchronous Presettable 4-Bit Binary Counter; Synchronous Reset

Objective Specification

FEATURES

- **Synchronous counting and loading**
- **Two count enable inputs for n-bit cascading**
- **Positive edge-triggered clock**
- **Synchronous reset**
- **Output capability: ±24mA**
- **CMOS (AC) and TTL (ACT) voltage level inputs**
- **50Ω incident wave switching**
- **Center-pin V_{CC} and ground configuration to minimize high-speed switching noise**
- **I_{CC} category: MSI**

DESCRIPTION

The 74AC/ACT11163 high-performance CMOS devices combine very high speed and high output drive comparable to the most advanced TTL families.

The 74AC/ACT11163 4-bit synchronous presettable binary counters feature an internal carry look-ahead and can be used for high-speed counting. Synchronous operation is provided by having all flip-flops clocked simultaneously on the positive-going edge of the clock.

GENERAL INFORMATION

SYMBOL	PARAMETER	CONDITIONS T_A = 25°C; GND = 0V; V_{CC} = 5.0V	TYPICAL		UNIT
			AC	ACT	
t_{PLH}/t_{PHL}	Propagation delay CP_n to Q_n ($\overline{PE}$ = High)	C_L = 50pF	7.5	8.8	ns
C_{PD}	Power dissipation capacitance[1]	f = 1MHz; C_L = 50pF	54	60	pF
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	4.0	4.0	pF
I_{LATCH}	Latch-up current	Per Jedec JC40.2 Standard 17	500	500	mA
f_{MAX}	Maximum clock frequency	C_L = 50pF	125	125	MHz

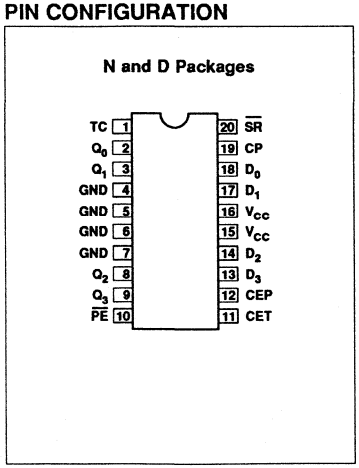
Note:

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_I + \Sigma (C_L \times V_{CC}^2 \times f_O)$ where:
   f_I = input frequency in MHz, C_L = output load capacitance in pF,
   f_O = output frequency in MHz, V_{CC} = supply voltage in V,
   $\Sigma (C_L \times V_{CC}^2 \times f_O)$ = sum of outputs

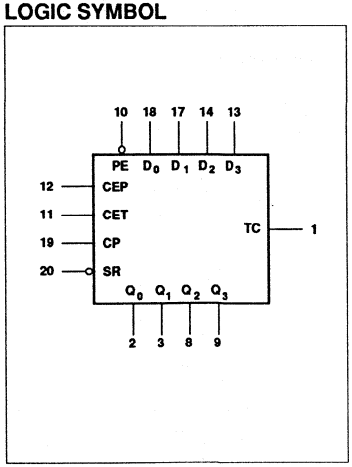
ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE
20-pin plastic DIP (300mil-wide)	-40°C to +85°C	74AC11163N 74ACT11163N
20-pin plastic SO (300mil-wide)	-40°C to +85°C	74AC11163D 74ACT11163D

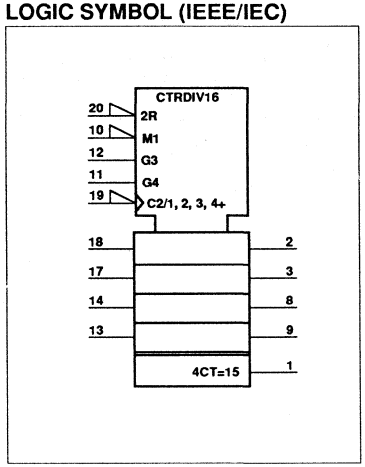
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



Synchronous Presettable 4-Bit Binary Counter; Synchronous Reset

The outputs of the counters may be preset to High or Low levels. A Low level at the Parallel Enable ($\overline{PE}$) input disables the counting action and causes the data at the D_0 - D_3 inputs to be loaded into the counter on the rising edge of the clock. Preset takes place regardless of the levels at Count Enable (CEP, CET) inputs.

A Low level at the Reset ($\overline{SR}$) input sets all four outputs of the flip-flops (Q_0 - Q_3) to Low levels after the next positive-going transition on the clock (CP) input. This action occurs regardless of the levels at $\overline{PE}$, CET, and CEP inputs. This synchronous reset feature enables the designer to modify the maximum count with only one external NAND gate.

The carry look-ahead simplifies serial cascading of the counters. Both Count Enable inputs (CEP and CET) must be High to count. The CET input is fed forward to enable the Terminal Count (TC) output. The TC output thus enabled will produce a High output pulse of a duration approximately equal to the High level output of Q_0. This pulse can be used to enable the next cascaded stage.

PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
20	$\overline{SR}$	Synchronous reset (active Low)
19	CP	Clock input (Low-to-High edge-triggered)
18, 17, 14, 13	D_0 - D_3	Data inputs
12	CEP	Count enable input
10	$\overline{PE}$	Parallel enable input (active Low)
11	CET	Count enable carry input
18, 17, 14, 13	Q_0 - Q_3	Counter outputs
1	TC	Terminal count output
4, 5, 6, 7	GND	Ground (0V)
15, 16	V_{CC}	Positive supply voltage

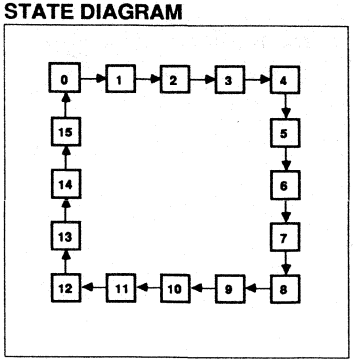
FUNCTION TABLE

OPERATING MODE	INPUTS						OUTPUTS	
	$\overline{SR}$	CP	CEP	CET	$\overline{PE}$	D_n	Q_n	TC
Reset (clear)	l	↑	X	X	X	X	L	L
Parallel load	h	↑	X	X	l	l	L	L
	h	↑	X	X	l	h	H	(1)
Count	h	↑	h	h	h	X	count	(1)
Hold (do nothing)	h	X	l	X	h	X	q_n	(1)
	h	X	X	l	h	X	q_n	L

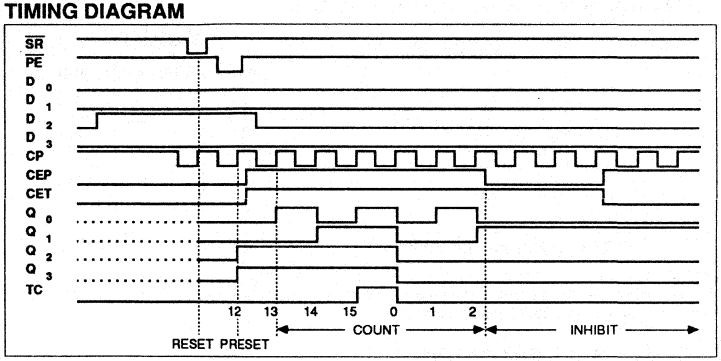
H = High voltage level
L = Low voltage level
h = High voltage level one setup time prior to the Low-to High clock transition
l = Low voltage level one setup time prior to the Low-to High clock transition
X = Don't care
q = State of the referenced output prior to the Low-to High clock transition
↑ = Low-to-High clock transition

NOTE:
1. The TC output is High when CET is High and the counter is at Terminal Count (HHHH).

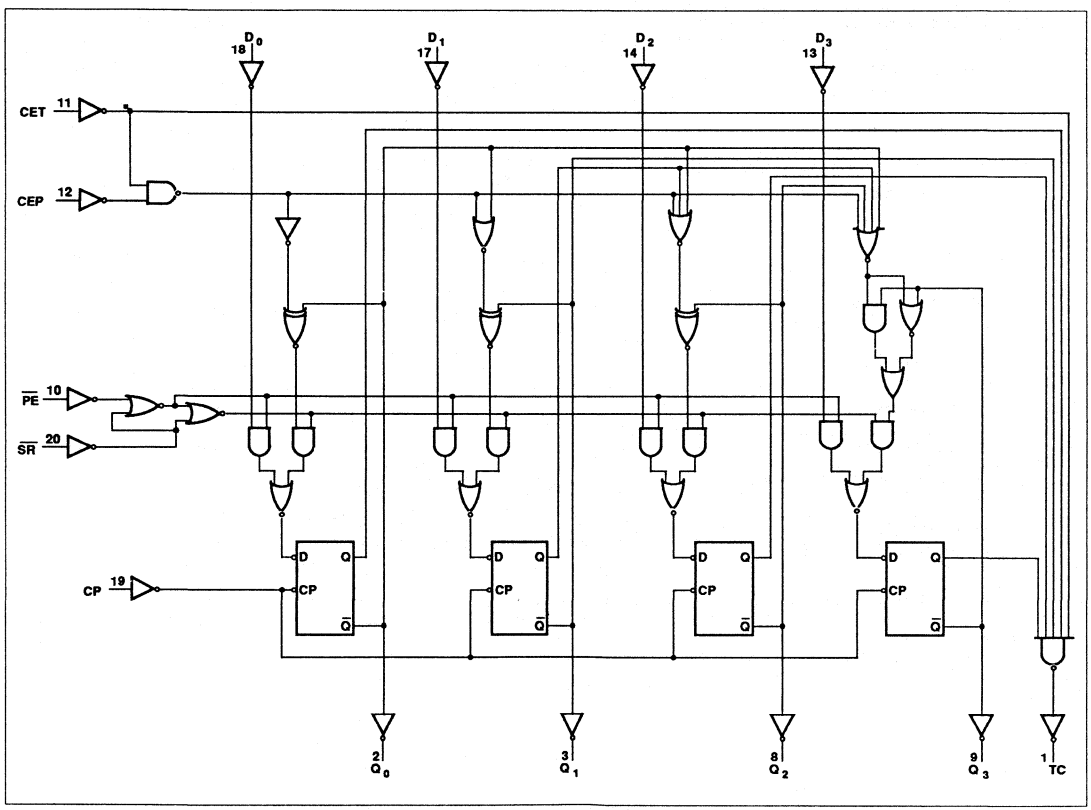
STATE DIAGRAM



TIMING DIAGRAM



LOGIC DIAGRAM



RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	74AC11163			74ACT11163			UNIT
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	DC supply voltage	3.0[1]	5.0	5.5	4.5	5.0	5.5	V
V_I	Input voltage	0		V_{CC}	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	0		V_{CC}	V
$\Delta t/\Delta v$	Input transition rise or fall rate	0		10	0		10	ns/V
T_A	Operating free-air temperature	-40		+85	-40		+85	°C

NOTE:

1. No electrical or switching characteristics are specified at $V_{CC} < 3V$. Operation between 2V and 3V is not recommended, but within that range, a device output will maintain a previously established logic state.

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	TEST CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 to+7.0	V
I_{IK} or V_I	DC input diode current[2]	$V_I < 0$	-20	mA
		$V_I > V_{CC}$	20	
	DC input voltage		-0.5 to V_{CC} +0.5	V
I_{OK} or V_O	DC output diode current[2]	$V_O < 0$	-50	mA
		$V_O > V_{CC}$	50	
	DC output voltage		-0.5 to V_{CC} +0.5	V
I_O	DC output source or sink current per output pin	V_O = 0 to V_{CC}	±50	mA
I_{CC} or I_{GND}	DC V_{CC} current		±125	mA
	DC ground current		±125	
T_{STG}	Storage temperature		-65 to 150	°C
P_{TOT}	Power dissipation per package Plastic DIP	Above 70°C:derate linearly by 8mW/K	500	mW
	Power dissipation per package Plastic surface mount (SO)	Above 70°C:derate linearly by 6mW/K	400	mW

NOTES:

1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		V_{CC}	74AC11163				74ACT11163				UNIT
					T_A = +25°C		T_A = -40°C to +85°C		T_A = +25°C		T_A = -40°C to +85°C		
				V	Min	Max	Min	Max	Min	Max	Min	Max	
V_{IH}	High-level input voltage			3.0	2.10		2.10						V
				4.5	3.15		3.15		2.0		2.0		
				5.5	3.85		3.85		2.0		2.0		
V_{IL}	Low-level input voltage			3.0		0.90		0.90					V
				4.5		1.35		1.35		0.8		0.8	
				5.5		1.65		1.65		0.8		0.8	
V_{OH}	High-level output voltage	V_I = V_{IL} or V_{IH}	I_{OH} = -50μA	3.0	2.9		2.9						V
				4.5	4.4		4.4		4.4		4.4		
				5.5	5.4		5.4		5.4		5.4		
			I_{OH} = -4mA	3.0	2.58		2.48						
			I_{OH} = -24mA	4.5	3.94		3.8		3.94		3.8		
				5.5	4.94		4.8		4.94		4.8		
			I_{OH} = -75mA[1]	5.5			3.85				3.85		
V_{OL}	Low-level output voltage	V_I = V_{IL} or V_{IH}	I_{OL} = 50μA	3.0		0.1		0.1					V
				4.5		0.1		0.1		0.1		0.1	
				5.5		0.1		0.1		0.1		0.1	
			I_{OL} = 12mA	3.0		0.36		0.44					
			I_{OL} = 24mA	4.5		0.36		0.44		0.36		0.44	
				5.5		0.36		0.44		0.36		0.44	
			I_{OL} = 75mA[1]	5.5				1.65				1.65	
I_I	Input leakage current	V_I = V_{CC} or GND		5.5		±0.1		±1.0		±0.1		±1.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC} or GND, I_O = 0		5.5		8.0		80		8.0		80	μA
ΔI_{CC}	Supply current, TTL inputs High[2]	One input at 3.4V, other inputs at V_{CC} or GND		5.5						0.9		1.0	mA

NOTES:
1. Not more than one output should be tested at a time, and the duration of the test should not exceed 10ms.
2. This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0V or V_{CC}.

74AC/ACT11168

Synchronous Presettable 4-Bit Up/Down BCD Decade Counter

Objective Specification

FEATURES

- **Synchronous counting and loading**
- **Up/Down counting**
- **BCD decade counter**
- **Two Count Enable inputs for n-bit cascading**
- **Positive edge-triggered Clock**
- **Built-in look-ahead carry capability**
- **Presettable for programmable operation**
- **Output capability: ±24mA**
- **CMOS (AC) and TTL (ACT) voltage level inputs**
- **50Ω incident wave switching**
- **Center-pin V_{CC} and ground configuration to minimize high-speed switching noise**
- **I_{CC} category: MSI**

DESCRIPTION

The 74AC/ACT11168 high-performance CMOS devices combine very high speed and high output drive comparable to the most advanced TTL families.

The AC/ACT11168 is a synchronous, presettable BCD decade up/down counter featuring an internal Carry look-

GENERAL INFORMATION

SYMBOL	PARAMETER	CONDITIONS T_A = 25°C; GND = 0V; V_{CC} = 5.0V	TYPICAL		UNIT
			AC	ACT	
t_{PLH}/ t_{PHL}	Propagation delay CP to Q_n ($\overline{PE}$ = High)	C_L = 50pF	5.8	6.3	ns
C_{PD}	Power dissipation capacitance[1]	f = 1MHz; C_L = 50pF	150	150	pF
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	4.0	4.0	pF
I_{LATCH}	Latch-up current	Per Jedec JC40.2 Standard 17	500	500	mA
f_{MAX}	Maximum clock frequency	C_L = 50pF	125	110	MHz

Note:

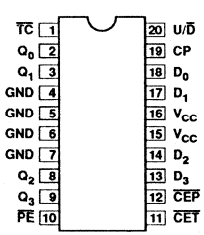
1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_I + \Sigma (C_L \times V_{CC}^2 \times f_O)$ where:
   f_I = input frequency in MHz, C_L = output load capacitance in pF,
   f_O = output frequency in MHz, V_{CC} = supply voltage in V,
   $\Sigma (C_L \times V_{CC}^2 \times f_O)$ = sum of outputs

ORDERING INFORMATION

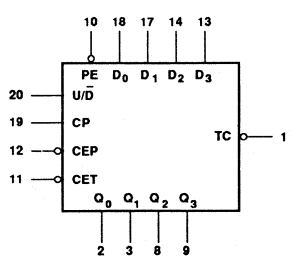
PACKAGES	TEMPERATURE RANGE	ORDER CODE
20-pin plastic DIP (300mil-wide)	-40°C to +85°C	74AC11168N 74ACT11168N
20-pin plastic SO (300mil-wide)	-40°C to +85°C	74AC11168D 74ACT11168D

PIN CONFIGURATION

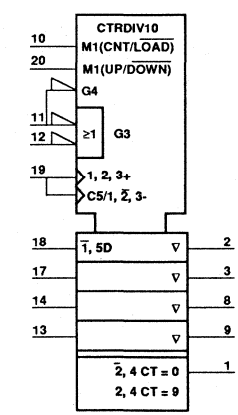
N and D Packages



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



Synchronous Presettable 4-Bit Up/Down BCD Decade Counter

74AC/ACT11168

ahead for applications in high-speed counting designs. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when so instructed by the Count Enable inputs and internal gating. This mode of operation eliminates the output spikes which are normally associated with asynchronous (ripple clock) counters. A buffered Clock input triggers the flip-flops on the Low-to-High transition of the clock.

The counter is fully programmable; that is, the outputs may be preset to either level.

Presetting is synchronous with the clock and takes place regardless of the levels of the Count Enable inputs. A Low level on the Parallel Enable ($\overline{PE}$) input disables the counter and causes the data at the D_n input to be loaded into the counter on the next Low-to-High transition of the clock.

The direction of counting is controlled by the Up/Down ($U/\overline{D}$) input; a High will cause the count to increase, a Low will cause the count to decrease.

The Carry look-ahead circuitry provides for cascading counters for n-bit synchronous applications without additional gating. Instrumental in accomplishing this function are two Count Enable inputs ($\overline{CET}$•$\overline{CEP}$) and a Terminal Count ($\overline{TC}$) output. Both Count Enable inputs must be Low to count. The $\overline{CET}$ input is fed forward to enable the $\overline{TC}$ output. The $\overline{TC}$ output thus enabled will produce a Low output pulse with a duration approximately equal to the High level or Low level portion of the Q_0 output, depending on the state of the $U/\overline{D}$ input. This Low level $\overline{TC}$ pulse is used to enable successive cascaded stages. See Figure 1 for the fast synchronous multi-stage counting connections.

FUNCTIONAL DESCRIPTION

The AC/ACT11168 uses edge-triggered D-type flip-flops and has no constraints on changing the control or data input signals in either state of the Clock. The only requirement is that the various inputs attain the desired state at least a setup time before the rising edge of the Clock and remain valid for the recommended hold time thereafter. The parallel load operation takes precedence over the other operations, as indicated in the Mode Select Table. When $\overline{PE}$ is Low, the data on the D_0 - D_3 inputs enter the flip-flops on the next rising edge of the Clock. In order for counting to occur, both $\overline{CEP}$ and $\overline{CET}$ must be Low and $\overline{PE}$ must be High; the $U/\overline{D}$ input then determines the direction of counting. The Terminal Count ($\overline{TC}$) output is normally High and goes Low when a counter reaches zero in the Count Down mode or reaches 9 in the Count Up mode, provided that $\overline{CET}$ is Low. The $\overline{TC}$ output state is not a function of the Count Enable Parallel ($\overline{CEP}$) input level. The $\overline{TC}$ output of the AC/ACT11168 decade counter can also be Low in the illegal states 11, 13, 15, which can occur when power is turned on or via parallel loading. If an illegal state occurs, the AC/ACT11168 will return to the legitimate sequence within two counts. The $\overline{TC}$ signal is derived by decoding the D-input signals of the counter flip-flops and using this decoded signal as the D-input driving the $\overline{TC}$ output. Use of this configuration gives a $\overline{TC}$ output which is free of decoding spikes. The possibility exists that on pwer-up that the $\overline{TC}$ output may not give a true indication of the state of the counter (i.e., $\overline{TC}$ may be Low while the counter is not at terminal count or High when it is at terminal count.) Should this occur, $\overline{TC}$ will always go to a correct state on the first Low-to-High transition of the clock.

1) Count Enable = $\overline{CEP} \cdot \overline{CET} \cdot \overline{PE}$

2) Up: $\overline{TC} = Q_0 \cdot Q_3 \cdot (U/\overline{D}) \cdot \overline{CET}$

3) Down: $\overline{TC} = \overline{Q}_0 \cdot \overline{Q}_1 \cdot \overline{Q}_2 \cdot \overline{Q}_3 \cdot \overline{(U/\overline{D})} \cdot \overline{CET}$

PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
20	$U/\overline{D}$	Up/down count control input
19	CP	Clock input (Low-to-High, edge-triggered)
18, 17, 14, 13	D_0 - D_3	Data inputs
12	$\overline{CEP}$	Count enable parallel input (active Low)
11	$\overline{CET}$	Count enable trickle input (active Low)
12	$\overline{PE}$	Parallel enable input (active Low)
2, 3, 8, 9	Q_0 - Q_3	Counter outputs
1	$\overline{TC}$	Terminal count output (active Low)
4, 5, 6, 7	GND	Ground (0V)
15, 16	V_{CC}	Positive supply voltage

MODE SELECT TABLE

$\overline{PE}$	$\overline{CEP}$	$\overline{CET}$	$U/\overline{D}$	ACTION ON RISING CLOCK EDGE
L	X	X	X	Load ($D_n \rightarrow Q_n$)
H	L	L	H	Count up (increment)
H	L	L	L	Count down (decrement)
H	H	X	X	No change (hold)
H	X	H	X	

H = High voltage level
L = Low voltage level
X = Don't care

Synchronous Presettable 4-Bit Up/Down BCD Decade Counter

74AC/ACT11168

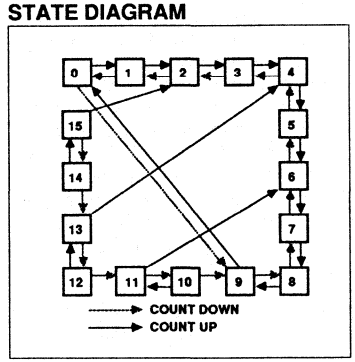
MODE SELECT—FUNCTION TABLE

OPERATING MODE	INPUTS						OUTPUTS	
	CP	U/$\overline{D}$	$\overline{CEP}$	$\overline{CET}$	$\overline{PE}$	D_n	Q_n	$\overline{TC}$
Parallel load	↑	X	X	X	l	l	L	(1)
	↑	X	X	X	l	h	H	(1)
Count up	↑	h	l	l	h	X	Count up	(1)
Count down	↑	l	l	l	h	X	Count down	(1)
Hold (do nothing)	↑	X	h	X	h	X	q_n	(1)
	↑	X	X	h	h	X	q_n	H

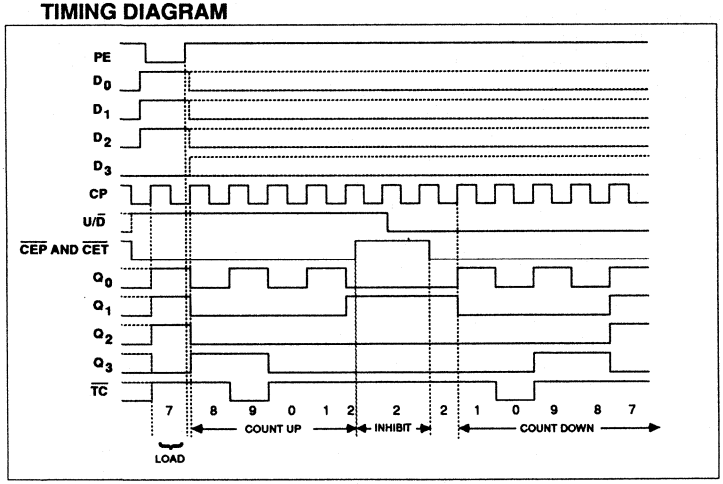
H = High voltage level steady state
h = High voltage level one setup time prior to the Low-to-High clock transition
L = Low voltage level steady state
l = Low voltage level one setup time prior to the Low-to-High clock transition
X = Don't care
q = State of the referenced output prior to the Low-to-High clock transition
↑ =Low-to-High clock transition

NOTES:
1. $\overline{TC}$ is Low when $\overline{CET}$ is Low and the counter is at Terminal Count. Terminal Count Up is (HLLH) and Terminal Count Down is (LLLL).

STATE DIAGRAM



TIMING DIAGRAM



Synchronous Presettable 4-Bit Up/Down BCD Decade Counter

74AC/ACT11168

LOGIC DIAGRAM

UNDER DEVELOPMENT

APPLICATIONS

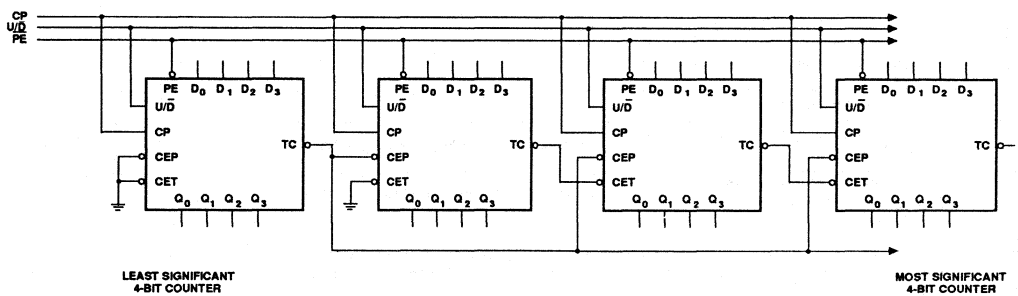


Figure 1. Synchronous Multistage Counting Scheme

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	74AC11168			74ACT11168			UNIT
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	DC supply voltage	3.0[1]	5.0	5.5	4.5	5.0	5.5	V
V_I	Input voltage	0		V_{CC}	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	0		V_{CC}	V
$\Delta t/\Delta v$	Input transition rise or fall rate	0		10	0		10	ns/V
T_A	Operating free-air temperature	-40		+85	-40		+85	°C

NOTE:

1. No electrical or switching characteristics are specified at $V_{CC} < 3V$. Operation between 2V and 3V is not recommended, but within that range, a device output will maintain a previously established logic state.

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	TEST CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 to+7.0	V
I_{IK} or V_I	DC input diode current[2]	$V_I < 0$	-20	mA
		$V_I > V_{CC}$	20	
	DC input voltage		-0.5 to V_{CC} +0.5	V
I_{OK} or V_O	DC output diode current[2]	$V_O < 0$	-50	mA
		$V_O > V_{CC}$	50	
	DC output voltage		-0.5 to V_{CC} +0.5	V
I_O	DC output source or sink current per output pin	V_O = 0 to V_{CC}	±50	mA
I_{CC} or I_{GND}	DC V_{CC} current		±125	mA
	DC ground current		±125	
T_{STG}	Storage temperature		-65 to 150	°C
P_{TOT}	Power dissipation per package Plastic DIP	Above 70°C:derate linearly by 8mW/K	500	mW
	Power dissipation per package Plastic surface mount (SO)	Above 70°C:derate linearly by 6mW/K	400	mW

NOTES:

1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		V_{CC}	74AC11168				74ACT11168				UNIT
					T_A = +25°C		T_A = -40°C to +85°C		T_A = +25°C		T_A = -40°C to +85°C		
				V	Min	Max	Min	Max	Min	Max	Min	Max	
V_{IH}	High-level input voltage			3.0	2.10		2.10						V
				4.5	3.15		3.15		2.0		2.0		
				5.5	3.85		3.85		2.0		2.0		
V_{IL}	Low-level input voltage			3.0		0.90		0.90					V
				4.5		1.35		1.35		0.8		0.8	
				5.5		1.65		1.65		0.8		0.8	
V_{OH}	High-level output voltage	V_I = V_{IL} or V_{IH}	I_{OH} = -50μA	3.0	2.9		2.9						V
				4.5	4.4		4.4		4.4		4.4		
				5.5	5.4		5.4		5.4		5.4		
			I_{OH} = -4mA	3.0	2.58		2.48						
			I_{OH} = -24mA	4.5	3.94		3.8		3.94		3.8		
				5.5	4.94		4.8		4.94		4.8		
			I_{OH} = -75mA[1]	5.5			3.85				3.85		
V_{OL}	Low-level output voltage	V_I = V_{IL} or V_{IH}	I_{OL} = 50μA	3.0		0.1		0.1					V
				4.5		0.1		0.1		0.1		0.1	
				5.5		0.1		0.1		0.1		0.1	
			I_{OL} = 12mA	3.0		0.36		0.44					
			I_{OL} = 24mA	4.5		0.36		0.44		0.36		0.44	
				5.5		0.36		0.44		0.36		0.44	
			I_{OL} = 75mA[1]	5.5				1.65				1.65	
I_I	Input leakage current	V_I = V_{CC} or GND		5.5		±0.1		±1.0		±0.1		±1.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC} or GND, I_O = 0		5.5		8.0		80		8.0		80	μA
ΔI_{CC}	Supply current, TTL inputs High[2]	One input at 3.4V, other inputs at V_{CC} or GND		5.5						0.9		1.0	mA

NOTES:
1. Not more than one output should be tested at a time, and the duration of the test should not exceed 10ms.
2. This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0V or V_{CC}.

74AC/ACT11169

Synchronous Presettable 4-Bit Up/Down Binary Counter

Objective Specification

FEATURES

- **Synchronous counting and loading**
- **Up/Down counting**
- **Modulo 16 binary counter**
- **Two Count Enable inputs for n-bit cascading**
- **Positive edge-triggered Clock**
- **Built-in look-ahead carry capability**
- **Presettable for programmable operation**
- **Output capability: ±24mA**
- **CMOS (AC) and TTL (ACT) voltage level inputs**
- **50Ω incident wave switching**
- **Center-pin V_{CC} and ground configuration to minimize high-speed switching noise**
- **I_{CC} category: MSI**

DESCRIPTION

The 74AC/ACT11169 high-performance CMOS devices combine very high speed and high output drive comparable to the most advanced TTL families.

The AC/ACT11169 is a synchronous, presettable 4-bit up/down binary counter featuring an internal Carry look-ahead for

GENERAL INFORMATION

SYMBOL	PARAMETER	CONDITIONS T_A = 25°C; GND = 0V; V_{CC} = 5.0V	TYPICAL		UNIT
			AC	ACT	
t_{PLH}/ t_{PHL}	Propagation delay CP to Q_n ($\overline{PE}$ = High)	C_L = 50pF	5.8	6.3	ns
C_{PD}	Power dissipation capacitance[1]	f = 1MHz; C_L = 50pF	150	150	pF
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	4.0	4.0	pF
I_{LATCH}	Latch-up current	Per Jedec JC40.2 Standard 17	500	500	mA
f_{MAX}	Maximum clock frequency	C_L = 50pF	125	110	MHz

Note:

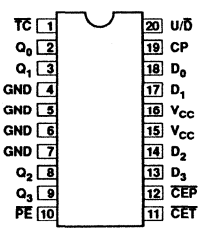
1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_I + \Sigma (C_L \times V_{CC}^2 \times f_O)$ where:
   f_I = input frequency in MHz, C_L = output load capacitance in pF,
   f_O = output frequency in MHz, V_{CC} = supply voltage in V,
   $\Sigma (C_L \times V_{CC}^2 \times f_O)$ = sum of outputs

ORDERING INFORMATION

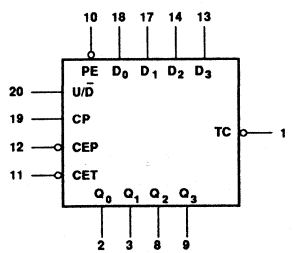
PACKAGES	TEMPERATURE RANGE	ORDER CODE
20-pin plastic DIP (300mil-wide)	-40°C to +85°C	74AC11169N 74ACT11169N
20-pin plastic SO (300mil-wide)	-40°C to +85°C	74AC11169D 74ACT11169D

PIN CONFIGURATION

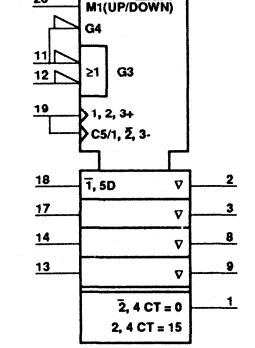
N and D Packages



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



applications in high-speed counting designs. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when so instructed by the Count Enable inputs and internal gating. This mode of operation eliminates the output spikes which are normally associated with asynchronous (ripple clock) counters. A buffered Clock input triggers the flip-flops on the Low-to-High transition of the clock.

The counter is fully programmable; that is, the outputs may be preset to either level.

Presetting is synchronous with the clock and takes place regardless of the levels of the Count Enable inputs. A Low level on the Parallel Enable ($\overline{PE}$) input disables the counter and causes the data at the D_n input to be loaded into the counter on the next Low-to-High transition of the clock.

The direction of counting is controlled by the Up/Down (U/$\overline{D}$) input; a High will cause the count to increase, a Low will cause the count to decrease.

The Carry look-ahead circuitry provides for cascading counters for n-bit synchronous applications without additional gating. Instrumental in accomplishing this function are two Count Enable inputs ($\overline{CET}$•$\overline{CEP}$) and a Terminal Count ($\overline{TC}$) output. Both Count Enable inputs must be Low to count. The $\overline{CET}$ input is fed forward to enable the $\overline{TC}$ output. The $\overline{TC}$ output thus enabled will produce a Low output pulse with a duration approximately equal to the High level portion or Low level portion of the Q_0 output depending on the state of the U/$\overline{D}$ input. This Low level $\overline{TC}$ pulse is used to enable successive cascaded stages. See Figure 1 for the fast synchronous multi-stage counting connections.

FUNCTIONAL DESCRIPTION

The AC/ACT11169 uses edge-triggered D-type flip-flops and has no constraints on changing the control or data input signals in either state of the Clock. The only requirement is that the various inputs attain the desired state at least a setup time before the rising edge of the Clock and remain valid for the recommended hold time thereafter. The parallel load operation takes precedence over the other operations, as indicated in the Mode Select Table. When $\overline{PE}$ is Low, the data on the D_0 - D_3 inputs enter the flip-flops on the next rising edge of the Clock. In order for counting to occur, both $\overline{CEP}$ and $\overline{CET}$ must be Low and $\overline{PE}$ must be High; the U/$\overline{D}$ input then determines the direction of counting. The Terminal Count ($\overline{TC}$) output is normally High and goes Low when a counter reaches zero in the Count Down mode or reaches 9 in the Count Up mode, provided that $\overline{CET}$ is Low. The $\overline{TC}$ output state is not a function of the Count Enable Parallel ($\overline{CEP}$) input level. The $\overline{TC}$ output of the AC/ACT11169 decade counter can also be Low in the illegal states 11, 13, 15, which can occur when power is turned on or via parallel loading. If an illegal state occurs, the AC/ACT11169 will return to the legitimate sequence within six counts. The $\overline{TC}$ signal is derived by decoding the D-input signals of the counter flip-flops and using this decoded signal as the D-input driving the $\overline{TC}$ output. Use of this configuration gives a $\overline{TC}$ output which is free of decoding spikes. The possibility exists that on pwer-up that the $\overline{TC}$ output may not give a true indication of the state of the counter (i.e., $\overline{TC}$ may be Low while the counter is not at terminal count or High when it is at terminal count.) Should this occur, $\overline{TC}$ will always go to a correct state on the first Low-to-High transition of the clock.

1) Count Enable = $\overline{CEP} \cdot \overline{CET} \cdot \overline{PE}$

2) Up: $\overline{TC} = Q_0 \cdot Q_3 \cdot (U/\overline{D}) \cdot \overline{CET}$

3) Down: $\overline{TC} = \overline{Q}_0 \cdot \overline{Q}_1 \cdot \overline{Q}_2 \cdot \overline{Q}_3 \cdot \overline{(U/\overline{D})} \cdot \overline{CET}$

PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
20	U/$\overline{D}$	Up/down count control input
19	CP	Clock input (Low-to-High, edge-triggered)
18, 17, 14, 13	D_0 - D_3	Data inputs
12	$\overline{CEP}$	Count enable parallel input (active Low)
11	$\overline{CET}$	Count enable trickle input (active Low)
12	$\overline{PE}$	Parallel enable input (active Low)
2, 3, 8, 9	Q_0 - Q_3	Counter outputs
1	$\overline{TC}$	Terminal count output (active Low)
4, 5, 6, 7	GND	Ground (0V)
15, 16	V_{CC}	Positive supply voltage

MODE SELECT TABLE

$\overline{PE}$	$\overline{CEP}$	$\overline{CET}$	U/$\overline{D}$	ACTION ON RISING CLOCK EDGE
L	X	X	X	Load ($D_n \rightarrow Q_n$)
H	L	L	H	Count up (increment)
H	L	L	L	Count down (decrement)
H	H	X	X	No change (hold)
H	X	H	X	

H = High voltage level
L = Low voltage level
X = Don't care

Synchronous Presettable 4-Bit Up/Down Binary Counter

74AC/ACT11169

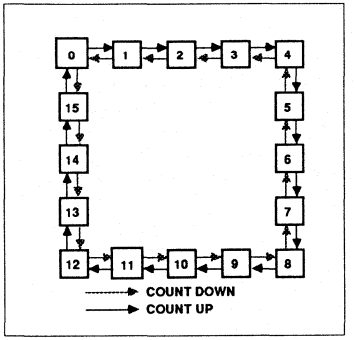
MODE SELECT—FUNCTION TABLE

OPERATING MODE	INPUTS						OUTPUTS	
	CP	U/$\overline{D}$	$\overline{CEP}$	$\overline{CET}$	$\overline{PE}$	D_n	Q_n	$\overline{TC}$
Parallel load	↑	X	X	X	l	l	L	(1)
	↑	X	X	X	l	h	H	(1)
Count up	↑	h	l	l	h	X	Count up	(1)
Count down	↑	l	l	l	h	X	Count down	(1)
Hold (do nothing)	↑	X	h	X	h	X	q_n	(1)
	↑	X	X	h	h	X	q_n	H

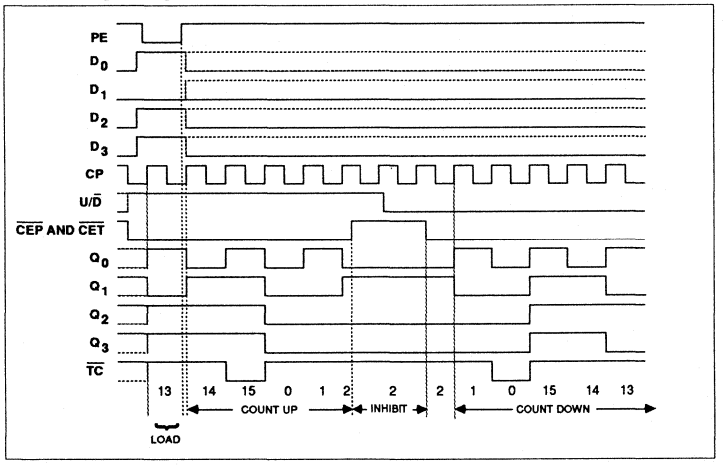
H = High voltage level steady state
h = High voltage level one setup time prior to the Low-to-High clock transition
L = Low voltage level steady state
l = Low voltage level one setup time prior to the Low-to-High clock transition
X = Don't care
q = State of the referenced output prior to the Low-to-High clock transition
↑ =Low-to-High clock transition

NOTES:
1. $\overline{TC}$ is Low when $\overline{CET}$ is Low and the counter is at Terminal Count. Terminal Count Up is (HHHH) and Terminal Count Down is (LLLL).

STATE DIAGRAM



TIMING DIAGRAM



Synchronous Presettable 4-Bit Up/Down Binary Counter

74AC/ACT11169

LOGIC DIAGRAM

UNDER DEVELOPMENT

APPLICATIONS

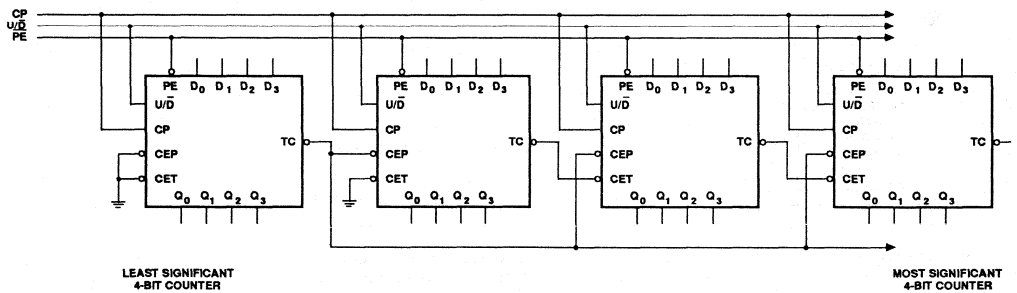


Figure 1. Synchronous Multistage Counting Scheme

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	74AC11169			74ACT11169			UNIT
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	DC supply voltage	3.0[1]	5.0	5.5	4.5	5.0	5.5	V
V_I	Input voltage	0		V_{CC}	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	0		V_{CC}	V
$\Delta t/\Delta v$	Input transition rise or fall rate	0		10	0		10	ns/V
T_A	Operating free-air temperature	-40		+85	-40		+85	°C

NOTE:

1. No electrical or switching characteristics are specified at $V_{CC} < 3V$. Operation between 2V and 3V is not recommended, but within that range, a device output will maintain a previously established logic state.

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	TEST CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 to+7.0	V
I_{IK} or V_I	DC input diode current[2]	$V_I < 0$	-20	mA
		$V_I > V_{CC}$	20	
	DC input voltage		-0.5 to V_{CC} +0.5	V
I_{OK} or V_O	DC output diode current[2]	$V_O < 0$	-50	mA
		$V_O > V_{CC}$	50	
	DC output voltage		-0.5 to V_{CC} +0.5	V
I_O	DC output source or sink current per output pin	V_O = 0 to V_{CC}	±50	mA
I_{CC} or I_{GND}	DC V_{CC} current		±125	mA
	DC ground current		±125	
T_{STG}	Storage temperature		-65 to 150	°C
P_{TOT}	Power dissipation per package Plastic DIP	Above 70°C:derate linearly by 8mW/K	500	mW
	Power dissipation per package Plastic surface mount (SO)	Above 70°C:derate linearly by 6mW/K	400	mW

NOTES:

1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		V_{CC}	74AC11169				74ACT11169				UNIT
					T_A = +25°C		T_A = -40°C to +85°C		T_A = +25°C		T_A = -40°C to +85°C		
				V	Min	Max	Min	Max	Min	Max	Min	Max	
V_{IH}	High-level input voltage			3.0	2.10		2.10						V
				4.5	3.15		3.15		2.0		2.0		
				5.5	3.85		3.85		2.0		2.0		
V_{IL}	Low-level input voltage			3.0		0.90		0.90					V
				4.5		1.35		1.35		0.8		0.8	
				5.5		1.65		1.65		0.8		0.8	
V_{OH}	High-level output voltage	V_I = V_{IL} or V_{IH}	I_{OH} = -50μA	3.0	2.9		2.9						V
				4.5	4.4		4.4		4.4		4.4		
				5.5	5.4		5.4		5.4		5.4		
			I_{OH} = -4mA	3.0	2.58		2.48						
			I_{OH} = -24mA	4.5	3.94		3.8		3.94		3.8		
				5.5	4.94		4.8		4.94		4.8		
			I_{OH} = -75mA[1]	5.5			3.85				3.85		
V_{OL}	Low-level output voltage	V_I = V_{IL} or V_{IH}	I_{OL} = 50μA	3.0		0.1		0.1					V
				4.5		0.1		0.1		0.1		0.1	
				5.5		0.1		0.1		0.1		0.1	
			I_{OL} = 12mA	3.0		0.36		0.44					
			I_{OL} = 24mA	4.5		0.36		0.44		0.36		0.44	
				5.5		0.36		0.44		0.36		0.44	
			I_{OL} = 75mA[1]	5.5				1.65				1.65	
I_I	Input leakage current	V_I = V_{CC} or GND		5.5		±0.1		±1.0		±0.1		±1.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC} or GND, I_O = 0		5.5		8.0		80		8.0		80	μA
ΔI_{CC}	Supply current, TTL inputs High[2]	One input at 3.4V, other inputs at V_{CC} or GND		5.5						0.9		1.0	mA

NOTES:
1. Not more than one output should be tested at a time, and the duration of the test should not exceed 10ms.
2. This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0V or V_{CC}.

74AC/ACT11174

Hex D-Type Flip-Flop w/Reset; Positive-Edge Trigger

Objective Specification

FEATURES

- **Output capability: ±24 mA**
- **CMOS (AC) and TTL (ACT) voltage level inputs**
- **50Ω incident wave switching**
- **Center-pin V_{CC} and ground configuration to minimize high-speed switching noise**
- **I_{CC} category: MSI**

DESCRIPTION

The 74AC/ACT11174 high-performance CMOS devices combine very high speed and high output drive comparable to the most advanced TTL families.

The 74AC/ACT11174 provides six D-type flip-flops with independent Data inputs, shared Clock and Master Reset inputs, and Q outputs.

Master Reset ($\overline{MR}$) is an asynchronous active-Low input and operates independently of the Clock input. Information on the Data (D) input is transferred to the Q output on the Low-to-High transition of the clock pulse. Clock triggering is threshold voltage dependent. The D inputs must be stable one set-up time prior to the Low-to-High clock transition for predictable operation.

GENERAL INFORMATION

SYMBOL	PARAMETER	CONDITIONS T_A = 25°C; GND = 0V V_{CC} = 5.0V	TYPICAL		UNIT
			AC	ACT	
t_{PLH}/ t_{PHL}	Propagation delay CP to Q_n	C_L = 50pF	4.4	5.5	ns
C_{PD}	Power dissipation capacitance per flip-flop[1]	f = 1MHz; C_L = 50pF	31	30	pF
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	4.0	4.0	pF
I_{LATCH}	Latch-up current	Per Jedec JC40.2 Standard 17	500	500	mA
f_{MAX}	Maximum clock frequency	C_L = 50 pF	160	150	MHz

Note:

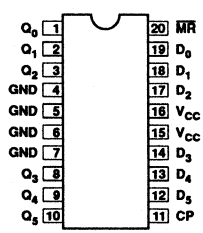
1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_O)$ where:
   f_i = input frequency in MHz, C_L = output load capacitance in pF,
   f_O = output frequency in MHz, V_{CC} = supply voltage in V,
   $\Sigma (C_L \times V_{CC}^2 \times f_O)$ = sum of outputs

ORDERING INFORMATION

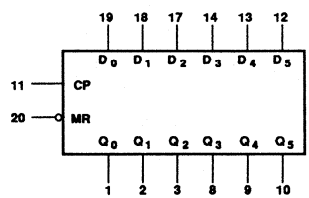
PACKAGES	TEMPERATURE RANGE	ORDER CODE
20-pin plastic DIP (300mil-wide)	-40°C to +85°C	74AC11174N 74ACT11174N
20-pin plastic SO (300mil-wide)	-40°C to +85°C	74AC11174D 74ACT11174D

PIN CONFIGURATION

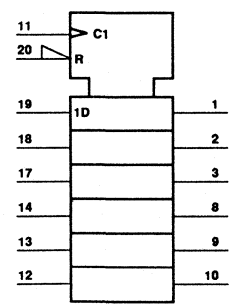
N and D Packages



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



Hex D-Type Flip-Flop w/Reset; Positive-Edge Trigger

74AC/ACT11174

PIN DESCRIPTION

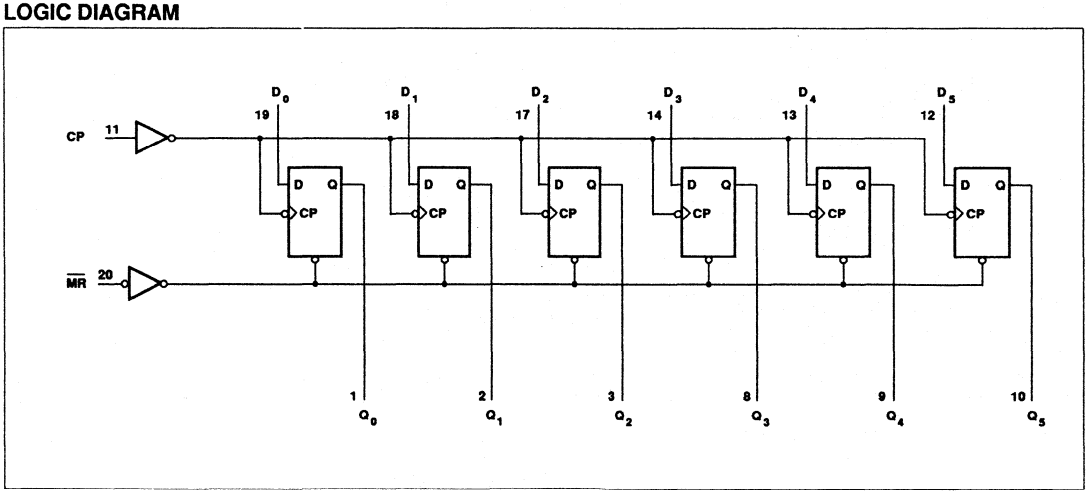
PIN NUMBER	SYMBOL	NAME AND FUNCTION
19, 18, 17, 14, 13, 12	D_0 - D_5	Data inputs
1, 2, 3, 8, 9, 10	Q_0 - Q_5	Data outputs
20	$\overline{MR}$	Master reset input (active Low)
11	CP	Clock input
4, 5, 6, 7	GND	Ground (0V)
15, 16	V_{CC}	Positive supply voltage

FUNCTION TABLE

OPERATING MODE	INPUTS			OUTPUTS
	$\overline{MR}$	CP	D_n	Q_n
Asynchronous reset	L	X	X	L
Load "1" (set)	H	↑	h	H
Load "0" (reset)	H	↑	l	L

H = High voltage level steady state
h = High voltage level one set-up time prior to the Low-to-High clock transition
L = Low voltage level steady state
l = Low voltage level one set-up time prior to the Low-to-High clock transition
X = Don't care
↑ = Low-to-High clock transition

LOGIC DIAGRAM



RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	74AC11174			74ACT11174			UNIT
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	DC supply voltage	3.0[1]	5.0	5.5	4.5	5.0	5.5	V
V_I	Input voltage	0		V_{CC}	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	0		V_{CC}	V
$\Delta t/\Delta v$	Input transition rise or fall rate	0		10	0		10	ns/V
T_A	Operating free-air temperature	-40		+85	-40		+85	°C

NOTE:

1. No electrical or switching characteristics are specified at V_{CC} < 3V. Operation between 2V and 3V is not recommended, but within that range, a device output will maintain a previously established logic state.

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	TEST CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 to+7.0	V
I_{IK} or V_I	DC input diode current[2]	$V_I < 0$	-20	mA
		$V_I > V_{CC}$	20	
	DC input voltage		-0.5 to V_{CC} +0.5	V
I_{OK} or V_O	DC output diode current[2]	$V_O < 0$	-50	mA
		$V_O > V_{CC}$	50	
	DC output voltage		-0.5 to V_{CC} +0.5	V
I_O	DC output source or sink current per output pin	V_O = 0 to V_{CC}	±50	mA
I_{CC} or I_{GND}	DC V_{CC} current		±150	mA
	DC ground current		±150	
T_{STG}	Storage temperature		-65 to 150	°C
P_{TOT}	Power dissipation per package Plastic DIP	Above 70°C:derate linearly by 8mW/K	500	mW
	Power dissipation per package Plastic surface mount (SO)	Above 70°C:derate linearly by 6mW/K	400	mW

NOTES:

1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		V_{CC}	74AC11174				74ACT11174				UNIT
					T_A = +25°C		T_A = -40°C to +85°C		T_A = +25°C		T_A = -40°C to +85°C		
				V	Min	Max	Min	Max	Min	Max	Min	Max	
V_{IH}	High-level input voltage			3.0	2.10		2.10						V
				4.5	3.15		3.15		2.0		2.0		
				5.5	3.85		3.85		2.0		2.0		
V_{IL}	Low-level input voltage			3.0		0.90		0.90					V
				4.5		1.35		1.35		0.8		0.8	
				5.5		1.65		1.65		0.8		0.8	
V_{OH}	High-level output voltage	V_I = V_{IL} or V_{IH}	I_{OH} = -50μA	3.0	2.9		2.9						V
				4.5	4.4		4.4		4.4		4.4		
				5.5	5.4		5.4		5.4		5.4		
			I_{OH} = -4mA	3.0	2.58		2.48						
			I_{OH} = -24mA	4.5	3.94		3.8		3.94		3.8		
				5.5	4.94		4.8		4.94		4.8		
			I_{OH} = -75mA[1]	5.5			3.85				3.85		
V_{OL}	Low-level output voltage	V_I = V_{IL} or V_{IH}	I_{OL} = 50μA	3.0		0.1		0.1					V
				4.5		0.1		0.1		0.1		0.1	
				5.5		0.1		0.1		0.1		0.1	
			I_{OL} = 12mA	3.0		0.36		0.44					
			I_{OL} = 24mA	4.5		0.36		0.44		0.36		0.44	
				5.5		0.36		0.44		0.36		0.44	
			I_{OL} = 75mA[1]	5.5				1.65				1.65	
I_I	Input leakage current	V_I = V_{CC} or GND		5.5		±0.1		±1.0		±0.1		±1.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC} or GND, I_O = 0		5.5		8.0		80		8.0		80	μA
ΔI_{CC}	Supply current, TTL inputs High[2]	One input at 3.4V, other inputs at V_{CC} or GND		5.5						0.9		1.0	mA

NOTES:
1. Not more than one output should be tested at a time, and the duration of the test should not exceed 10ms.
2. This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0V or V_{CC}.

74AC/ACT11175

Quad D-Type Flip-Flop w/Reset; Positive-Edge Trigger

Preliminary Specification

FEATURES

- **Output capability: ±24 mA**
- **CMOS (AC) and TTL (ACT) voltage level inputs**
- **50Ω incident wave switching**
- **Center-pin V_{CC} and ground configuration to minimize high-speed switching noise**
- **I_{CC} category: MSI**

DESCRIPTION

The 74AC/ACT11175 high-performance CMOS devices combine very high speed and high output drive comparable to the most advanced TTL families.

The 74AC/ACT11175 provides four D-type flip-flops with independent Data inputs, shared Clock and Master Reset inputs, and complementary Q and $\overline{Q}$ outputs.

Master Reset ($\overline{MR}$) is an asynchronous active-Low input and operates independently of the Clock input. Information on the Data (D) input is transferred to the Q output on the Low-to-High transition of the clock pulse. Clock triggering is threshold voltage dependent. The D inputs must be stable one set-up time prior to the Low-to-High clock transition for predictable operation.

GENERAL INFORMATION

SYMBOL	PARAMETER	CONDITIONS T_A = 25°C; GND = 0V; V_{CC} = 5.0V	TYPICAL		UNIT
			AC	ACT	
t_{PLH}/t_{PHL}	Propagation delay CP to Q_n or $\overline{Q}_n$	C_L = 50pF	6.3	7.3	ns
C_{PD}	Power dissipation capacitance per flip-flop[1]	f = 1MHz; C_L = 50pF	47	42	pF
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	3.5	3.5	pF
I_{LATCH}	Latch-up current	Per Jedec JC40.2 Standard 17	500	500	mA
f_{MAX}	Maximum clock frequency	C_L = 50pF	135	120	MHz

Note:

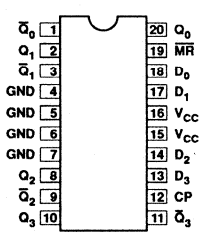
1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_I + \Sigma (C_L \times V_{CC}^2 \times f_O)$ where:
   f_I = input frequency in MHz, C_L = output load capacitance in pF,
   f_O = output frequency in MHz, V_{CC} = supply voltage in V,
   $\Sigma (C_L \times V_{CC}^2 \times f_O)$ = sum of outputs

ORDERING INFORMATION

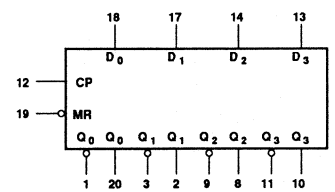
PACKAGES	TEMPERATURE RANGE	ORDER CODE
20-pin plastic DIP (300mil-wide)	-40°C to +85°C	74AC11175N 74ACT11175N
20-pin plastic SO (300mil-wide)	-40°C to +85°C	74AC11175D 74ACT11175D

PIN CONFIGURATION

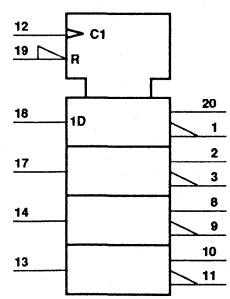
N and D Packages



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



Quad D-Type Flip-Flop w/Reset; Positive-Edge Trigger

74AC/ACT11175

PIN DESCRIPTION

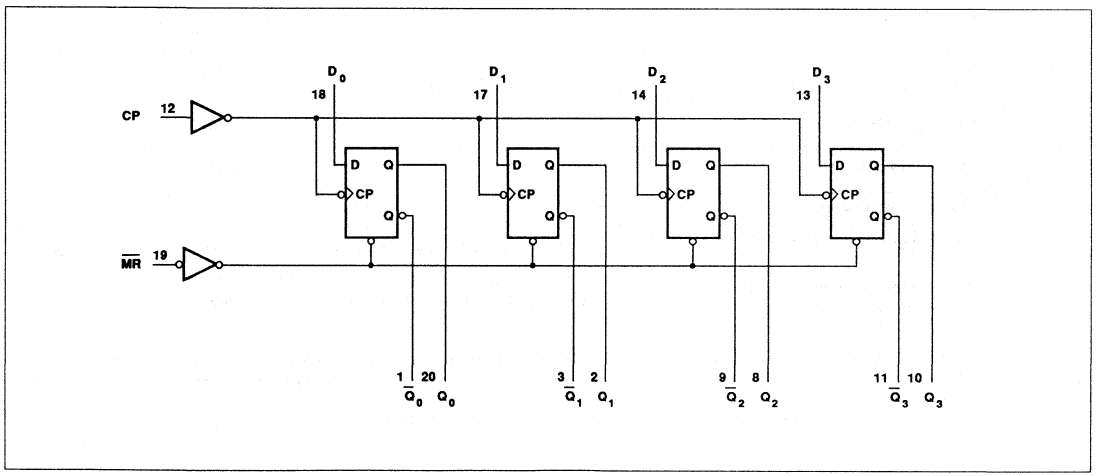
PIN NUMBER	SYMBOL	NAME AND FUNCTION
18, 17, 14, 13	D_0 - D_3	Data inputs
20, 2, 8, 10	Q_0 - Q_3	Data outputs
1, 3, 9, 11	$\overline{Q}_0$ - $\overline{Q}_3$	Data outputs (complements of Q_n outputs)
19	$\overline{MR}$	Master reset input (active Low)
12	CP	Clock input
4, 5, 6, 7	GND	Ground (0V)
15, 16	V_{CC}	Positive supply voltage

FUNCTION TABLE

OPERATING MODE	INPUTS			OUTPUTS	
	$\overline{MR}$	CP	D_n	Q_n	$\overline{Q}_n$
Asynchronous reset	L	X	X	L	H
Load "1" (set)	H	↑	h	H	L
Load "0" (reset)	H	↑	l	L	H

H = High voltage level steady state
h = High voltage level one set-up time prior to the Low-to-High clock transition
L = Low voltage level steady state
l = Low voltage level one set-up time prior to the Low-to-High clock transition
X = Don't care
↑ = Low-to-High clock transition

LOGIC DIAGRAM



RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	74AC11175			74ACT11175			UNIT
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	DC supply voltage	3.0[1]	5.0	5.5	4.5	5.0	5.5	V
V_I	Input voltage	0		V_{CC}	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	0		V_{CC}	V
$\Delta t/\Delta v$	Input transition rise or fall rate	0		10	0		10	ns/V
T_A	Operating free-air temperature	-40		+85	-40		+85	°C

NOTE:
1. No electrical or switching characteristics are specified at V_{CC} < 3V. Operation between 2V and 3V is not recommended, but within that range, a device output will maintain a previously established logic state.

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	TEST CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 to+7.0	V
I_{IK} or V_I	DC input diode current[2]	$V_I < 0$	-20	mA
		$V_I > V_{CC}$	20	
	DC input voltage		-0.5 to V_{CC} +0.5	V
I_{OK} or V_O	DC output diode current[2]	$V_O < 0$	-50	mA
		$V_O > V_{CC}$	50	
	DC output voltage		-0.5 to V_{CC} +0.5	V
I_O	DC output source or sink current per output pin	V_O = 0 to V_{CC}	±50	mA
I_{CC} or I_{GND}	DC V_{CC} current		±200	mA
	DC ground current		±200	
T_{STG}	Storage temperature		-65 to 150	°C
P_{TOT}	Power dissipation per package Plastic DIP	Above 70°C:derate linearly by 8mW/K	500	mW
	Power dissipation per package Plastic surface mount (SO)	Above 70°C:derate linearly by 6mW/K	400	mW

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		V_{CC}	74AC11175				74ACT11175				UNIT
					T_A = +25°C		T_A = -40°C to +85°C		T_A = +25°C		T_A = -40°C to +85°C		
				V	Min	Max	Min	Max	Min	Max	Min	Max	
V_{IH}	High-level input voltage			3.0	2.10		2.10						V
				4.5	3.15		3.15		2.0		2.0		
				5.5	3.85		3.85		2.0		2.0		
V_{IL}	Low-level input voltage			3.0		0.90		0.90					V
				4.5		1.35		1.35		0.8		0.8	
				5.5		1.65		1.65		0.8		0.8	
V_{OH}	High-level output voltage	V_I = V_{IL} or V_{IH}	I_{OH} = -50μA	3.0	2.9		2.9						V
				4.5	4.4		4.4		4.4		4.4		
				5.5	5.4		5.4		5.4		5.4		
			I_{OH} = -4mA	3.0	2.58		2.48						
			I_{OH} = -24mA	4.5	3.94		3.8		3.94		3.8		
				5.5	4.94		4.8		4.94		4.8		
			I_{OH} = -75mA[1]	5.5			3.85				3.85		
V_{OL}	Low-level output voltage	V_I = V_{IL} or V_{IH}	I_{OL} = 50μA	3.0		0.1		0.1					V
				4.5		0.1		0.1		0.1		0.1	
				5.5		0.1		0.1		0.1		0.1	
			I_{OL} = 12mA	3.0		0.36		0.44					
			I_{OL} = 24mA	4.5		0.36		0.44		0.36		0.44	
				5.5		0.36		0.44		0.36		0.44	
			I_{OL} = 75mA[1]	5.5				1.65				1.65	
I_I	Input leakage current	V_I = V_{CC} or GND		5.5		±0.1		±1.0		±0.1		±1.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC} or GND, I_O = 0		5.5		8.0		80		8.0		80	μA
ΔI_{CC}	Supply current, TTL inputs High[2]	One input at 3.4V, other inputs at V_{CC} or GND		5.5						0.9		1.0	mA

NOTES:
1. Not more than one output should be tested at a time, and the duration of the test should not exceed 10ms.
2. This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0V or V_{CC}.

AC ELECTRICAL CHARACTERISTICS AT 3.3V ±0.3V

SYMBOL	PARAMETER	WAVEFORM	74AC11175					UNIT
			T_A = +25°C			T_A = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	1	100	115		100		MHz
t_{PLH} t_{PHL}	Propagation delay CP to Q_n, $\overline{Q}_n$	1	1.5 1.5	7.8 10.8	10.0 13.7	1.5 1.5	10.9 14.6	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{MR}$ to Q_n, $\overline{Q}_n$	2	1.5 1.5	7.9 11.4	9.8 13.7	1.5 1.5	10.6 14.6	ns
t_S	Setup time, High or Low D_n to CP	1	8.0			8.0		ns
t_H	Hold time, High or Low CP to D_n	1	0.0			0.0		ns
t_W	Clock pulse width High or Low	1	5.0			5.0		ns
t_W	$\overline{MR}$ pulse width, Low	2	5.0			5.0		ns
t_{REC}	Recovery time $\overline{MR}$ to CP	3	1.0			1.0		ns

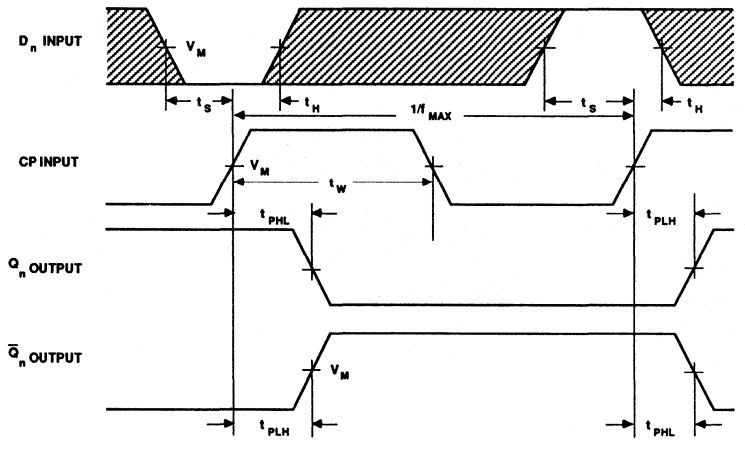
AC ELECTRICAL CHARACTERISTICS AT 5.0V ±0.5V

SYMBOL	PARAMETER	WAVEFORM	74AC11175					UNIT
			T_A = +25°C			T_A = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	1	110	135		110		MHz
t_{PLH} t_{PHL}	Propagation delay CP to Q_n, $\overline{Q}_n$	1	1.5 1.5	5.4 7.2	7.2 9.8	1.5 1.5	7.8 10.7	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{MR}$ to Q_n, $\overline{Q}_n$	2	1.5 1.5	5.4 8.1	7.0 9.8	1.5 1.5	7.5 10.7	ns
t_S	Setup time, High or Low D_n to CP	1	5.5			5.5		ns
t_H	Hold time, High or Low CP to D_n	1	0.5			0.5		ns
t_W	Clock pulse width High or Low	1	4.5			4.5		ns
t_W	$\overline{MR}$ pulse width, Low	2	4.5			4.5		ns
t_{REC}	Recovery time $\overline{MR}$ to CP	3	1.0			1.0		ns

AC ELECTRICAL CHARACTERISTICS AT 5.0V ±0.5V

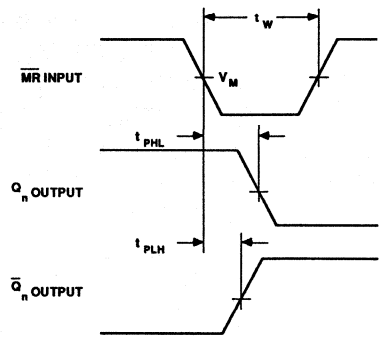
SYMBOL	PARAMETER	WAVEFORM	74ACT11175					UNIT
			T_A = +25°C			T_A = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	1	100	120		100		MHz
t_{PLH} t_{PHL}	Propagation delay CP to Q_n, $\overline{Q}_n$	1	1.5 1.5	6.1 8.4	7.8 10.6	1.5 1.5	8.3 11.6	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{MR}$ to Q_n, $\overline{Q}_n$	2	1.5 1.5	6.9 9.5	8.4 11.6	1.5 1.5	8.9 12.5	ns
t_S	Setup time, High or Low D_n to CP	1	5.5			5.5		ns
t_H	Hold time, High or Low CP to D_n	1	1.0			1.0		ns
t_W	Clock pulse width High or Low	1	5.0			5.0		ns
t_W	$\overline{MR}$ pulse width, Low	2	5.0			5.0		ns
t_{REC}	Recovery time $\overline{MR}$ to CP	3	1.5			1.5		ns

AC WAVEFORMS

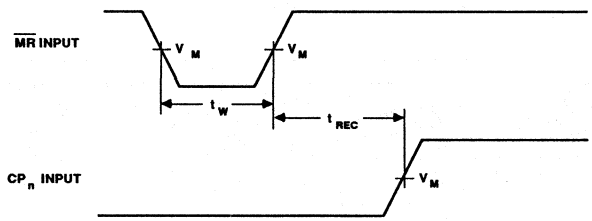


Waveform 1. Waveforms Showing Clock to Output Delays, Data Setup, and Clock Pulse Width

AC WAVEFORMS (Continued)



Waveform 2. Waveforms Showing Master Reset to Output Delay and Master Reset Pulse Width

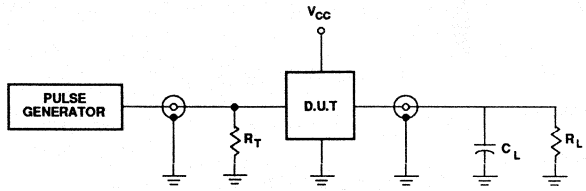


Waveform 3. Waveforms Showing Recovery Time

WAVEFORM CONDITIONS

	INPUTS	OUTPUTS
AC	V_{IN} = GND to V_{CC}, V_M = 50% V_{CC}	V_{OUT} = V_{OL} to V_{OH}
ACT	V_{IN} = GND to 3.0V, V_M = 1.5V	V_M = 50% V_{CC}

TEST CIRCUIT



Test Circuit

DEFINITIONS

C_L = Load capacitance, 50pF; includes jig and probe capacitance

R_L = Load resistor, 500Ω

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators

Input pulses: PRR ≤ 10MHz

$t_r = t_f$ = 3ns

74AC/ACT11181

4-Bit Arithmetic Logic Unit

Objective Specification

FEATURES

- **Provides 16 arithmetic operations: add, subtract, compare, and double; plus 12 other arithmetic operations**
- **Provides all 16 logic operations of two variables: Exclusive-OR, Compare, AND, NAND, NOR, OR, plus 10 other logic operations**
- **Full look-ahead Carry for high-speed arithmetic operation on long words**
- **Output capability: ±24 mA**
- **CMOS (AC) and TTL (ACT) voltage level inputs**
- **50Ω incident wave switching**
- **Center-pin V_{CC} and ground configuration to minimize high-speed switching noise**
- **I_{CC} category: MSI**

DESCRIPTION

The 74AC/ACT11181 high-performance CMOS devices combine very high speed and high output drive comparable to the most advanced TTL families.

GENERAL INFORMATION

SYMBOL	PARAMETER	CONDITIONS T_A = 25°C; GND = 0V; V_{CC} = 5.0V	TYPICAL		UNIT
			AC	ACT	
t_{PLH}/ t_{PHL}	Propagation delay $\overline{A}_i$ or $\overline{B}_i$ to $\overline{F}_i$ (sum mode)	C_L = 50pF	9.5	11.6	ns
C_{PD}	Power dissipation capacitance[1]	f = 1MHz; C_L = 50pF	119	119	pF
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	4.5	4.5	pF
C_{OUT}	Output capacitance	V_O = 0V or V_{CC} (A = B)	11	11	pF
I_{LATCH}	Latch-up current	Per Jedec JC40.2 Standard 17	500	500	mA

Note:

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_I + \Sigma (C_L \times V_{CC}^2 \times f_O)$ where:
   f_I = input frequency in MHz, C_L = output load capacitance in pF,
   f_O = output frequency in MHz, V_{CC} = supply voltage in V,
   $\Sigma (C_L \times V_{CC}^2 \times f_O)$ = sum of outputs

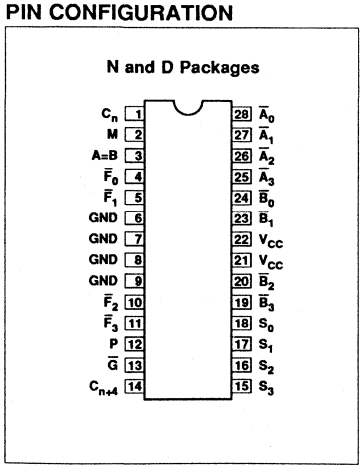
ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE
28-pin plastic DIP (300mil-wide)	-40°C to +85°C	74AC11181N 74ACT11181N
28-pin plastic SO (300mil-wide)	-40°C to +85°C	74AC11181D 74ACT11181D

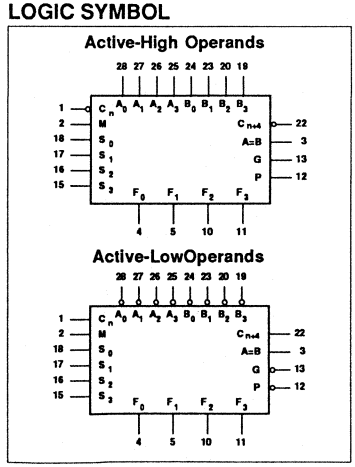
The 74AC/ACT11181 arithmetic logic units (ALU) are controlled by the four Function Select inputs (S_0 - S_3) and the Mode Control input (M) and can perform all the 16 possible logic operations or 16 different arithmetic operations on active-High or active-Low operands. The Function Tables list these operations.

When the Mode Control input (M) is High, all internal carries are inhibited and the device performs logic operations on the individual bits as listed. When the Mode

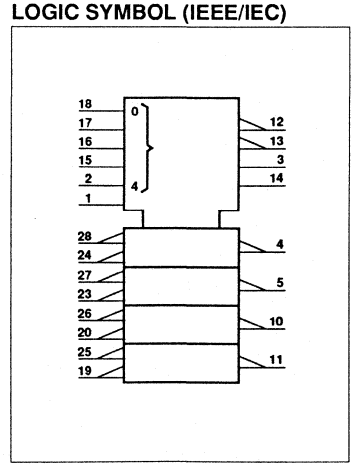
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



Control input is Low, the carries are enabled and the device performs arithmetic operations on the two 4-bit words. The device incorporates full internal carry look-ahead and provides for either ripple carry between devices using the C_{n+4} output, or for carry look-ahead between packages using the signals $\overline{P}$ (Carry Propagate) and $\overline{G}$ (Carry Generate). $\overline{P}$ and $\overline{G}$ are not affected by carry in. When speed requirements are not stringent, it can be used in a simple ripple carry mode by connecting the Carry output ($C_{n+}4$) signal to the Carry input (C_n) of the next unit. For high-speed operation the device is used in conjunction with the 74AC/ACT11882 carry look-ahead circuit. One carry look-ahead package is required for each group of eight 74AC/ACT11181 devices. Carry look-ahead can be provided at various levels and offers high-speed capability over extremely long word lengths.

The A = B output from the device goes High when all four $\overline{F}$ outputs are High and can be used to indicate logic equivalence over 4 bits when the unit is in the subtract mode. The A = B output is open-collector and can be wired-AND with other A = B outputs to give a comparison for more than 4 bits. The A = B signal can also be used with the C_{n+4} signal to indicate A > B and A < B.

The Function Tables list both the arithmetic operations that are performed without a carry in and with a carry in. Note that a carry adds a one to each operation. Thus, select code LHHL generates A minus B minus 1 (two's complement notation) without a carry in and generates A minus B when a carry is applied. Because subtraction is actually performed by complementary addition (one's complement), a carry out means borrow; thus a carry is generated when there is no underflow and no carry is generated when there is underflow.

As indicated, this device can be used with either active-Low inputs producing active-Low outputs or with active-High inputs producing active-High outputs. For either case, the tables list the operations that are performed to the operands labeled inside the logic symbol.

PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
2	M	Mode control input
28, 27, 26, 25	$\overline{A}_0$ - $\overline{A}_3$	$\overline{A}$ operand inputs
24, 23, 20, 19	$\overline{B}_0$ - $\overline{B}_3$	$\overline{B}$ operand inputs
18, 17, 16, 15	S_0 - S_3	Function select inputs
1	C_n	Carry input
14	C_{n+4}	Carry output
3	A = B	Compare output
4, 5, 10, 11	$\overline{F}_0$ - $\overline{F}_3$	Outputs
13	$\overline{G}$	Carry generate output
12	$\overline{P}$	Carry propagate output
6, 7, 8, 9	GND	Ground (0V)
21, 22	V_{CC}	Positive supply voltage

The 74AC/ACT11181 devices will accomdate active-High or active-Low data if the pin designations are interpreted as follows:

PIN NUMBER	28	24	27	23	26	20	25	19	4	5	10	11	1	14	12	13
Active-Low data (Table 1)	$\overline{A}_0$	$\overline{B}_0$	$\overline{A}_1$	$\overline{B}_1$	$\overline{A}_2$	$\overline{B}_2$	$\overline{A}_3$	$\overline{B}_3$	$\overline{F}_0$	$\overline{F}_0$	$\overline{F}_0$	$\overline{F}_0$	C_n	C_{n+4}	$\overline{P}$	$\overline{G}$
Active-High data (Table 2)	A_0	B_0	A_1	B_1	A_2	B_2	A_3	B_3	F_0	F_0	F_0	F_0	$\overline{C}_n$	$\overline{C}_{n+4}$	X	Y

FUNCTION TABLE FOR ACTIVE-LOW DATA

SELECTION				ACTIVE LOW INPUTS & OUTPUTS		
				LOGIC (M = H)	ARITHMETIC** (M = L)	
S3	S2	S1	S0		C_n = L (no carry)	C_n = H (with carry)
L	L	L	L	$\overline{A}$	A minus 1	A
L	L	L	H	$\overline{AB}$	AB minus 1	AB
L	L	H	L	$\overline{A}+B$	$A\overline{B}$ minus 1	$A\overline{B}$
L	L	H	H	Logical 1	minus 1	0 (zero)
L	H	L	L	$\overline{A+B}$	A plus $(A+\overline{B})$	A plus $(A+\overline{B})$ plus 1
L	H	L	H	$\overline{B}$	AB plus $(A+\overline{B})$	AB plus $(A+\overline{B})$ plus 1
L	H	H	L	$\overline{A \oplus B}$	A minus B minus 1	A minus B
L	H	H	H	$A+\overline{B}$	$A+\overline{B}$	$(A+\overline{B})$ plus 1
H	L	L	L	$\overline{AB}$	A plus (A + B)	A plus (A + B) plus 1
H	L	L	H	$A \oplus B$	A plus B	A plus B plus 1
H	L	H	L	B	$A\overline{B}$ plus (A + B)	$A\overline{B}$ plus (A + B) plus 1
H	L	H	H	A + B	(A + B)	(A + B) plus 1
H	H	L	L	Logical 0	A plus A*	A plus A plus 1
H	H	L	H	$A\overline{B}$	AB plus A	AB plus A plus 1
H	H	H	L	AB	A plus $A\overline{B}$	A plus $A\overline{B}$ plus 1
H	H	H	H	A	A	A plus 1

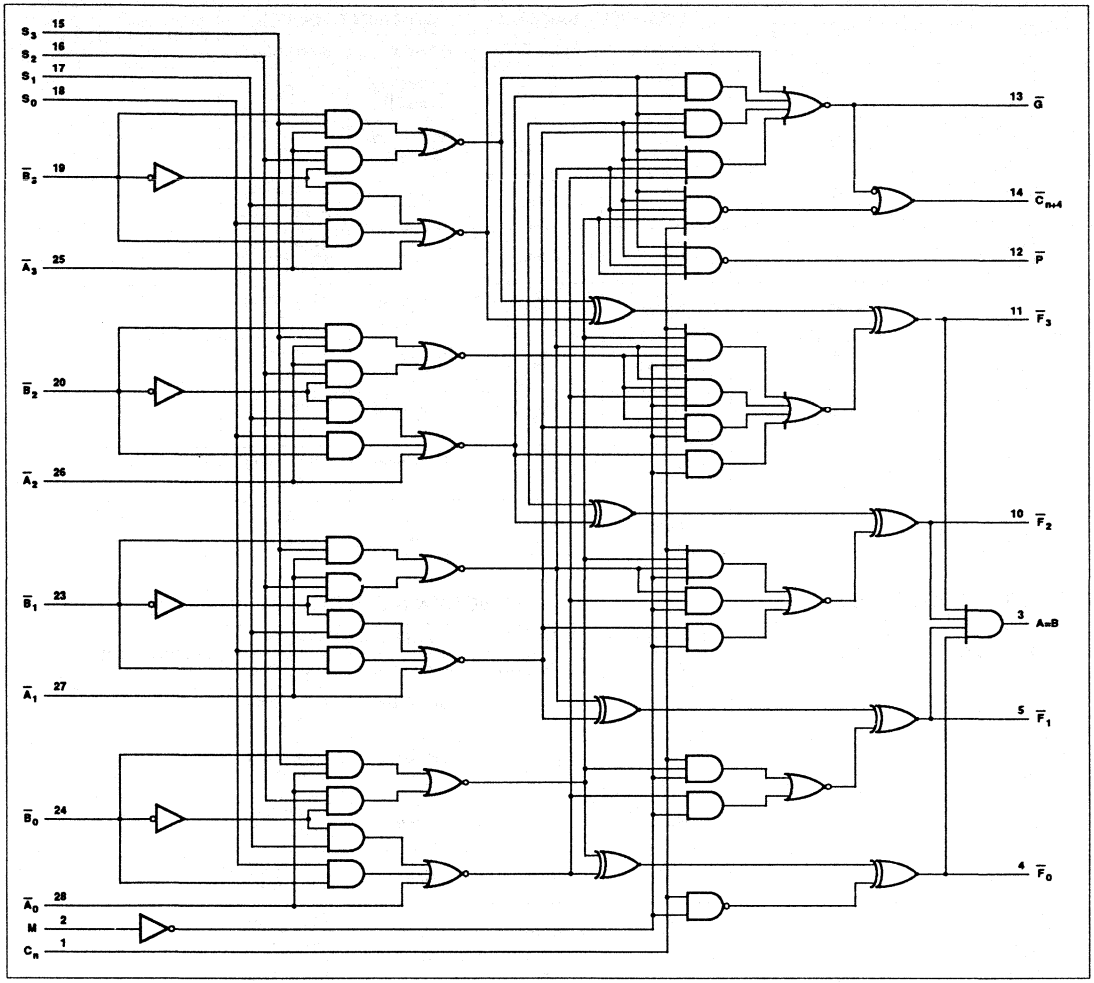
L = Low voltage
H = High voltage level
*Each bit is shifted to the next more significant position.
**Arithmetic operations expressed in two's complement notation.

FUNCTION TABLE FOR ACTIVE-HIGH DATA

SELECTION				ACTIVE HIGH INPUTS & OUTPUTS		
				LOGIC (M = H)	ARITHMETIC** (M = L)	
S3	S2	S1	S0		C_n = H (no carry)	C_n = L (with carry)
L	L	L	L	$\overline{A}$	A	A plus 1
L	L	L	H	$\overline{A+B}$	(A + B)	(A + B) plus 1
L	L	H	L	$\overline{AB}$	$A+\overline{B}$	$(A+\overline{B})$ plus 1
L	L	H	H	Logical 0	minus 1	0 (zero)
L	H	L	L	$\overline{A\overline{B}}$	A plus $A\overline{B}$	A plus $A\overline{B}$ plus 1
L	H	L	H	$\overline{B}$	$A\overline{B}$ plus (A + B)	$A\overline{B}$ plus (A + B) plus 1
L	H	H	L	$A \oplus B$	A minus B minus 1	A minus B
L	H	H	H	$A\overline{B}$	$A\overline{B}$ minus 1	$A\overline{B}$
H	L	L	L	$\overline{A}+B$	AB plus A	AB plus A plus 1
H	L	L	H	$\overline{A \oplus B}$	A plus B	A plus B plus 1
H	L	H	L	B	AB plus $(A+\overline{B})$	AB plus $(A+\overline{B})$ plus 1
H	L	H	H	AB	AB minus 1	AB
H	H	L	L	Logical 1	A plus A*	A plus A plus 1
H	H	L	H	$A+\overline{B}$	A plus (A + B)	A plus (A + B) plus 1
H	H	H	L	A + B	A plus $(A+\overline{B})$	A plus $(A+\overline{B})$ plus 1
H	H	H	H	A	A minus 1	A

L = Low voltage
H = High voltage level
*Each bit is shifted to the next more significant position.
**Arithmetic operations expressed in two's complement notation.

LOGIC DIAGRAM



SUM MODE TEST TABLE I **FUNCTION INPUTS:** $S_0 = S_3 = V_{CC}$, $S_1 = S_2 = M = GND$

PARAMETER	INPUT UNDER TEST	OTHER INPUT, SAME BIT		OTHER DATA INPUTS		OUTPUT UNDER TEST
		Apply V_{CC}	Apply GND	Apply V_{CC}	Apply GND	
t_{PLH} t_{PHL}	$\overline{A}_i$	$\overline{B}_i$	None	Remaining $\overline{A}$ and $\overline{B}$	C_n	$\overline{F}_i$
t_{PLH} t_{PHL}	$\overline{B}_i$	$\overline{A}_i$	None	Remaining $\overline{A}$ and $\overline{B}$	C_n	$\overline{F}_i$
t_{PLH} t_{PHL}	$\overline{A}_i$	$\overline{B}_i$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{P}$
t_{PLH} t_{PHL}	$\overline{B}_i$	$\overline{A}_i$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{P}$
t_{PLH} t_{PHL}	$\overline{A}_i$	None	$\overline{B}_i$	Remaining $\overline{B}$	Remaining $\overline{A}$, C_n	$\overline{G}$
t_{PLH} t_{PHL}	$\overline{B}_i$	None	$\overline{A}_i$	Remaining $\overline{B}$	Remaining C_n	$\overline{G}$
t_{PLH} t_{PHL}	$\overline{A}_i$	None	$\overline{B}_i$	Remaining $\overline{B}$	Remaining $\overline{A}$, C_n	C_{n+4}
t_{PLH} t_{PHL}	$\overline{B}_i$	None	$\overline{A}_i$	Remaining $\overline{B}$	Remaining $\overline{A}$, C_n	C_{n+4}
t_{PLH} t_{PHL}	C_n	None	None	All $\overline{A}$	All $\overline{B}$	Any $\overline{F}$ or C_{n+4}

DIFF MODE TEST TABLE II **FUNCTION INPUTS:** $S_1 = S_2 = V_{CC}$, $S_0 = S_3 = M = GND$

PARAMETER	INPUT UNDER TEST	OTHER INPUT, SAME BIT		OTHER DATA INPUTS		OUTPUT UNDER TEST
		Apply V_{CC}	Apply GND	Apply V_{CC}	Apply GND	
t_{PLH} t_{PHL}	$\overline{A}_i$	None	$\overline{B}_i$	Remaining $\overline{A}$	Remaining $\overline{B}$, C_n	$\overline{F}_i$
t_{PLH} t_{PHL}	$\overline{B}_i$	$\overline{A}_i$	None	Remaining $\overline{A}$	Remaining $\overline{B}$, C_n	$\overline{F}_i$
t_{PLH} t_{PHL}	$\overline{A}_i$	None	$\overline{B}_i$	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{P}$
t_{PLH} t_{PHL}	$\overline{B}_i$	$\overline{A}_i$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{P}$
t_{PLH} t_{PHL}	$\overline{A}_i$	$\overline{B}_i$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{G}$
t_{PLH} t_{PHL}	$\overline{B}_i$	None	$\overline{A}_i$	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{G}$
t_{PLH} t_{PHL}	$\overline{A}_i$	None	$\overline{B}_i$	Remaining $\overline{A}$	Remaining $\overline{B}$, C_n	A = B
t_{PLH} t_{PHL}	$\overline{B}_i$	$\overline{A}_i$	None	Remaining $\overline{A}$	Remaining $\overline{B}$, C_n	A = B
t_{PLH} t_{PHL}	$\overline{A}_i$	$\overline{B}_i$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	C_{n+4}
t_{PLH} t_{PHL}	$\overline{B}_i$	None	$\overline{A}_i$	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	C_{n+4}
t_{PLH} t_{PHL}	C_n	None	None	All $\overline{A}$ and $\overline{B}$	None	Any $\overline{F}$ or C_{n+4}

LOGIC MODE TEST TABLE III **FUNCTION INPUTS:** $S_1 = S_2 = M = V_{CC}$, $S_0 = S_3 = GND$

PARAMETER	INPUT UNDER TEST	OTHER INPUT, SAME BIT		OTHER DATA INPUTS		OUTPUT UNDER TEST
		Apply V_{CC}	Apply GND	Apply V_{CC}	Apply GND	
t_{PLH} t_{PHL}	$\overline{A}_i$	$\overline{B}_i$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{F}_i$
t_{PLH} t_{PHL}	$\overline{B}_i$	$\overline{A}_i$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{F}_i$

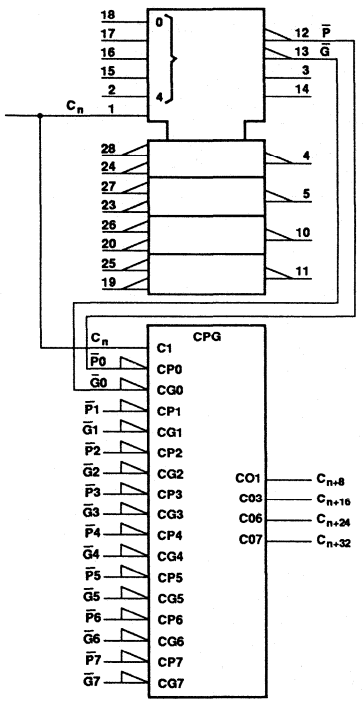


Figure 1

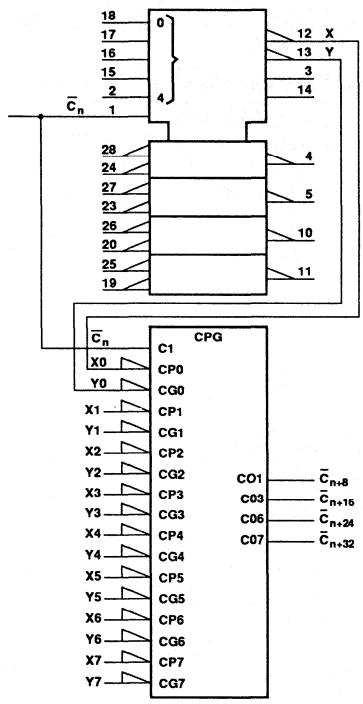


Figure 2

The signal designations in Figure 1 agree with the indicated internal functions based on active-Low data and are for use with the logic functions and arithmetic operations shown in the Function Table for Active-Low Data. The signal designators have been changed in Figure 2 to accommodate the logic functions and arithmetic operations given in the Function Table for Active-Low Data.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	74AC11181			74ACT11181			UNIT
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	DC supply voltage	3.0[1]	5.0	5.5	4.5	5.0	5.5	V
V_I	Input voltage	0		V_{CC}	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	0		V_{CC}	V
$\Delta t/\Delta v$	Input transition rise or fall rate	0		10	0		10	ns/V
T_A	Operating free-air temperature	-40		+85	-40		+85	°C

NOTE:
1. No electrical or switching characteristics are specified at $V_{CC} < 3V$. Operation between 2V and 3V is not recommended, but within that range, a device output will maintain a previously established logic state.

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	TEST CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 to+7.0	V
I_{IK} or V_I	DC input diode current[2]	$V_I < 0$	-20	mA
		$V_I > V_{CC}$	20	
	DC input voltage		-0.5 to V_{CC} +0.5	V
I_{OK} or V_O	DC output diode current[2]	$V_O < 0$	-50	mA
		$V_O > V_{CC}$	50	
	DC output voltage		-0.5 to V_{CC} +0.5	V
I_O	DC output source or sink current per output pin	V_O = 0 to V_{CC}	±50	mA
I_{CC} or I_{GND}	DC V_{CC} current		±100	mA
	DC ground current		±100	
T_{STG}	Storage temperature		-65 to 150	°C
P_{TOT}	Power dissipation per package Plastic DIP	Above 70°C:derate linearly by 8mW/K	500	mW
	Power dissipation per package Plastic surface mount (SO)	Above 70°C:derate linearly by 6mW/K	400	mW

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		V_{CC}	74AC11181				74ACT11181				UNIT
					T_A = +25°C		T_A = -40°C to +85°C		T_A = +25°C		T_A = -40°C to +85°C		
				V	Min	Max	Min	Max	Min	Max	Min	Max	
V_{IH}	High-level input voltage			3.0	2.10		2.10						V
				4.5	3.15		3.15		2.0		2.0		
				5.5	3.85		3.85		2.0		2.0		
V_{IL}	Low-level input voltage			3.0		0.90		0.90					V
				4.5		1.35		1.35		0.8		0.8	
				5.5		1.65		1.65		0.8		0.8	
V_{OH}	High-level output voltage	$V_I = V_{IL}$ or V_{IH}	I_{OH} = -50μA	3.0	2.9		2.9						V
				4.5	4.4		4.4		4.4		4.4		
				5.5	5.4		5.4		5.4		5.4		
			I_{OH} = -4mA	3.0	2.58		2.48						
			I_{OH} = -24mA	4.5	3.94		3.8		3.94		3.8		
				5.5	4.94		4.8		4.94		4.8		
			I_{OH} = -75mA[1]	5.5			3.85				3.85		
V_{OL}	Low-level output voltage	$V_I = V_{IL}$ or V_{IH}	I_{OL} = 50μA	3.0		0.1		0.1					V
				4.5		0.1		0.1		0.1		0.1	
				5.5		0.1		0.1		0.1		0.1	
			I_{OL} = 12mA	3.0		0.36		0.44					
			I_{OL} = 24mA	4.5		0.36		0.44		0.36		0.44	
				5.5		0.36		0.44		0.36		0.44	
			I_{OL} = 75mA[1]	5.5				1.65				1.65	
I_I	Input leakage current	$V_I = V_{CC}$ or GND		5.5		±0.1		±1.0		±0.1		±1.0	μA
I_{CC}	Quiescent supply current	$V_I = V_{CC}$ or GND, I_O = 0mA		5.5		8.0		80		8.0		80	μA
ΔI_{CC}	Supply current, TTL inputs High[2]	One input at 3.4V, other inputs at V_{CC} or GND		5.5						0.9		1.0	mA

NOTES:

1. Not more than one output should be tested at a time, and the duration of the test should not exceed 10ms.
2. This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0V or V_{CC}.

74AC/ACT11190

Asynchronous Presettable Synchronous Decade Up/Down Counter w/Single Clock

Preliminary Specification

FEATURES

- **Synchronous, reversible counting**
- **Positive edge-triggered clock**
- **BCD/decade**
- **Asynchronous Parallel Load capability**
- **Output capability: ±24mA**
- **CMOS (AC) and TTL (ACT) voltage level inputs**
- **50Ω incident wave switching**
- **Center-pin V_{CC} and ground configuration to minimize high-speed switching noise**
- **I_{CC} category: MSI**

DESCRIPTION

The 74AC/ACT11190 high-performance CMOS devices combine very high speed and high output drive comparable to the most advanced TTL families.

The 74AC/ACT11190 is an asynchronously presettable up/down BCD decade counter. It contains four master/slave flip-flops with internal gating and steering logic to provide asynchronous preset and synchronous count-up and count-down operation.

GENERAL INFORMATION

SYMBOL	PARAMETER	CONDITIONS T_A = 25°C; GND = 0V; V_{CC} = 5.0V	TYPICAL		UNIT
			AC	ACT	
t_{PLH}/ t_{PHL}	Propagation delay CP to Q_n ($\overline{PE}$ = High)	C_L = 50pF	5.7	7.1	ns
C_{PD}	Power dissipation capacitance[1]	f = 1MHz; C_L = 50pF	68	70	pF
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	4.0	4.0	pF
I_{LATCH}	Latch-up current	Per Jedec JC40.2 Standard 17	500	500	mA
f_{MAX}	Maximum clock frequency; CP → Q_n	C_L = 50pF	140	120	MHz

Note:

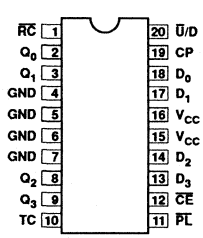
1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_I + \Sigma (C_L \times V_{CC}^2 \times f_O)$ where:
   f_I = input frequency in MHz, C_L = output load capacitance in pF,
   f_O = output frequency in MHz, V_{CC} = supply voltage in V,
   $\Sigma (C_L \times V_{CC}^2 \times f_O)$ = sum of outputs

ORDERING INFORMATION

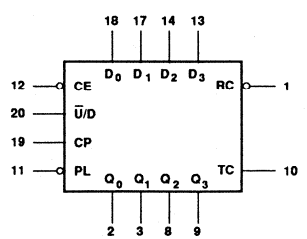
PACKAGES	TEMPERATURE RANGE	ORDER CODE
20-pin plastic DIP (300mil-wide)	-40°C to +85°C	74AC11190N 74ACT11190N
20-pin plastic SO (300mil-wide)	-40°C to +85°C	74AC11190D 74ACT11190D

PIN CONFIGURATION

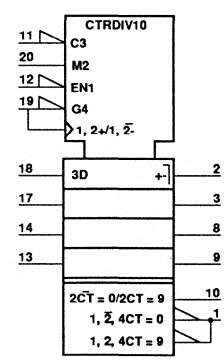
N and D Packages



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



Asynchronous Presettable Synchronous Decade Up/Down Counter w/Single Clock

74AC/ACT11190

Asynchronous Parallel Load capability permits the counter to be preset to any desired number. Information present on the parallel Data inputs (D_0 - D_3) is loaded into the counter and appears on the outputs when the Parallel Load ($\overline{PL}$) input is Low. As indicated in the Mode Select Table, this operation overrides the counting function.

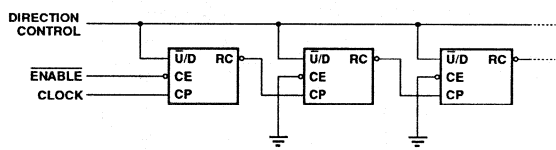
Counting is inhibited by a High level on the Count Enable ($\overline{CE}$) input.

Overflow/underflow indications are provided by two types of outputs, the Terminal Count (TC) and Ripple Clock ($\overline{RC}$). The TC output is normally Low and goes High when: 1) the count reaches zero in the count-down mode or 2) reaches "9" in the Count-up mode. The TC output will remain High until a state change occurs, either by counting or presetting, or until $\overline{U}$/D is changed. TC output should not be used as a clock signal because it is subject to decoding spikes. The TC signal is used internally to enable the $\overline{RC}$ output. When TC is High and $\overline{CE}$ is Low, the $\overline{RC}$ follows the Clock Pulse. The $\overline{RC}$ output essentially duplicates the Low clock pulse width, although delayed in time by two gate delays. The 74AC/ACT11190 simplifies the design of multistage counters, as indicated in Figures 1a and 1b.

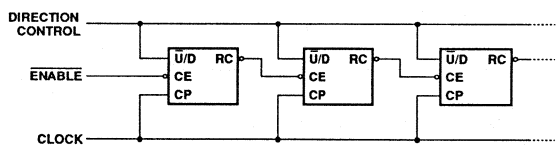
In Figure 1a, each $\overline{RC}$ output is used as the Clock input for the next higher stage. When the Clock input source has limited drive capability this configuration is particularly advantageous, since the clock source drives only the first stage. It is only necessary to inhibit the first stage to prevent counting in all stages, since a High signal on $\overline{CE}$ inhibits the $\overline{RC}$ output pulse as indicated in the Mode Select Table. The timing skew between state changes in the first and last stages is represented by the cumulative delay of the clock as it ripples through the preceding stages. This is a disadvantage of the configuration in some applications.

Figure 1b shows a method of causing state changes to occur simultaneously in all stages. The $\overline{RC}$ outputs propagate the carry/borrow signals in ripple fashion and all Clock inputs are driven in parallel. The Low state duration of the clock in this configuration must be long enough to allow the negative-going edge of the carry/borrow signal to ripple through to the last stage before the clock goes High. Since the $\overline{RC}$ output of any package goes High shortly after its CP input goes High, there is no such restriction on the High state duration of the clock.

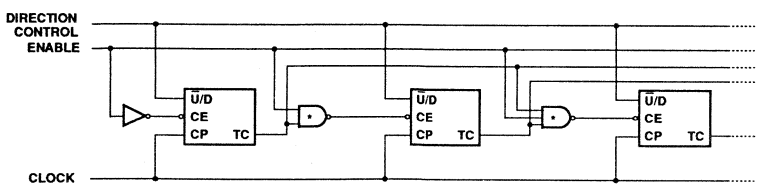
In Figure 1c, the configuration shown avoids ripple delays and their associated restrictions. Combining the TC signals from all the preceding stages forms the $\overline{CE}$ input signal for a given stage. An enable signal must be included in each carry gate in order to inhibit counting. The TC output of a given stage is not affected by its own $\overline{CE}$, therefore, the simple inhibit scheme of Figure 1a and 1b does not apply.



a. N-Stage Counter Using Ripple Clock



b. Synchronous N-Stage Counter with Common Clock Using Ripple Clock



c. Synchronous N-Stage Counter with Common Clock and Parallel Gated Terminal Count

Figure 1

Asynchronous Presettable Synchronous Decade Up/Down Counter w/Single Clock

PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
20	$\overline{U}$/D	Up/down count control input
12	$\overline{CE}$	Count enable input (active-Low)
18, 17, 14, 13	D_0 - D_3	Data inputs
19	CP	Clock pulse input (active rising edge)
11	$\overline{PL}$	Asynchronous load input (active-Low)
2, 3, 8, 9	Q_0 - Q_3	Counter outputs
1	$\overline{RC}$	Ripple clock output (active-Low)
10	TC	Terminal count output
4, 5, 6, 7	GND	Ground (0V)
15, 16	V_{CC}	Positive supply voltage

MODE SELECT — FUNCTION TABLE

OPERATING MODE	INPUTS					OUTPUTS
	$\overline{PL}$	$\overline{U}$/D	$\overline{CE}$	CP	D_n	Q_n
Parallel load	L	X	X	X	L	L
	L	X	X	X	H	H
Count up	H	L	l	↑	X	count up
Count down	H	H	l	↑	X	count down
Hold (do nothing)	H	X	H	X	X	no change

TC AND $\overline{RC}$ FUNCTION TABLE

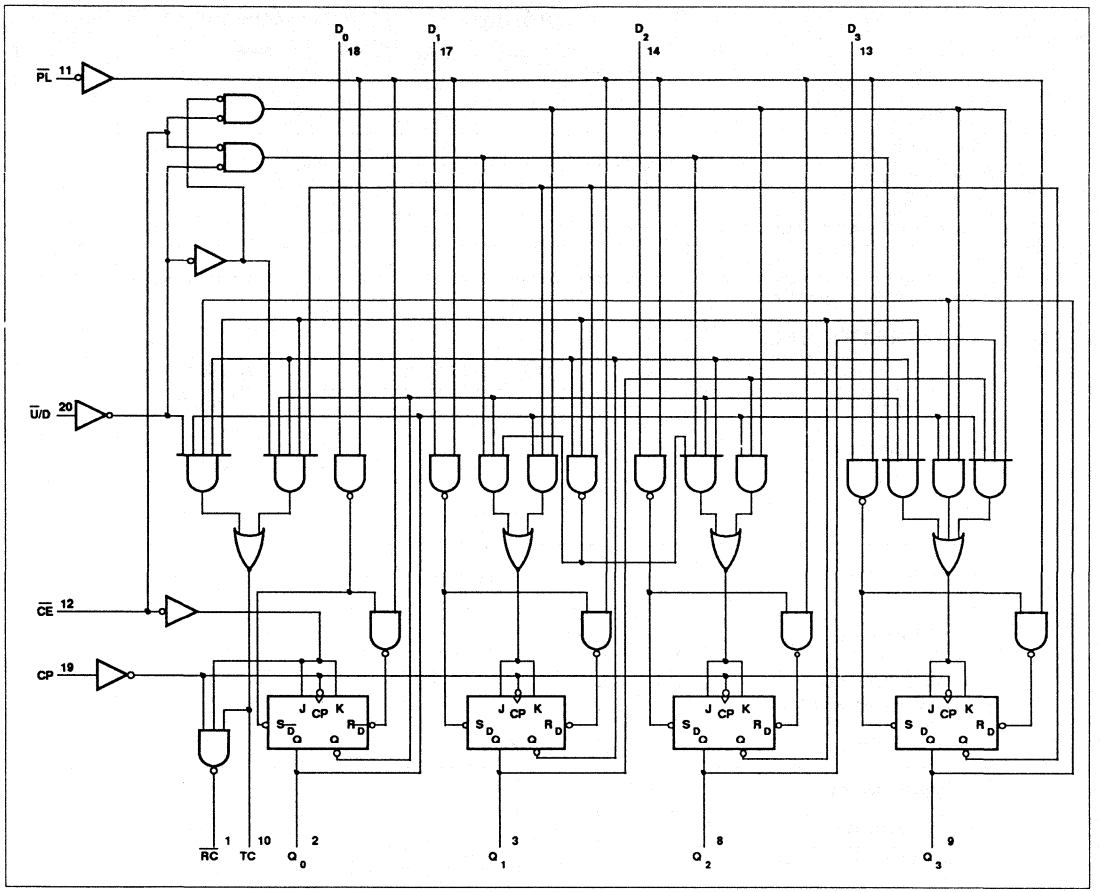
INPUTS			TERMINAL COUNT STATE				OUTPUTS	
$\overline{U}$/D	$\overline{CE}$	CP	Q_0	Q_1	Q_2	Q_3	TC	$\overline{RC}$
H	H	X	H	X	X	H	L	H
L	H	X	H	L	L	H	H	H
L	L	⊓	H	L	L	H	H	⊓
L	H	X	L	L	L	L	L	H
H	H	X	L	L	L	L	H	H
H	L	⊓	L	L	L	L	H	⊓

H = High voltage level
L = Low voltage level
h = High voltage level one setup time prior to the Low-to High clock transition
l = Low voltage level one setup time prior to the Low-to High clock transition
X = Don't care
↑ = Low-to-High clock transition
⊓ = Low pulse

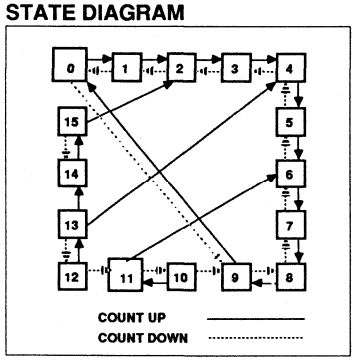
Asynchronous Presettable Synchronous Decade Up/Down Counter w/Single Clock

74AC/ACT11190

LOGIC DIAGRAM



STATE DIAGRAM



RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	74AC11190			74ACT11190			UNIT
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	DC supply voltage	3.0[1]	5.0	5.5	4.5	5.0	5.5	V
V_I	Input voltage	0		V_{CC}	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	0		V_{CC}	V
$\Delta t/\Delta v$	Input transition rise or fall rate	0		10	0		10	ns/V
T_A	Operating free-air temperature	-40		+85	-40		+85	°C

NOTE:

1. No electrical or switching characteristics are specified at V_{CC} < 3V. Operation between 2V and 3V is not recommended, but within that range, a device output will maintain a previously established logic state.

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	TEST CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 to+7.0	V
I_{IK} or V_I	DC input diode current[2]	$V_I < 0$	-20	mA
		$V_I > V_{CC}$	20	
	DC input voltage		-0.5 to V_{CC} +0.5	V
I_{OK} or V_O	DC output diode current[2]	$V_O < 0$	-50	mA
		$V_O > V_{CC}$	50	
	DC output voltage		-0.5 to V_{CC} +0.5	V
I_O	DC output source or sink current per output pin	V_O = 0 to V_{CC}	±50	mA
I_{CC} or I_{GND}	DC V_{CC} current		±150	mA
	DC ground current		±150	
T_{STG}	Storage temperature		-65 to 150	°C
P_{TOT}	Power dissipation per package Plastic DIP	Above 70°C:derate linearly by 8mW/K	500	mW
	Power dissipation per package Plastic surface mount (SO)	Above 70°C:derate linearly by 6mW/K	400	mW

NOTES:

1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		V_{CC}	74AC11190				74ACT11190				UNIT
					T_A = +25°C		T_A = -40°C to +85°C		T_A = +25°C		T_A = -40°C to +85°C		
				V	Min	Max	Min	Max	Min	Max	Min	Max	
V_{IH}	High-level input voltage			3.0	2.10		2.10						V
				4.5	3.15		3.15		2.0		2.0		
				5.5	3.85		3.85		2.0		2.0		
V_{IL}	Low-level input voltage			3.0		0.90		0.90					V
				4.5		1.35		1.35		0.8		0.8	
				5.5		1.65		1.65		0.8		0.8	
V_{OH}	High-level output voltage	V_I = V_{IL} or V_{IH}	I_{OH} = -50μA	3.0	2.9		2.9						V
				4.5	4.4		4.4		4.4		4.4		
				5.5	5.4		5.4		5.4		5.4		
			I_{OH} = -4mA	3.0	2.58		2.48						
			I_{OH} = -24mA	4.5	3.94		3.8		3.94		3.8		
				5.5	4.94		4.8		4.94		4.8		
			I_{OH} = -75mA[1]	5.5			3.85				3.85		
V_{OL}	Low-level output voltage	V_I = V_{IL} or V_{IH}	I_{OL} = 50μA	3.0		0.1		0.1					V
				4.5		0.1		0.1		0.1		0.1	
				5.5		0.1		0.1		0.1		0.1	
			I_{OL} = 12mA	3.0		0.36		0.44					
			I_{OL} = 24mA	4.5		0.36		0.44		0.36		0.44	
				5.5		0.36		0.44		0.36		0.44	
			I_{OL} = 75mA[1]	5.5				1.65				1.65	
I_I	Input leakage current	V_I = V_{CC} or GND		5.5		±0.1		±1.0		±0.1		±1.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC} or GND, I_O = 0		5.5		8.0		80		8.0		80	μA
ΔI_{CC}	Supply current, TTL inputs High[2]	One input at 3.4V, other inputs at V_{CC} or GND		5.5						0.9		1.0	mA

NOTES:
1. Not more than one output should be tested at a time, and the duration of the test should not exceed 10ms.
2. This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0V or V_{CC}.

AC ELECTRICAL CHARACTERISTICS AT 3.3V ±0.3V

SYMBOL	PARAMETER		WAVEFORM	74AC11190					UNIT
				T_A = +25°C			T_A = -40°C to +85°C		
				Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	CP to Q_n	1	70	90		70		MHz
		CP to $\overline{RC}$, TC		70	90		70		MHz
t_{PLH} t_{PHL}	Propagation delay CP to Q_n		1	1.5 1.5	7.6 7.6	9.4 9.3	1.5 1.5	10.4 10.3	ns
t_{PLH} t_{PHL}	Propagation delay CP to TC		1	1.5 1.5	10.2 8.3	12.2 10.2	1.5 1.5	13.7 11.6	ns
t_{PLH} t_{PHL}	Propagation delay CP to $\overline{RC}$		2	1.5 1.5	8.7 6.1	10.5 7.8	1.5 1.5	11.7 8.8	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{CE}$ to $\overline{RC}$		2	1.5 1.5	7.4 4.7	9.1 6.2	1.5 1.5	10.0 7.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{U}$/D to $\overline{RC}$		2	1.5 1.5	11.7 8.5	13.8 11.0	1.5 1.5	15.3 12.5	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{U}$/D to TC		4	1.5 1.5	8.9 6.5	11.5 8.6	1.5 1.5	12.7 9.7	ns
t_{PLH} t_{PHL}	Propagation delay D_n to Q_n		3	1.5 1.5	9.8 8.8	11.8 10.7	1.5 1.5	13.1 11.9	ns
t_{PLH} t_{PHL}	Propagation delay D_n to TC		3, 4	1.5 1.5	13.9 9.8	17.2 13.4	1.5 1.5	19.3 15.1	ns
t_{PLH} t_{PHL}	Propagation delay D_n to $\overline{RC}$		3, 4	1.5 1.5	14.9 13.6	18.9 17.0	1.5 1.5	21.1 19.1	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{PL}$ to Q_n		5	1.5 1.5	10.8 9.3	12.9 11.2	1.5 1.5	14.2 12.4	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{PL}$ to TC		5	1.5 1.5	14.2 10.6	16.8 14.1	1.5 1.5	18.6 15.7	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{PL}$ to $\overline{RC}$		5	1.5 1.5	15.6 14.1	19.3 17.2	1.5 1.5	21.4 19.0	ns
$t_S(H)$ $t_S(L)$	Setup time, High or Low D_n to $\overline{PL}$		6	3.5			3.5		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low D_n to $\overline{PL}$		6	0.5			0.5		ns
$t_S(H)$ $t_S(L)$	Setup time, High or Low $\overline{CE}$ to CP		6	11.5			11.5		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low $\overline{CE}$ to CP		6	0.0			0.0		ns
$t_S(H)$ $t_S(L)$	Setup time, High or Low $\overline{U}$/D to CP		6	12.5			12.5		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low $\overline{U}$/D to CP		6	0.0			0.0		ns
$t_w(L)$	$\overline{PL}$ pulse width, Low		5	4.0			4.0		ns
$t_w(H)$ $t_w(L)$	CP pulse width, High or Low		1	7.1			7.1		ns
t_{REC}	Recover time, $\overline{PL}$ to CP		5	2.0			2.0		ns

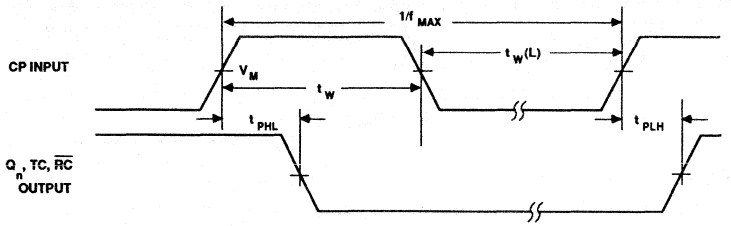
AC ELECTRICAL CHARACTERISTICS AT 5.0V ±0.5V

SYMBOL	PARAMETER		WAVEFORM	74AC11190					UNIT
				T_A = +25°C			T_A = -40°C to +85°C		
				Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	CP to Q_n	1	110	140		110		MHz
		CP to $\overline{RC}$, TC		80	110		80		MHz
t_{PLH} t_{PHL}	Propagation delay CP to Q_n		1	1.5 1.5	5.5 5.8	7.1 7.3	1.5 1.5	7.8 8.0	ns
t_{PLH} t_{PHL}	Propagation delay CP to TC		1	1.5 1.5	6.9 6.0	8.6 7.6	1.5 1.5	9.5 8.6	ns
t_{PLH} t_{PHL}	Propagation delay CP to $\overline{RC}$		2	1.5 1.5	6.1 4.4	7.6 5.8	1.5 1.5	8.2 6.5	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{CE}$ to $\overline{RC}$		2	1.5 1.5	5.0 3.4	6.4 4.8	1.5 1.5	7.0 5.4	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{U}$/D to $\overline{RC}$		2	1.5 1.5	7.5 5.8	9.4 7.7	1.5 1.5	10.4 8.9	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{U}$/D to TC		4	1.5 1.5	5.8 4.7	7.8 6.2	1.5 1.5	8.8 7.0	ns
t_{PLH} t_{PHL}	Propagation delay D_n to Q_n		3	1.5 1.5	6.6 6.5	8.3 8.0	1.5 1.5	9.1 8.8	ns
t_{PLH} t_{PHL}	Propagation delay D_n to TC		3, 4	1.5 1.5	9.0 6.7	11.3 9.4	1.5 1.5	12.7 10.5	ns
t_{PLH} t_{PHL}	Propagation delay D_n to $\overline{RC}$		3, 4	1.5 1.5	9.5 9.0	12.3 11.3	1.5 1.5	13.8 13.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{PL}$ to Q_n		5	1.5 1.5	7.2 6.8	8.9 8.4	1.5 1.5	9.9 9.2	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{PL}$ to TC		5	1.5 1.5	9.3 7.3	11.2 9.8	1.5 1.5	12.6 11.1	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{PL}$ to $\overline{RC}$		5	1.5 1.5	9.9 9.3	12.5 11.5	1.5 1.5	14.0 12.8	ns
$t_S(H)$ $t_S(L)$	Setup time, High or Low D_n to $\overline{PL}$		6	2.5			2.5		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low D_n to $\overline{PL}$		6	1.0			1.0		ns
$t_S(H)$ $t_S(L)$	Setup time, High or Low $\overline{CE}$ to CP		6	7.0			7.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low $\overline{CE}$ to CP		6	0.5			0.5		ns
$t_S(H)$ $t_S(L)$	Setup time, High or Low $\overline{U}$/D to CP		6	8.0			8.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low $\overline{U}$/D to CP		6	0.0			0.0		ns
$t_w(L)$	$\overline{PL}$ pulse width, Low		5	3.0			3.0		ns
$t_w(H)$ $t_w(L)$	CP pulse width, High or Low		1	6.3			6.3		ns
t_{REC}	Recover time, $\overline{PL}$ to CP		5	1.5			1.5		ns

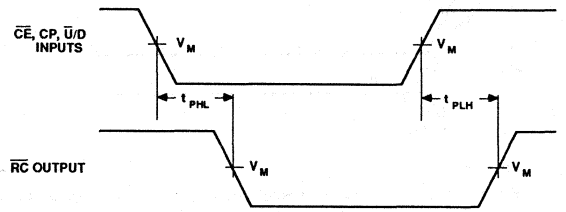
AC ELECTRICAL CHARACTERISTICS AT 5.0V ±0.5V

SYMBOL	PARAMETER		WAVEFORM	74ACT11190					UNIT
				T_A = +25°C			T_A = -40°C to +85°C		
				Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	CP to Q_n	1	90	120		90		MHz
		CP to $\overline{RC}$, TC		90	120		90		MHz
t_{PLH} t_{PHL}	Propagation delay CP to Q_n		1	1.5 1.5	6.9 7.2	8.5 8.7	1.5 1.5	9.3 9.6	ns
t_{PLH} t_{PHL}	Propagation delay CP to TC		1	1.5 1.5	8.1 7.5	9.9 9.1	1.5 1.5	10.9 10.2	ns
t_{PLH} t_{PHL}	Propagation delay CP to $\overline{RC}$		2	1.5 1.5	7.9 7.3	9.5 8.9	1.5 1.5	10.4 9.7	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{CE}$ to $\overline{RC}$		2	1.5 1.5	6.6 4.8	8.0 6.2	1.5 1.5	8.8 6.9	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{U}$/D to $\overline{RC}$		2	1.5 1.5	9.0 7.2	10.9 9.3	1.5 1.5	11.9 10.4	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{U}$/D to TC		4	1.5 1.5	7.6 7.8	9.8 9.6	1.5 1.5	10.9 10.5	ns
t_{PLH} t_{PHL}	Propagation delay D_n to Q_n		3	1.5 1.5	8.2 7.8	9.9 9.5	1.5 1.5	10.9 10.4	ns
t_{PLH} t_{PHL}	Propagation delay D_n to TC		3, 4	1.5 1.5	10.3 8.2	12.6 10.8	1.5 1.5	14.1 12.1	ns
t_{PLH} t_{PHL}	Propagation delay D_n to $\overline{RC}$		3, 4	1.5 1.5	11.0 10.3	14.0 12.9	1.5 1.5	15.3 14.4	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{PL}$ to Q_n		5	1.5 1.5	8.6 8.1	10.3 9.7	1.5 1.5	11.3 10.6	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{PL}$ to TC		5	1.5 1.5	10.9 10.3	12.9 12.8	1.5 1.5	14.2 14.1	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{PL}$ to $\overline{RC}$		5	1.5 1.5	12.0 12.1	14.9 14.2	1.5 1.5	16.4 15.8	ns
$t_S(H)$ $t_S(L)$	Setup time, High or Low D_n to $\overline{PL}$		6	2.0			2.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low D_n to $\overline{PL}$		6	2.0			2.0		ns
$t_S(H)$ $t_S(L)$	Setup time, High or Low $\overline{CE}$ to CP		6	7.0			7.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low $\overline{CE}$ to CP		6	1.5			1.5		ns
$t_S(H)$ $t_S(L)$	Setup time, High or Low $\overline{U}$/D to CP		6	7.5			7.5		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low $\overline{U}$/D to CP		6	0.0			0.0		ns
$t_w(L)$	$\overline{PL}$ pulse width, Low		5	3.5			3.5		ns
$t_w(H)$ $t_w(L)$	CP pulse width, High or Low		1	5.6			5.6		ns
t_{REC}	Recover time, $\overline{PL}$ to CP		5	2.0			2.0		ns

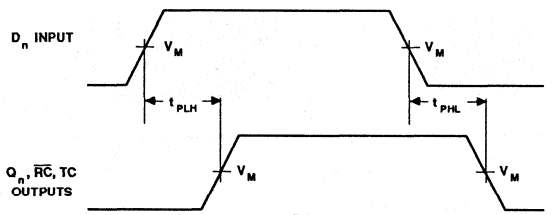
AC WAVEFORMS



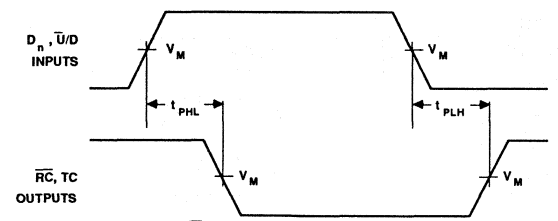
Waveform 1. Waveforms Showing Clock to Outputs Propagation Delays and Clock Pulse Width



Waveform 2. Waveforms Showing the Clock, Count Enable, or U/D to Ripple Clock Output Propagation Delay

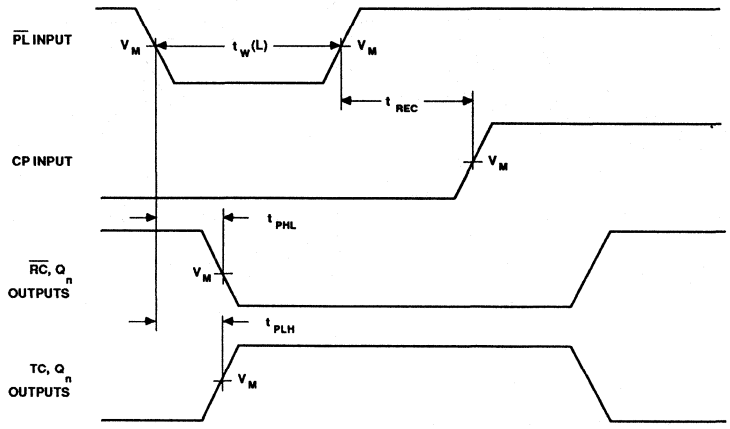


Waveform 3. Waveforms Showing the Input (D_n) to Output (Q_n, $\overline{RC}$, TC) Propagation Delays, Non-Inverting Path

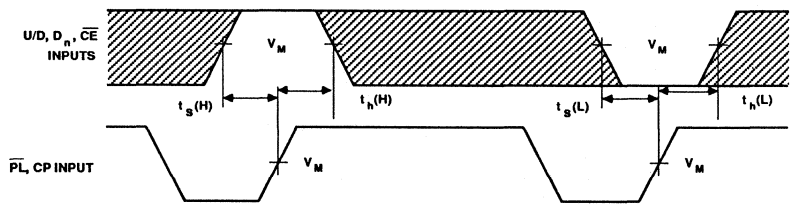


Waveform 4. Waveforms Showing the Input (D_n, $\overline{U}$/D) to Output ($\overline{RC}$, TC) Propagation Delays, Inverting Path

AC WAVEFORMS



Waveform 5. Waveforms Showing the Parallel Load Pulse Width, Parallel Load to Output Delay and Parallel Load to Clock Recovery Time

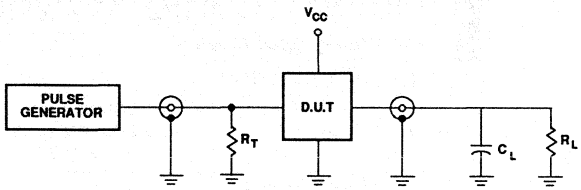


Waveform 6. Waveforms Showing Setup Time and Hold Time for D_n to $\overline{PL}$, $\overline{U}/D$ to CP and $\overline{CE}$ to CP

WAVEFORM CONDITIONS

	INPUTS	OUTPUTS
AC	V_{IN} = GND to V_{CC}, V_M = 50% V_{CC}	V_{OUT} = V_{OL} to V_{OH}
ACT	V_{IN} = GND to 3.0V, V_M = 1.5V	V_M = 50% V_{CC}

TEST CIRCUIT



Test Circuit

DEFINITIONS

C_L = Load capacitance, 50pF; includes jig and probe capacitance

R_L = Load resistor, 500Ω

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators

Input pulses: PRR ≤ 10MHz

$t_r = t_f = 3ns$

74AC/ACT11191

Asynchronous Presettable Synchronous 4-Bit Binary Up/ Down Counter w/Single Clock

Preliminary Specification

FEATURES

- **Synchronous, reversible counting**
- **Positive edge-triggered clock**
- **4-bit binary**
- **Asynchronous Parallel Load capability**
- **Output capability: ±24mA**
- **CMOS (AC) and TTL (ACT) voltage level inputs**
- **50Ω incident wave switching**
- **Center-pin V_{CC} and ground configuration to minimize high-speed switching noise**
- **I_{CC} category: MSI**

DESCRIPTION

The 74AC/ACT11191 high-performance CMOS devices combine very high speed and high output drive comparable to the most advanced TTL families.

The 74AC/ACT11191 is an asynchronously presettable up/down 4-bit binary counter. It contains four master/slave flip-flops with internal gating and steering logic to provide asynchronous preset and synchronous count-up and count-down operation.

GENERAL INFORMATION

SYMBOL	PARAMETER	CONDITIONS T_A = 25°C; GND = 0V; V_{CC} = 5.0V	TYPICAL AC	TYPICAL ACT	UNIT
t_{PLH}/ t_{PHL}	Propagation delay CP to Q_n ($\overline{PE}$ = High)	C_L = 50pF	5.8	7.5	ns
C_{PD}	Power dissipation capacitance[1]	f = 1MHz; C_L = 50pF	66	68	pF
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	4.0	4.0	pF
I_{LATCH}	Latch-up current	Per Jedec JC40.2 Standard 17	500	500	mA
f_{MAX}	Maximum clock frequency, CP → Q_n	C_L = 50pF	140	120	MHz

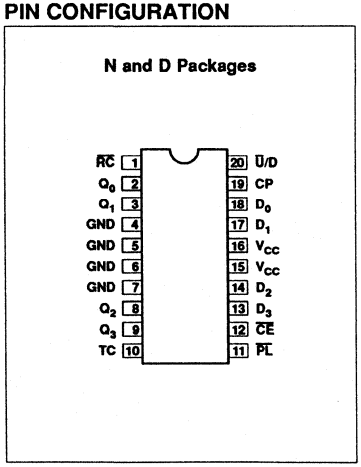
Note:

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_I + \Sigma (C_L \times V_{CC}^2 \times f_O)$ where:
   f_I = input frequency in MHz, C_L = output load capacitance in pF,
   f_O = output frequency in MHz, V_{CC} = supply voltage in V,
   $\Sigma (C_L \times V_{CC}^2 \times f_O)$ = sum of outputs

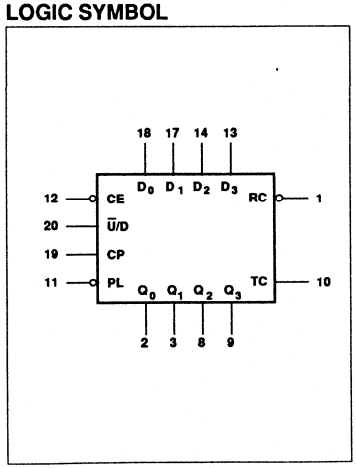
ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE
20-pin plastic DIP (300mil-wide)	-40°C to +85°C	74AC11191N 74ACT11191N
20-pin plastic SO (300mil-wide)	-40°C to +85°C	74AC11191D 74ACT11191D

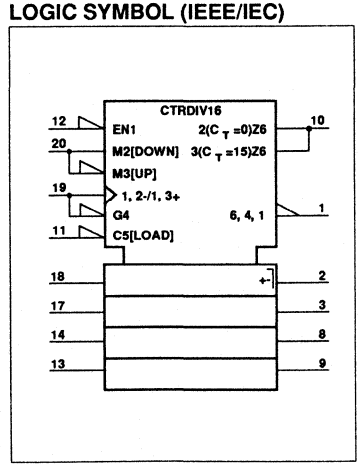
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



Asynchronous Parallel Load capability permits the counter to be preset to any desired number. Information present on the parallel Data inputs (D_0 - D_3) is loaded into the counter and appears on the outputs when the Parallel Load ($\overline{PL}$) input is Low. As indicated in the Mode Select Table, this operation overrides the counting function.

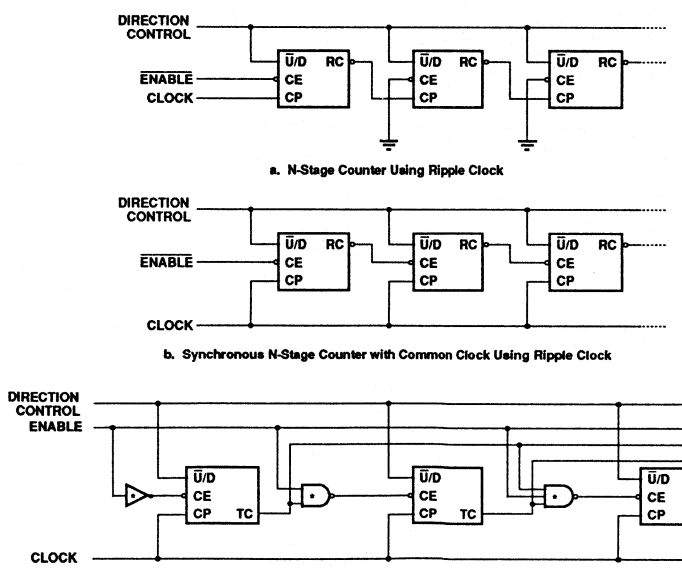
Counting is inhibited by a High level on the Count Enable ($\overline{CE}$) input.

Overflow/underflow indications are provided by two types of outputs, the Terminal Count (TC) and Ripple Clock ($\overline{RC}$). The TC output is normally Low and goes High when: 1) the count reaches zero in the count-down mode or 2) reaches "15" in the Count-up mode. The TC output will remain High until a state change occurs, either by counting or presetting, or until $\overline{U}$/D is changed. TC output should not be used as a clock signal because it is subject to decoding spikes. The TC signal is used internally to enable the $\overline{RC}$ output. When TC is High and $\overline{CE}$ is Low, the $\overline{RC}$ follows the Clock Pulse. The $\overline{RC}$ output essentially duplicates the Low clock pulse width, although delayed in time by two gate delays. The 74AC/ACT11191 simplifies the design of multistage counters, as indicated in Figures 1a and 1b.

In Figure 1a, each $\overline{RC}$ output is used as the Clock input for the next higher stage. When the Clock input source has limited drive capability this configuration is particularly advantageous, since the clock source drives only the first stage. It is only necessary to inhibit the first stage to prevent counting in all stages, since a High signal on $\overline{CE}$ inhibits the $\overline{RC}$ output pulse as indicated in the Mode Select Table. The timing skew between state changes in the first and last stages is represented by the cumulative delay of the clock as it ripples through the preceding stages. This is a disadvantage of the configuration in some applications.

Figure 1b shows a method of causing state changes to occur simultaneously in all stages. The $\overline{RC}$ outputs propagate the carry/borrow signals in ripple fashion and all Clock inputs are driven in parallel. The Low state duration of the clock in this configuration must be long enough to allow the negative-going edge of the carry/borrow signal to ripple through to the last stage before the clock goes High. Since the $\overline{RC}$ output of any package goes High shortly after its CP input goes High, there is no such restriction on the High state duration of the clock.

In Figure 1c, the configuration shown avoids ripple delays and their associated restrictions. Combining the TC signals from all the preceding stages forms the $\overline{CE}$ input signal for a given stage. An enable signal must be included in each carry gate in order to inhibit counting. The TC output of a given stage is not affected by its own $\overline{CE}$, therefore, the simple inhibit scheme of Figure 1a and 1b does not apply.



a. N-Stage Counter Using Ripple Clock

b. Synchronous N-Stage Counter with Common Clock Using Ripple Clock

c. Synchronous N-Stage Counter with Common Clock and Parallel Gated Terminal Count

* Additional devices

Figure 1

PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
20	$\overline{U}/D$	Up/down count control input
12	$\overline{CE}$	Count enable input (active-Low)
18, 17, 14, 13	$D_0 - D_3$	Data inputs
19	CP	Clock pulse input (active rising edge)
11	$\overline{PL}$	Asynchronous load input (active-Low)
2, 3, 8, 9	$Q_0 - Q_3$	Counter outputs
1	$\overline{RC}$	Ripple clock output (active-Low)
10	TC	Terminal count output
4, 5, 6, 7	GND	Ground (0V)
15, 16	V_{CC}	Positive supply voltage

MODE SELECT — FUNCTION TABLE

OPERATING MODE	INPUTS					OUTPUTS
	$\overline{PL}$	$\overline{U}/D$	$\overline{CE}$	CP	D_n	Q_n
Parallel load	L	X	X	X	L	L
	L	X	X	X	H	H
Count up	H	L	l	↑	X	count up
Count down	H	H	l	↑	X	count down
Hold (do nothing)	H	X	H	X	X	no change

TC AND $\overline{RC}$ FUNCTION TABLE

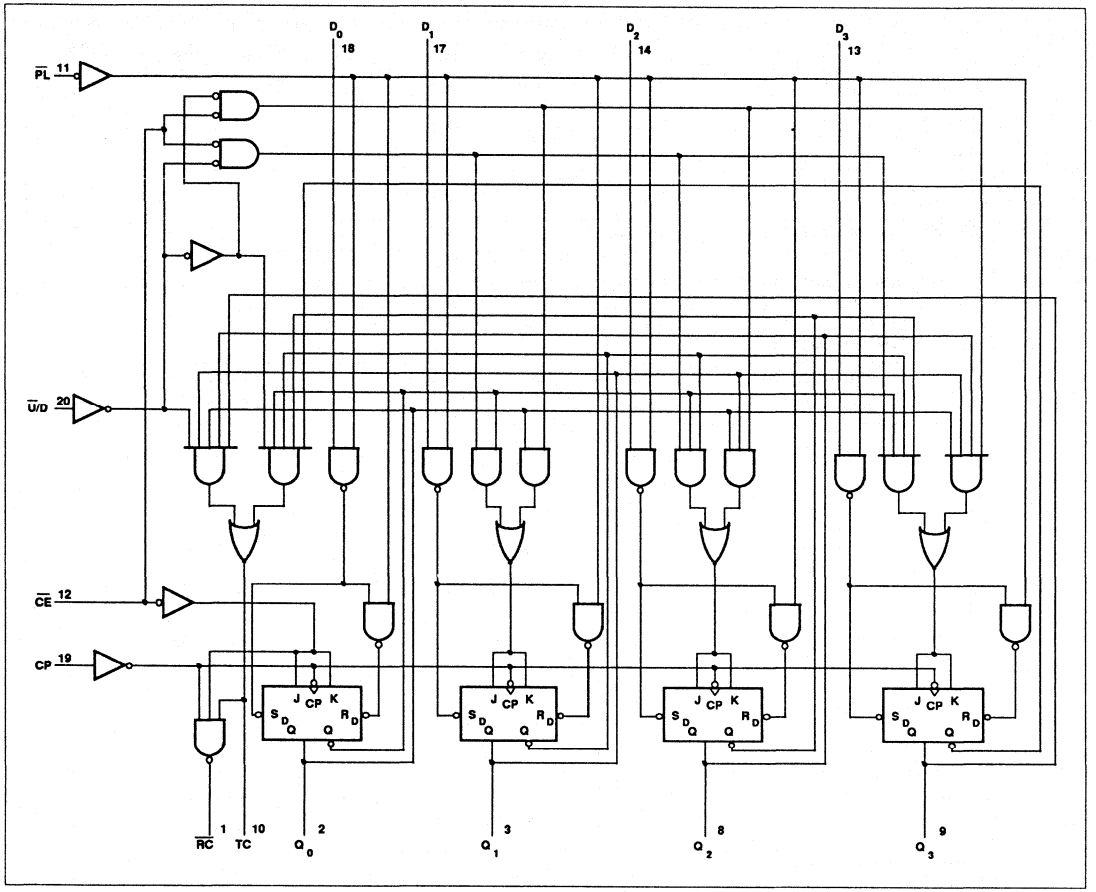
INPUTS			TERMINAL COUNT STATE				OUTPUTS	
$\overline{U}/D$	$\overline{CE}$	CP	Q_0	Q_1	Q_2	Q_3	TC	$\overline{RC}$
H	H	X	H	H	H	H	L	H
L	H	X	H	H	H	H	H	H
L	L	⊓	H	H	H	H	H	⊓
L	H	X	L	L	L	L	L	H
H	H	X	L	L	L	L	H	H
H	L	⊓	L	L	L	L	H	⊓

H = High voltage level
L = Low voltage level
h = High voltage level one setup time prior to the Low-to High clock transition
l = Low voltage level one setup time prior to the Low-to High clock transition
X = Don't care
↑ = Low-to-High clock transition
↓ = High-to-Low Trickle Clock transition
⊓ = Low pulse

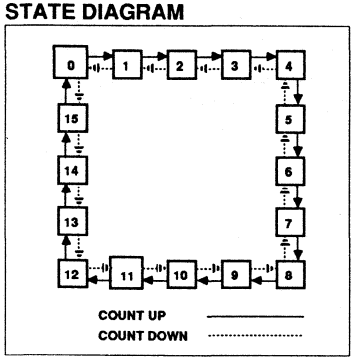
Asynchronous Presettable Synchronous 4-Bit Binary Up/Down Counter w/Single Clock

74AC/ACT11191

LOGIC DIAGRAM



STATE DIAGRAM



RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	74AC11191			74ACT11191			UNIT
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	DC supply voltage	3.0[1]	5.0	5.5	4.5	5.0	5.5	V
V_I	Input voltage	0		V_{CC}	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	0		V_{CC}	V
$\Delta t/\Delta v$	Input transition rise or fall rate	0		10	0		10	ns/V
T_A	Operating free-air temperature	-40		+85	-40		+85	°C

NOTE:

1. No electrical or switching characteristics are specified at $V_{CC} < 3V$. Operation between 2V and 3V is not recommended, but within that range, a device output will maintain a previously established logic state.

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	TEST CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 to+7.0	V
I_{IK} or V_I	DC input diode current[2]	$V_I < 0$	-20	mA
		$V_I > V_{CC}$	20	
	DC input voltage		-0.5 to V_{CC} +0.5	V
I_{OK} or V_O	DC output diode current[2]	$V_O < 0$	-50	mA
		$V_O > V_{CC}$	50	
	DC output voltage		-0.5 to V_{CC} +0.5	V
I_O	DC output source or sink current per output pin	V_O = 0 to V_{CC}	±50	mA
I_{CC} or I_{GND}	DC V_{CC} current		±150	mA
	DC ground current		±150	
T_{STG}	Storage temperature		-65 to 150	°C
P_{TOT}	Power dissipation per package Plastic DIP	Above 70°C:derate linearly by 8mW/K	500	mW
	Power dissipation per package Plastic surface mount (SO)	Above 70°C:derate linearly by 6mW/K	400	mW

NOTES:

1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		V_{CC}	74AC11191				74ACT11191				UNIT
					T_A = +25°C		T_A = -40°C to +85°C		T_A = +25°C		T_A = -40°C to +85°C		
				V	Min	Max	Min	Max	Min	Max	Min	Max	
V_{IH}	High-level input voltage			3.0	2.10		2.10						V
				4.5	3.15		3.15		2.0		2.0		
				5.5	3.85		3.85		2.0		2.0		
V_{IL}	Low-level input voltage			3.0		0.90		0.90					V
				4.5		1.35		1.35		0.8		0.8	
				5.5		1.65		1.65		0.8		0.8	
V_{OH}	High-level output voltage	V_I = V_{IL} or V_{IH}	I_{OH} = -50μA	3.0	2.9		2.9						V
				4.5	4.4		4.4		4.4		4.4		
				5.5	5.4		5.4		5.4		5.4		
			I_{OH} = -4mA	3.0	2.58		2.48						
			I_{OH} = -24mA	4.5	3.94		3.8		3.94		3.8		
				5.5	4.94		4.8		4.94		4.8		
			I_{OH} = -75mA[1]	5.5			3.85				3.85		
V_{OL}	Low-level output voltage	V_I = V_{IL} or V_{IH}	I_{OL} = 50μA	3.0		0.1		0.1					V
				4.5		0.1		0.1		0.1		0.1	
				5.5		0.1		0.1		0.1		0.1	
			I_{OL} = 12mA	3.0		0.36		0.44					
			I_{OL} = 24mA	4.5		0.36		0.44		0.36		0.44	
				5.5		0.36		0.44		0.36		0.44	
			I_{OL} = 75mA[1]	5.5				1.65				1.65	
I_I	Input leakage current	V_I = V_{CC} or GND		5.5		±0.1		±1.0		±0.1		±1.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC} or GND, I_O = 0		5.5		8.0		80		8.0		80	μA
ΔI_{CC}	Supply current, TTL inputs High[2]	One input at 3.4V, other inputs at V_{CC} or GND		5.5						0.9		1.0	mA

NOTES:
1. Not more than one output should be tested at a time, and the duration of the test should not exceed 10ms.
2. This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0V or V_{CC}.

AC ELECTRICAL CHARACTERISTICS AT 3.3V ±0.3V

SYMBOL	PARAMETER		WAVEFORM	74AC11191					UNIT
				T_A = +25°C			T_A = -40°C to +85°C		
				Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	CP to Q_n	1	70	90		70		MHz
		CP to $\overline{RC}$, TC		60	80		60		MHz
t_{PLH} t_{PHL}	Propagation delay CP to Q_n		1	1.5 1.5	7.8 7.7	9.7 9.4	1.5 1.5	10.7 10.3	ns
t_{PLH} t_{PHL}	Propagation delay CP to TC		1	1.5 1.5	10.2 10.5	11.9 12.3	1.5 1.5	13.2 13.5	ns
t_{PLH} t_{PHL}	Propagation delay CP to $\overline{RC}$		2	1.5 1.5	9.0 8.0	10.8 9.5	1.5 1.5	11.8 10.4	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{CE}$ to $\overline{RC}$		2	1.5 1.5	7.5 6.8	9.0 8.1	1.5 1.5	9.9 8.9	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{U}$/D to $\overline{RC}$		2	1.5 1.5	11.5 10.6	14.0 12.9	1.5 1.5	15.3 14.2	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{U}$/D to TC		4	1.5 1.5	9.1 8.6	11.2 10.6	1.5 1.5	12.3 11.8	ns
t_{PLH} t_{PHL}	Propagation delay D_n to Q_n		3	1.5 1.5	10.1 9.1	11.8 10.7	1.5 1.5	13.0 11.8	ns
t_{PLH} t_{PHL}	Propagation delay D_n to TC		3, 4	1.5 1.5	14.0 12.2	16.8 15.5	1.5 1.5	18.9 17.1	ns
t_{PLH} t_{PHL}	Propagation delay D_n to $\overline{RC}$		3, 4	1.5 1.5	15.2 15.6	18.6 18.7	1.5 1.5	20.6 20.7	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{PL}$ to Q_n		5	1.5 1.5	11.1 9.6	12.8 11.2	1.5 1.5	14.0 12.3	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{PL}$ to TC		5	1.5 1.5	14.7 13.0	17.3 15.8	1.5 1.5	19.4 17.5	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{PL}$ to $\overline{RC}$		5	1.5 1.5	16.0 16.3	19.1 19.2	1.5 1.5	21.2 21.3	ns
$t_S(H)$ $t_S(L)$	Setup time, High or Low D_n to $\overline{PL}$		6	3.5			3.5		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low D_n to $\overline{PL}$		6	0.5			0.5		ns
$t_S(H)$ $t_S(L)$	Setup time, High or Low $\overline{CE}$ to CP		6	10.0			10.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low $\overline{CE}$ to CP		6	0.0			0.0		ns
$t_S(H)$ $t_S(L)$	Setup time, High or Low $\overline{U}$/D to CP		6	11.0			11.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low $\overline{U}$/D to CP		6	0.0			0.0		ns
$t_w(L)$	$\overline{PL}$ pulse width, Low		5	4.0			4.0		ns
$t_w(H)$ $t_w(L)$	CP pulse width, High or Low		1	8.3			8.3		ns
t_{REC}	Recover time, $\overline{PL}$ to CP		5	2.5			2.5		ns

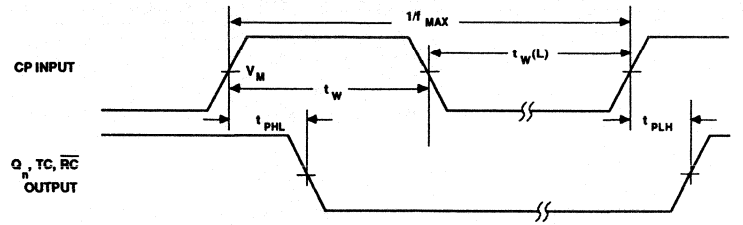
AC ELECTRICAL CHARACTERISTICS AT 5.0V ±0.5V

SYMBOL	PARAMETER		WAVEFORM	74AC11191					UNIT
				T_A = +25°C			T_A = -40°C to +85°C		
				Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	CP to Q_n	1	110	140		110		MHz
		CP to $\overline{RC}$, TC		80	100		80		MHz
t_{PLH} t_{PHL}	Propagation delay CP to Q_n		1	1.5 1.5	5.7 5.9	7.5 7.5	1.5 1.5	8.1 8.2	ns
t_{PLH} t_{PHL}	Propagation delay CP to TC		1	1.5 1.5	7.2 7.8	8.8 9.3	1.5 1.5	9.7 10.3	ns
t_{PLH} t_{PHL}	Propagation delay CP to $\overline{RC}$		2	1.5 1.5	6.5 6.1	8.2 7.4	1.5 1.5	8.8 8.1	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{CE}$ to $\overline{RC}$		2	1.5 1.5	5.5 5.3	6.7 6.5	1.5 1.5	7.3 7.1	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{U}$/D to $\overline{RC}$		2	1.5 1.5	8.1 7.7	10.1 9.4	1.5 1.5	11.0 10.4	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{U}$/D to TC		4	1.5 1.5	6.3 6.5	8.1 8.2	1.5 1.5	9.0 8.9	ns
t_{PLH} t_{PHL}	Propagation delay D_n to Q_n		3	1.5 1.5	7.0 6.8	8.4 8.2	1.5 1.5	9.3 9.0	ns
t_{PLH} t_{PHL}	Propagation delay D_n to TC		3, 4	1.5 1.5	9.5 8.8	11.7 11.3	1.5 1.5	13.0 12.3	ns
t_{PLH} t_{PHL}	Propagation delay D_n to $\overline{RC}$		3, 4	1.5 1.5	10.4 10.7	12.9 13.0	1.5 1.5	14.4 14.5	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{PL}$ to Q_n		5	1.5 1.5	7.6 7.1	9.0 8.5	1.5 1.5	9.9 9.3	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{PL}$ to TC		5	1.5 1.5	10.0 9.4	12.0 11.5	1.5 1.5	13.4 12.7	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{PL}$ to $\overline{RC}$		5	1.5 1.5	10.9 11.3	13.1 13.2	1.5 1.5	14.4 14.7	ns
$t_S(H)$ $t_S(L)$	Setup time, High or Low D_n to $\overline{PL}$		6	2.5			2.5		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low D_n to $\overline{PL}$		6	1.0			1.0		ns
$t_S(H)$ $t_S(L)$	Setup time, High or Low $\overline{CE}$ to CP		6	6.5			6.5		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low $\overline{CE}$ to CP		6	0.5			0.5		ns
$t_S(H)$ $t_S(L)$	Setup time, High or Low $\overline{U}$/D to CP		6	7.5			7.5		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low $\overline{U}$/D to CP		6	0.0			0.0		ns
$t_w(L)$	$\overline{PL}$ pulse width, Low		5	3.0			3.0		ns
$t_w(H)$ $t_w(L)$	CP pulse width, High or Low		1	6.3			6.3		ns
t_{REC}	Recover time, $\overline{PL}$ to CP		5	2.0			2.0		ns

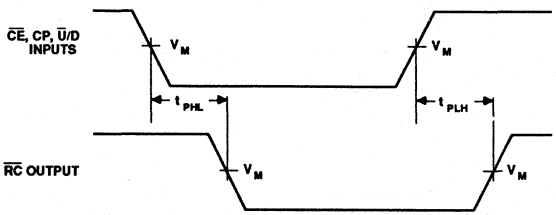
AC ELECTRICAL CHARACTERISTICS AT 5.0V ±0.5V

SYMBOL	PARAMETER		WAVEFORM	74ACT11191					UNIT
				T_A = +25°C			T_A = -40°C to +85°C		
				Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	CP to Q_n	1	90	120		90		MHz
		CP to $\overline{RC}$, TC		90	120		90		MHz
t_{PLH} t_{PHL}	Propagation delay CP to Q_n		1	1.5 1.5	7.3 7.6	9.1 9.2	1.5 1.5	9.9 10.1	ns
t_{PLH} t_{PHL}	Propagation delay CP to TC		1	1.5 1.5	8.8 9.3	10.6 11.1	1.5 1.5	11.7 12.3	ns
t_{PLH} t_{PHL}	Propagation delay CP to $\overline{RC}$		2	1.5 1.5	8.0 7.7	9.8 9.3	1.5 1.5	10.7 10.2	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{CE}$ to $\overline{RC}$		2	1.5 1.5	6.8 6.8	8.4 8.4	1.5 1.5	9.2 9.1	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{U}$/D to $\overline{RC}$		2	1.5 1.5	9.6 9.3	12.1 11.4	1.5 1.5	13.1 12.6	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{U}$/D to TC		4	1.5 1.5	7.9 8.1	9.9 10.4	1.5 1.5	11.2 11.4	ns
t_{PLH} t_{PHL}	Propagation delay D_n to Q_n		3	1.5 1.5	8.4 8.3	10.3 10.2	1.5 1.5	11.4 11.2	ns
t_{PLH} t_{PHL}	Propagation delay D_n to TC		3, 4	1.5 1.5	11.0 10.3	13.8 13.4	1.5 1.5	15.4 14.7	ns
t_{PLH} t_{PHL}	Propagation delay D_n to $\overline{RC}$		3, 4	1.5 1.5	11.8 12.2	14.9 15.1	1.5 1.5	16.5 16.8	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{PL}$ to Q_n		5	1.5 1.5	9.1 8.6	11.0 10.5	1.5 1.5	12.2 11.4	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{PL}$ to TC		5	1.5 1.5	11.4 10.9	14.1 13.5	1.5 1.5	15.6 14.9	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{PL}$ to $\overline{RC}$		5	1.5 1.5	12.3 12.7	15.3 15.5	1.5 1.5	17.0 17.3	ns
$t_S(H)$ $t_S(L)$	Setup time, High or Low D_n to $\overline{PL}$		6	2.5			2.5		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low D_n to $\overline{PL}$		6	2.0			2.0		ns
$t_S(H)$ $t_S(L)$	Setup time, High or Low $\overline{CE}$ to CP		6	6.5			6.5		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low $\overline{CE}$ to CP		6	1.5			1.5		ns
$t_S(H)$ $t_S(L)$	Setup time, High or Low $\overline{U}$/D to CP		6	7.5			7.5		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low $\overline{U}$/D to CP		6	0.5			0.5		ns
$t_w(L)$	$\overline{PL}$ pulse width, Low		5	3.0			3.0		ns
$t_w(H)$ $t_w(L)$	CP pulse width, High or Low		1	5.6			5.6		ns
t_{REC}	Recover time, $\overline{PL}$ to CP		5	2.0			2.0		ns

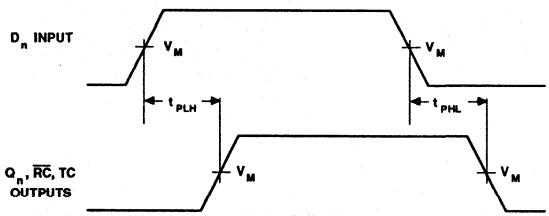
AC WAVEFORMS



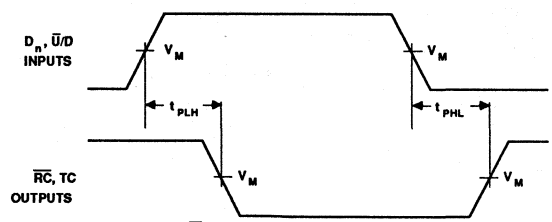
Waveform 1. Waveforms Showing Clock to Outputs Propagation Delays and Clock Pulse Width



Waveform 2. Waveforms Showing the Clock, Count Enable, or U/D to Ripple Clock Output Propagation Delay

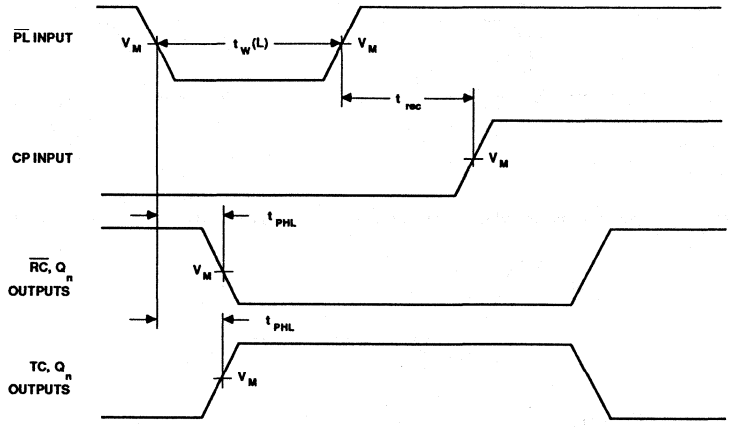


Waveform 3. Waveforms Showing the Input (D_n) to Output (Q_n, $\overline{RC}$, TC) Propagation Delays, Non-Inverting Path

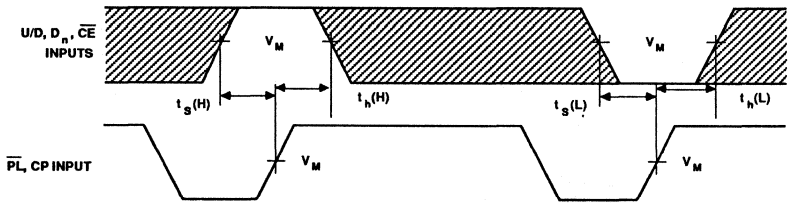


Waveform 4. Waveforms Showing the Input (D_n, $\overline{U}$/D) to Output ($\overline{RC}$, TC) Propagation Delays, Inverting Path

AC WAVEFORMS



Waveform 5. Waveforms Showing the Parallel Load Pulse Width, Parallel Load to Output Delay and Parallel Load to Clock Recovery Time

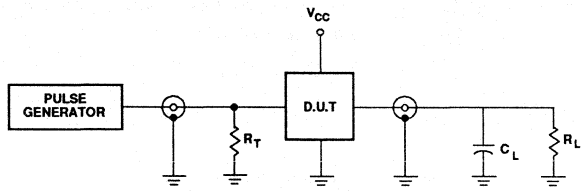


Waveform 6. Waveforms Showing Setup Time and Hold Time for D_n to $\overline{PL}$, $\overline{U}$/D to CP and $\overline{CE}$ to CP

WAVEFORM CONDITIONS

	INPUTS	OUTPUTS
AC	V_{IN} = GND to V_{CC}, V_M = 50% V_{CC}	$V_{OUT} = V_{OL}$ to V_{OH}
ACT	V_{IN} = GND to 3.0V, V_M = 1.5V	V_M = 50% V_{CC}

TEST CIRCUIT



Test Circuit

DEFINITIONS

C_L = Load capacitance, 50pF; includes jig and probe capacitance

R_L = Load resistor, 500Ω

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators

Input pulses: PRR ≤ 10MHz

$t_r = t_f = 3ns$

74AC/ACT11192

Asynchronous Presettable Synchronous BCD Decade Up/ Down Counter w/Dual Clock

Objective Specification

FEATURES

- **Synchronous, reversible counting**
- **Positive edge-triggered clock**
- **BCD/decade**
- **Asynchronous Parallel Load capability**
- **Output capability: ±24mA**
- **CMOS (AC) and TTL (ACT) voltage level inputs**
- **50Ω incident wave switching**
- **Center-pin V_{CC} and ground configuration to minimize high-speed switching noise**
- **I_{CC} category: MSI**

DESCRIPTION

The 74AC/ACT11192 high-performance CMOS devices combine very high speed and high output drive comparable to the most advanced TTL families.

The 74AC/ACT11192 is an asynchronously presettable up/down BCD decade counter. Separate up/down clocks, CP_U and CP_D respectively, simplify operation. the outputs change state synchronously with the Low-to-High transition of either Clock input. If the CP_U clock is pulsed while CP_D is held High, the device will

GENERAL INFORMATION

SYMBOL	PARAMETER	CONDITIONS T_A = 25°C; GND = 0V; V_{CC} = 5.0V	TYPICAL		UNIT
			AC	ACT	
t_{PLH}/ t_{PHL}	Propagation delay CP_x to Q_n ($\overline{PL}$ = High)	C_L = 50pF	6.8	8.5	ns
C_{PD}	Power dissipation capacitance[1]	f = 1MHz; C_L = 50pF	68	70	pF
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	4.0	4.0	pF
I_{LATCH}	Latch-up current	Per Jedec JC40.2 Standard 17	500	500	mA
f_{MAX}	Maximum clock frequency; $CP_x \rightarrow Q_n$	C_L = 50pF	125	110	MHz

Note:

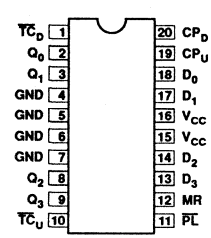
1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_I + \Sigma (C_L \times V_{CC}^2 \times f_O)$ where:
   f_I = input frequency in MHz, C_L = output load capacitance in pF,
   f_O = output frequency in MHz, V_{CC} = supply voltage in V,
   $\Sigma (C_L \times V_{CC}^2 \times f_O)$ = sum of outputs

ORDERING INFORMATION

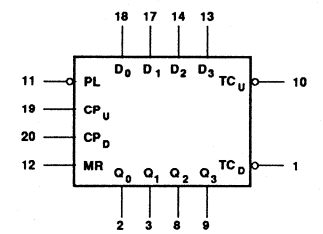
PACKAGES	TEMPERATURE RANGE	ORDER CODE
20-pin plastic DIP (300mil-wide)	-40°C to +85°C	74AC11192N 74ACT11192N
20-pin plastic SO (300mil-wide)	-40°C to +85°C	74AC11192D 74ACT11192D

PIN CONFIGURATION

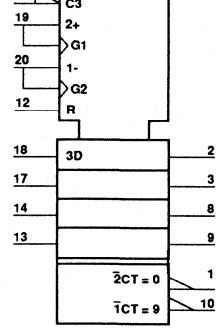
N and D Packages



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



Asynchronous Presettable Synchronous BCD Decade Up/Down Counter w/Dual Clock

74AC/ACT11192

count up, if CP_D is pulsed while CP_U is held High, the device will count down. Only one Clock input can be held High at any time, or erroneous operation will result.

Inside the device are four master-slave JK flip-flops with the necessary steering logic to provide the asynchronous reset, preset load, and synchronous count up and count down functions.

Each flip-flop contains JK feedback from slave to master such that a Low-to-High transition on the CP_D input will decrease the count by one, while a similar transition on the CP_U input will advance the count by one.

One clock must be held High while counting with the other because the circuit will either count by two's or not at all depending on the state of the first flip-flop, which cannot toggle as long as either Clock input is Low. Applications requiring reversible operation must make the reversing decision while the activating clock is High to avoid erroneous counts.

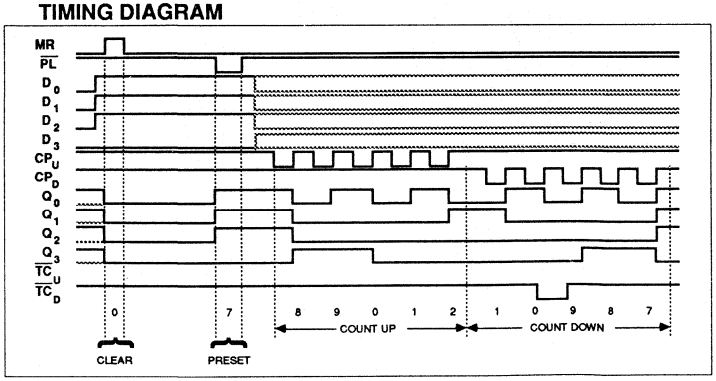
The Terminal Count Up ($\overline{TC}_U$) and Terminal Count Down ($\overline{TC}_D$) outputs are normally High. When the circuit has reached the maximum count state of 9, the next High-to-Low transition of CP_U will cause $\overline{TC}_U$ to go Low. $\overline{TC}_U$ will stay Low until CP_U goes High again, duplicating the count up clock, although delayed by two gate delays. Likewise, the $\overline{TC}_D$ output will go Low when the circuit is in the zero state and the CP_D goes Low. The $\overline{TC}$ outputs can be used as the Clock input signals to the next higher order circuit in a multi-stage counter, since they duplicate the clock waveforms. Multi-stage counters will not be fully synchronous, since there is a two-gate delay time difference added for each stage that is added.

Asynchronous Parallel Load capability permits the counter to be preset to any desired number. Information present on the parallel Data inputs (D_0 - D_3) is loaded into the counter and appears on the outputs when the Parallel Load ($\overline{PL}$) input is Low. A High level on the Master Reset (MR) input will disable the parallel load gates, override both Clock inputs, and set all Q outputs Low. If one of the Clock inputs is Low during and after a reset or load operation, the next Low-to-High transition of that clock will be interpreted as a legitimate signal and will be counted.

PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
12	MR	Master reset input
11	$\overline{PL}$	Parallel load input (active-Low)
19	CP_U	Count up clock input (active rising edge)
20	CP_D	Count down clock input (active rising edge)
18, 17, 14, 13	D_0 - D_3	Data inputs
2, 3, 8, 9	Q_0 - Q_3	Counter outputs
10	$\overline{TC}_U$	Terminal count up (carry) output (active-Low)
1	$\overline{TC}_D$	Terminal count down (carry) output (active-Low)
4, 5, 6, 7	GND	Ground (0V)
15, 16	V_{CC}	Positive supply voltage

TIMING DIAGRAM



Asynchronous Presettable Synchronous BCD Decade Up/Down Counter w/Dual Clock

74AC/ACT11192

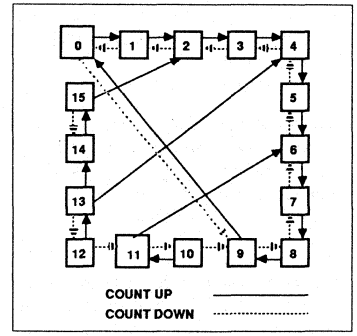
MODE SELECT—FUNCTION TABLE

OPERATING MODE	INPUTS								OUTPUTS					
	MR	$\overline{PL}$	CP_U	CP_D	D_0	D_1	D_2	D_3	Q_0	Q_1	Q_2	Q_3	$\overline{TC}_U$	$\overline{TC}_D$
Reset (clear)	H	X	X	L	X	X	X	X	L	L	L	L	H	L
	H	X	X	H	X	X	X	X	L	L	L	L	H	H
Parallel load	L	L	X	L	L	L	L	L	L	L	L	L	H	L
	L	L	X	H	L	L	L	L	L	L	L	L	H	H
	L	L	L	X	H	X	X	H	$Q_n = D_n$				L	H
	L	L	H	X	H	X	X	H	$Q_n = D_n$				H	H
Count up	L	H	↑	H	X	X	X	X	Count up				H(1)	H
Count down	L	H	H	↑	X	X	X	X	Count down				H	H(2)

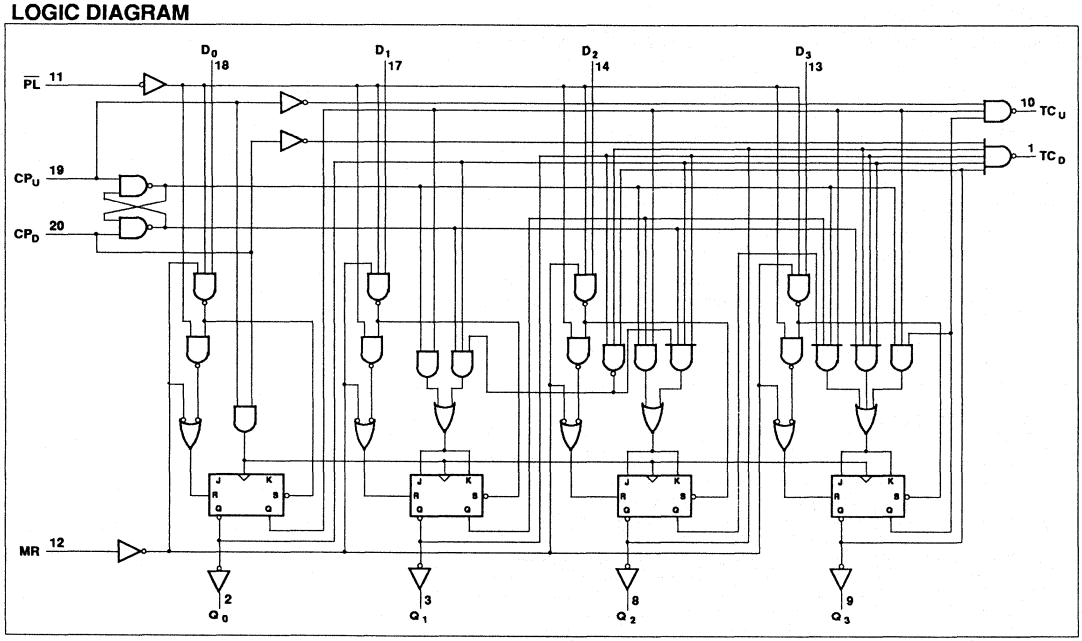
H = High voltage level
L = Low voltage level
X = Don't care
↑ =Low-to-High clock transition

NOTES:
1. $\overline{TC}_U$ = CPU at terminal count up (HLLH).
2. $\overline{TC}_D$ = CPD at terminal count down (LLLL).

STATE DIAGRAM



LOGIC DIAGRAM



RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	74AC11192			74ACT11192			UNIT
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	DC supply voltage	3.0[1]	5.0	5.5	4.5	5.0	5.5	V
V_I	Input voltage	0		V_{CC}	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	0		V_{CC}	V
$\Delta t/\Delta v$	Input transition rise or fall rate	0		10	0		10	ns/V
T_A	Operating free-air temperature	-40		+85	-40		+85	°C

NOTE:

1. No electrical or switching characteristics are specified at V_{CC} < 3V. Operation between 2V and 3V is not recommended, but within that range, a device output will maintain a previously established logic state.

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	TEST CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 to+7.0	V
I_{IK} or V_I	DC input diode current[2]	$V_I < 0$	-20	mA
		$V_I > V_{CC}$	20	
	DC input voltage		-0.5 to V_{CC} +0.5	V
I_{OK} or V_O	DC output diode current[2]	$V_O < 0$	-50	mA
		$V_O > V_{CC}$	50	
	DC output voltage		-0.5 to V_{CC} +0.5	V
I_O	DC output source or sink current per output pin	V_O = 0 to V_{CC}	±50	mA
I_{CC} or I_{GND}	DC V_{CC} current		±150	mA
	DC ground current		±150	
T_{STG}	Storage temperature		-65 to 150	°C
P_{TOT}	Power dissipation per package Plastic DIP	Above 70°C:derate linearly by 8mW/K	500	mW
	Power dissipation per package Plastic surface mount (SO)	Above 70°C:derate linearly by 6mW/K	400	mW

NOTES:

1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		V_{CC}	74AC11192				74ACT11192				UNIT
					T_A = +25°C		T_A = -40°C to +85°C		T_A = +25°C		T_A = -40°C to +85°C		
				V	Min	Max	Min	Max	Min	Max	Min	Max	
V_{IH}	High-level input voltage			3.0	2.10		2.10						V
				4.5	3.15		3.15		2.0		2.0		
				5.5	3.85		3.85		2.0		2.0		
V_{IL}	Low-level input voltage			3.0		0.90		0.90					V
				4.5		1.35		1.35		0.8		0.8	
				5.5		1.65		1.65		0.8		0.8	
V_{OH}	High-level output voltage	V_I = V_{IL} or V_{IH}	I_{OH} = -50μA	3.0	2.9		2.9						V
				4.5	4.4		4.4		4.4		4.4		
				5.5	5.4		5.4		5.4		5.4		
			I_{OH} = -4mA	3.0	2.58		2.48						
			I_{OH} = -24mA	4.5	3.94		3.8		3.94		3.8		
				5.5	4.94		4.8		4.94		4.8		
			I_{OH} = -75mA[1]	5.5			3.85				3.85		
V_{OL}	Low-level output voltage	V_I = V_{IL} or V_{IH}	I_{OL} = 50μA	3.0		0.1		0.1					V
				4.5		0.1		0.1		0.1		0.1	
				5.5		0.1		0.1		0.1		0.1	
			I_{OL} = 12mA	3.0		0.36		0.44					
			I_{OL} = 24mA	4.5		0.36		0.44		0.36		0.44	
				5.5		0.36		0.44		0.36		0.44	
			I_{OL} = 75mA[1]	5.5				1.65				1.65	
I_I	Input leakage current	V_I = V_{CC} or GND		5.5		±0.1		±1.0		±0.1		±1.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC} or GND, I_O = 0		5.5		8.0		80		8.0		80	μA
ΔI_{CC}	Supply current, TTL inputs High[2]	One input at 3.4V, other inputs at V_{CC} or GND		5.5						0.9		1.0	mA

NOTES:
1. Not more than one output should be tested at a time, and the duration of the test should not exceed 10ms.
2. This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0V or V_{CC}.

74AC/ACT11193

Asynchronous Presettable Synchronous 4-Bit Binary Up/ Down Counter w/Dual Clock

Objective Specification

FEATURES

- **Synchronous, reversible counting**
- **Positive edge-triggered clock**
- **4-bit binary**
- **Asynchronous Parallel Load capability**
- **Output capability: ±24mA**
- **CMOS (AC) and TTL (ACT) voltage level inputs**
- **50Ω incident wave switching**
- **Center-pin V_{CC} and ground configuration to minimize high-speed switching noise**
- **I_{CC} category: MSI**

DESCRIPTION

The 74AC/ACT11193 high-performance CMOS devices combine very high speed and high output drive comparable to the most advanced TTL families.

The 74AC/ACT11193 is an asynchronously presettable up/down 4-bit binary counter. Separate up/down clocks, CP_U and CP_D respectively, simplify operation. the outputs change state synchronously with the Low-to-High transition of either Clock input. If the CP_U clock is pulsed while CP_D is held High, the device will

GENERAL INFORMATION

SYMBOL	PARAMETER	CONDITIONS T_A = 25°C; GND = 0V; V_{CC} = 5.0V	TYPICAL		UNIT
			AC	ACT	
t_{PLH}/ t_{PHL}	Propagation delay CP_x to Q_n ($\overline{PL}$ = High)	C_L = 50pF	6.8	8.5	ns
C_{PD}	Power dissipation capacitance[1]	f = 1MHz; C_L = 50pF	68	70	pF
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	4.0	4.0	pF
I_{LATCH}	Latch-up current	Per Jedec JC40.2 Standard 17	500	500	mA
f_{MAX}	Maximum clock frequency; $CP_x \rightarrow Q_n$	C_L = 50pF	125	110	MHz

Note:

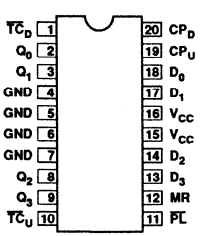
1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_I + \Sigma (C_L \times V_{CC}^2 \times f_O)$ where:
   f_I = input frequency in MHz, C_L = output load capacitance in pF,
   f_O = output frequency in MHz, V_{CC} = supply voltage in V,
   $\Sigma (C_L \times V_{CC}^2 \times f_O)$ = sum of outputs

ORDERING INFORMATION

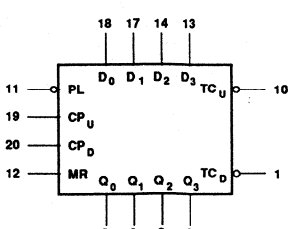
PACKAGES	TEMPERATURE RANGE	ORDER CODE
20-pin plastic DIP (300mil-wide)	-40°C to +85°C	74AC11193N 74ACT11193N
20-pin plastic SO (300mil-wide)	-40°C to +85°C	74AC11193D 74ACT11193D

PIN CONFIGURATION

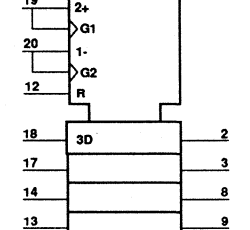
N and D Packages



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



Asynchronous Presettable Synchronous 4-Bit Binary Up/Down Counter w/Dual Clock

74AC/ACT11193

count up, if CP_D is pulsed while CP_U is held High, the device will count down. Only one Clock input can be held High at any time, or erroneous operation will result.

Inside the device are four master-slave JK flip-flops with the necessary steering logic to provide the asynchronous reset, preset load, and synchronous count up and count down functions.

Each flip-flop contains JK feedback from slave to master such that a Low-to-High transition on the CP_D input will decrease the count by one, while a similar transition on the CP_U input will advance the count by one.

One clock must be held High while counting with the other because the circuit will either count by two's or not at all depending on the state of the first flip-flop, which cannot toggle as long as either Clock input is Low. Applications requiring reversible operation must make the reversing decision while the activating clock is High to avoid erroneous counts.

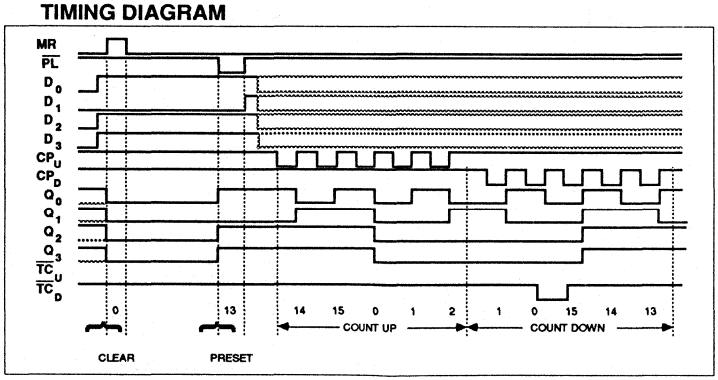
The Terminal Count Up ($\overline{TC_U}$) and Terminal Count Down ($\overline{TC_D}$) outputs are normally High. When the circuit has reached the maximum count state of 15, the next High-to-Low transition of CP_U will cause $\overline{TC_U}$ to go Low. $\overline{TC_U}$ will stay Low until CP_U goes High again, duplicating the count up clock, although delayed by two gate delays. Likewise, the $\overline{TC_D}$ output will go Low when the circuit is in the zero state and the CP_D goes Low. The $\overline{TC}$ outputs can be used as the Clock input signals to the next higher order circuit in a multi-stage counter, since they duplicate the clock waveforms. Multi-stage counters will not be fully synchronous, since there is a two-gate delay time difference added for each stage that is added.

Asynchronous Parallel Load capability permits the counter to be preset to any desired number. Information present on the parallel Data inputs (D_0 - D_3) is loaded into the counter and appears on the outputs when the Parallel Load ($\overline{PL}$) input is Low. A High level on the Master Reset (MR) input will disable the parallel load gates, override both Clock inputs, and set all Q outputs Low. If one of the Clock inputs is Low during and after a reset or load operation, the next Low-to-High transition of that clock will be interpreted as a legitimate signal and will be counted.

PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
12	MR	Master reset input
11	$\overline{PL}$	Parallel load input (active-Low)
19	CP_U	Count up clock input (active rising edge)
20	CP_D	Count down clock input (active rising edge)
18, 17, 14, 13	D_0 - D_3	Data inputs
2, 3, 8, 9	Q_0 - Q_3	Counter outputs
10	$\overline{TC_U}$	Terminal count up (carry) output (active-Low)
1	$\overline{TC_D}$	Terminal count down (carry) output (active-Low)
4, 5, 6, 7	GND	Ground (0V)
15, 16	V_{CC}	Positive supply voltage

TIMING DIAGRAM



Asynchronous Presettable Synchronous 4-Bit Binary Up/Down Counter w/Dual Clock

74AC/ACT11193

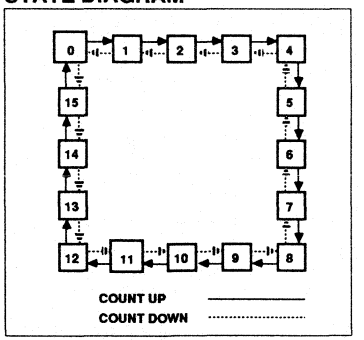
MODE SELECT—FUNCTION TABLE

OPERATING MODE	INPUTS								OUTPUTS					
	MR	$\overline{PL}$	CP_U	CP_D	D_0	D_1	D_2	D_3	Q_0	Q_1	Q_2	Q_3	$\overline{TC}_U$	$\overline{TC}_D$
Reset (clear)	H	X	X	L	X	X	X	X	L	L	L	L	H	L
	H	X	X	H	X	X	X	X	L	L	L	L	H	H
Parallel load	L	L	X	L	L	L	L	L	L	L	L	L	H	L
	L	L	X	H	L	L	L	L	L	L	L	L	H	H
	L	L	L	X	H	H	H	H	H	H	H	H	L	H
	L	L	H	X	H	H	H	H	H	H	H	H	H	H
Count up	L	H	↑	H	X	X	X	X	Count up				H(1)	H
Count down	L	H	H	↑	X	X	X	X	Count down				H	H(2)

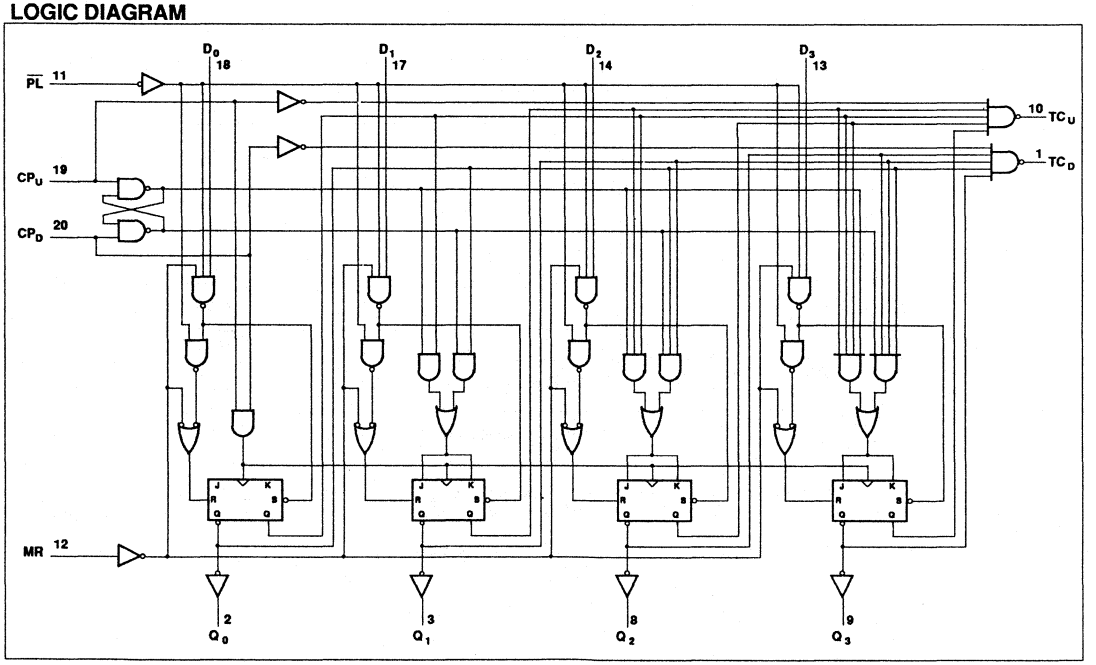
H = High voltage level
L = Low voltage level
X = Don't care
↑ =Low-to-High clock transition

NOTES:
1. $\overline{TC}_U$ = CPU at terminal count up (HHHH).
2. $\overline{TC}_D$ = CPD at terminal count down (LLLL).

STATE DIAGRAM



LOGIC DIAGRAM



RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	74AC11193			74ACT11193			UNIT
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	DC supply voltage	3.0[1]	5.0	5.5	4.5	5.0	5.5	V
V_I	Input voltage	0		V_{CC}	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	0		V_{CC}	V
$\Delta t/\Delta v$	Input transition rise or fall rate	0		10	0		10	ns/V
T_A	Operating free-air temperature	-40		+85	-40		+85	°C

NOTE:

1. No electrical or switching characteristics are specified at $V_{CC} < 3V$. Operation between 2V and 3V is not recommended, but within that range, a device output will maintain a previously established logic state.

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	TEST CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 to+7.0	V
I_{IK} or V_I	DC input diode current[2]	$V_I < 0$	-20	mA
		$V_I > V_{CC}$	20	
	DC input voltage		-0.5 to V_{CC} +0.5	V
I_{OK} or V_O	DC output diode current[2]	$V_O < 0$	-50	mA
		$V_O > V_{CC}$	50	
	DC output voltage		-0.5 to V_{CC} +0.5	V
I_O	DC output source or sink current per output pin	V_O = 0 to V_{CC}	±50	mA
I_{CC} or I_{GND}	DC V_{CC} current		±150	mA
	DC ground current		±150	
T_{STG}	Storage temperature		-65 to 150	°C
P_{TOT}	Power dissipation per package Plastic DIP	Above 70°C:derate linearly by 8mW/K	500	mW
	Power dissipation per package Plastic surface mount (SO)	Above 70°C:derate linearly by 6mW/K	400	mW

NOTES:

1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		V_{CC}	74AC11193				74ACT11193				UNIT
					T_A = +25°C		T_A = -40°C to +85°C		T_A = +25°C		T_A = -40°C to +85°C		
				V	Min	Max	Min	Max	Min	Max	Min	Max	
V_{IH}	High-level input voltage			3.0	2.10		2.10						V
				4.5	3.15		3.15		2.0		2.0		
				5.5	3.85		3.85		2.0		2.0		
V_{IL}	Low-level input voltage			3.0		0.90		0.90					V
				4.5		1.35		1.35		0.8		0.8	
				5.5		1.65		1.65		0.8		0.8	
V_{OH}	High-level output voltage	V_I = V_{IL} or V_{IH}	I_{OH} = -50µA	3.0	2.9		2.9						V
				4.5	4.4		4.4		4.4		4.4		
				5.5	5.4		5.4		5.4		5.4		
			I_{OH} = -4mA	3.0	2.58		2.48						
			I_{OH} = -24mA	4.5	3.94		3.8		3.94		3.8		
				5.5	4.94		4.8		4.94		4.8		
			I_{OH} = -75mA[1]	5.5			3.85				3.85		
V_{OL}	Low-level output voltage	V_I = V_{IL} or V_{IH}	I_{OL} = 50µA	3.0		0.1		0.1					V
				4.5		0.1		0.1		0.1		0.1	
				5.5		0.1		0.1		0.1		0.1	
			I_{OL} = 12mA	3.0		0.36		0.44					
			I_{OL} = 24mA	4.5		0.36		0.44		0.36		0.44	
				5.5		0.36		0.44		0.36		0.44	
			I_{OL} = 75mA[1]	5.5				1.65				1.65	
I_I	Input leakage current	V_I = V_{CC} or GND		5.5		±0.1		±1.0		±0.1		±1.0	µA
I_{CC}	Quiescent supply current	V_I = V_{CC} or GND, I_O = 0		5.5		8.0		80		8.0		80	µA
ΔI_{CC}	Supply current, TTL inputs High[2]	One input at 3.4V, other inputs at V_{CC} or GND		5.5						0.9		1.0	mA

NOTES:
1. Not more than one output should be tested at a time, and the duration of the test should not exceed 10ms.
2. This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0V or V_{CC}.

74AC/ACT11194

4-Bit Bidirectional Universal Shift Register

Preliminary Specification

FEATURES

- **Shift left and shift right capability**
- **Synchronous Parallel and Serial data transfers**
- **Easily expanded for both Serial and Parallel operation**
- **Asynchronous reset**
- **Output capability: ±24mA**
- **CMOS (AC) and TTL (ACT) voltage level inputs**
- **50Ω incident wave switching**
- **Center-pin V_{CC} and ground configuration to minimize high-speed switching noise**
- **I_{CC} category: MSI**

DESCRIPTION

The 74AC/ACT11194 high-performance CMOS devices combine very high speed and high output drive comparable to the most advanced TTL families.

The 74AC/ACT11194 4-bit Bidirectional Universal Shift Register is fully synchronous, making the device especially useful for implementing very high speed CPUs, or for memory buffer registers.

GENERAL INFORMATION

SYMBOL	PARAMETER	CONDITIONS T_A = 25°C; GND = 0V; V_{CC} = 5.0V	TYPICAL		UNIT
			AC	ACT	
t_{PLH}/ t_{PHL}	Propagation delay CP to Q_n ($\overline{MR}$ = High)	C_L = 50pF	4.8	5.8	ns
C_{PD}	Power dissipation capacitance[1]	f = 1MHz; C_L = 50pF	66	69	pF
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	3.5	3.5	pF
I_{LATCH}	Latch-up current	Per Jedec JC40.2 Standard 17	500	500	mA
f_{MAX}	Maximum clock frequency	C_L = 50pF	150	130	MHz

Note:

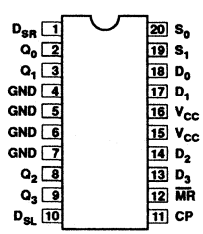
1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_I + \Sigma (C_L \times V_{CC}^2 \times f_O)$ where:
   f_I = input frequency in MHz, C_L = output load capacitance in pF,
   f_O = output frequency in MHz, V_{CC} = supply voltage in V,
   $\Sigma (C_L \times V_{CC}^2 \times f_O)$ = sum of outputs

ORDERING INFORMATION

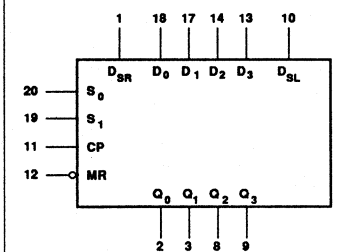
PACKAGES	TEMPERATURE RANGE	ORDER CODE
20-pin plastic DIP (300mil-wide)	-40°C to +85°C	74AC11194N 74ACT11194N
20-pin plastic SO (300mil-wide)	-40°C to +85°C	74AC11194D 74ACT11194D

PIN CONFIGURATION

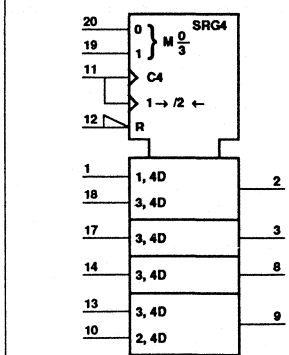
N and D Packages



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



The 74AC/ACT11194 design has special logic features which increase the range of application. The synchronous operation of the device is determined by two Mode Select inputs, S_0 and S_1. As shown in the Function Table, data can be entered and shifted from left to right (shift right, $Q_0 \rightarrow Q_1$, etc.), or right to left (shift left, $Q_3 \rightarrow Q_2$, etc.), or parallel data can be entered, loading all 4 bits of the register simultaneously. When both S_0 and S_1 are Low, existing data is retained in a hold (do nothing) mode. The first and last stages provide D-type Serial Data input (D_{SR}, D_{SL}) to allow multistage shift right or shift left data transfers without interfering with parallel load operation.

The only timing restriction is that the Mode Control and selected Data inputs must be stable one setup time prior to the positive transition of the clock pulse. Signals on the Select (S_0, S_1), Parallel Data (D_0 - D_3) and Serial Data (D_{SR}, D_{SL}) inputs can change when the clock is in either state, provided only the recommended setup and hold times, with respect to the clock rising edge are observed.

The four Parallel Data inputs (D_0 - D_3) are D-type inputs. Data appearing on D_0 - D_3 inputs when S_0 and S_1 are High is transferred to the Q_0 - Q_3 outputs respectively, following the next Low-to-High transition of the clock. When Low, the asynchronous Master Reset ($\overline{MR}$) overrides all other input conditions and forces the Q outputs Low.

PIN DESCRIPTION

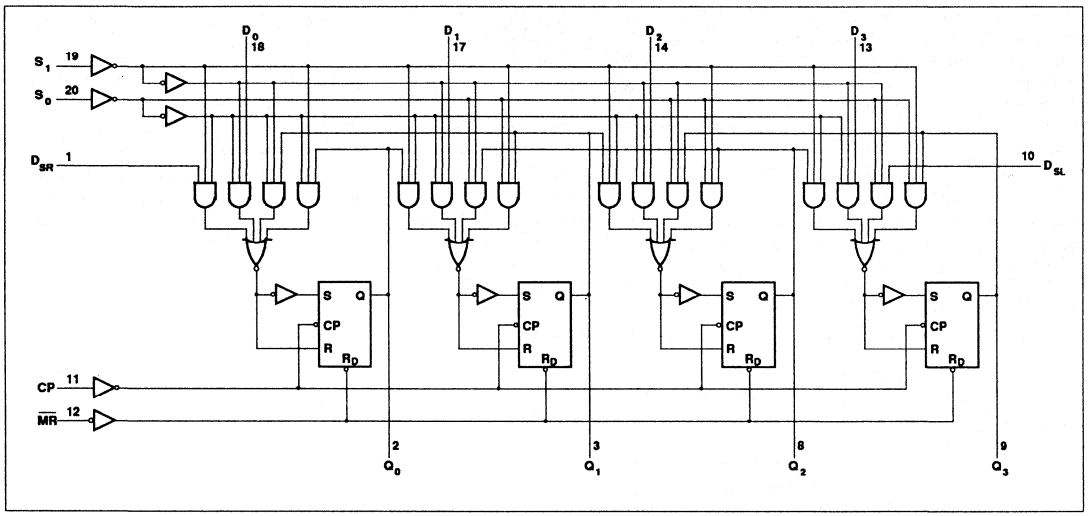
PIN NUMBER	SYMBOL	NAME AND FUNCTION
12	$\overline{MR}$	Asynchronous master reset (active Low)
11	CP	Clock input (Low-to-High, edge-triggered)
18, 17, 14, 13	D_0 - D_3	Data inputs
1	D_{SR}	Serial data input (shift right)
10	D_{SL}	Serial data input (shift left)
20, 19	S_0, S_1	Mode control inputs
2, 3, 8, 9	Q_0 - Q_3	Parallel outputs outputs
4, 5, 6, 7	GND	Ground (0V)
15, 16	V_{CC}	Positive supply voltage

FUNCTION TABLE

OPERATING MODE	INPUTS							OUTPUTS			
	CP	$\overline{MR}$	S_1	S_0	D_{SR}	D_{SL}	D_n	Q_0	Q_1	Q_2	Q_3
Reset (clear)	X	L	X	X	X	X	X	L	L	L	L
Hold (do nothing)	X	H	l	l	X	X	X	q_0	q_1	q_2	q_3
Shift Left	↑	H	h	l	X	l	X	q_1	q_2	q_3	L
	↑	H	h	l	X	h	X	q_1	q_2	q_3	H
Shift Right	↑	H	l	h	l	X	X	L	q_0	q_1	q_2
	↑	H	l	h	h	X	X	H	q_0	q_1	q_2
Parallel Load	↑	H	h	h	X	X	dn	d_0	d_1	d_2	d_3

H = High voltage level
L = Low voltage level
h = High voltage level one setup time prior to the Low-to High clock transition
l = Low voltage level one setup time prior to the Low-to High clock transition
X = Don't care
d_n (q_n) = State of the referenced input (or output) one setup time prior to the Low-to-High clock transition
↑ = Low-to-High clock transition

LOGIC DIAGRAM



RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	74AC11194			74ACT11194			UNIT
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	DC supply voltage	3.0[1]	5.0	5.5	4.5	5.0	5.5	V
V_I	Input voltage	0		V_{CC}	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	0		V_{CC}	V
$\Delta t/\Delta v$	Input transition rise or fall rate	0		10	0		10	ns/V
T_A	Operating free-air temperature	-40		+85	-40		+85	°C

NOTE:
1. No electrical or switching characteristics are specified at $V_{CC} < 3V$. Operation between 2V and 3V is not recommended, but within that range, a device output will maintain a previously established logic state.

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	TEST CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 to+7.0	V
I_{IK} or V_I	DC input diode current[2]	$V_I < 0$	-20	mA
		$V_I > V_{CC}$	20	
	DC input voltage		-0.5 to V_{CC} +0.5	V
I_{OK} or V_O	DC output diode current[2]	$V_O < 0$	-50	mA
		$V_O > V_{CC}$	50	
	DC output voltage		-0.5 to V_{CC} +0.5	V
I_O	DC output source or sink current per output pin	V_O = 0 to V_{CC}	±50	mA
I_{CC} or I_{GND}	DC V_{CC} current		±100	mA
	DC ground current		±100	
T_{STG}	Storage temperature		-65 to 150	°C
P_{TOT}	Power dissipation per package Plastic DIP	Above 70°C:derate linearly by 8mW/K	500	mW
	Power dissipation per package Plastic surface mount (SO)	Above 70°C:derate linearly by 6mW/K	400	mW

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		V_{CC}	74AC11194				74ACT11194				UNIT
					T_A = +25°C		T_A = -40°C to +85°C		T_A = +25°C		T_A = -40°C to +85°C		
				V	Min	Max	Min	Max	Min	Max	Min	Max	
V_{IH}	High-level input voltage			3.0	2.10		2.10						V
				4.5	3.15		3.15		2.0		2.0		
				5.5	3.85		3.85		2.0		2.0		
V_{IL}	Low-level input voltage			3.0		0.90		0.90					V
				4.5		1.35		1.35		0.8		0.8	
				5.5		1.65		1.65		0.8		0.8	
V_{OH}	High-level output voltage	V_I = V_{IL} or V_{IH}	I_{OH} = -50μA	3.0	2.9		2.9						V
				4.5	4.4		4.4		4.4		4.4		
				5.5	5.4		5.4		5.4		5.4		
			I_{OH} = -4mA	3.0	2.58		2.48						
			I_{OH} = -24mA	4.5	3.94		3.8		3.94		3.8		
				5.5	4.94		4.8		4.94		4.8		
			I_{OH} = -75mA[1]	5.5			3.85				3.85		
V_{OL}	Low-level output voltage	V_I = V_{IL} or V_{IH}	I_{OL} = 50μA	3.0		0.1		0.1					V
				4.5		0.1		0.1		0.1		0.1	
				5.5		0.1		0.1		0.1		0.1	
			I_{OL} = 12mA	3.0		0.36		0.44					
			I_{OL} = 24mA	4.5		0.36		0.44		0.36		0.44	
				5.5		0.36		0.44		0.36		0.44	
			I_{OL} = 75mA[1]	5.5				1.65				1.65	
I_I	Input leakage current	V_I = V_{CC} or GND		5.5		±0.1		±1.0		±0.1		±1.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC} or GND, I_O = 0		5.5		8.0		80		8.0		80	μA
ΔI_{CC}	Supply current, TTL inputs High[2]	One input at 3.4V, other inputs at V_{CC} or GND		5.5						0.9		1.0	mA

NOTES:
1. Not more than one output should be tested at a time, and the duration of the test should not exceed 10ms.
2. This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0V or V_{CC}.

AC ELECTRICAL CHARACTERISTICS AT 3.3V ±0.3V

SYMBOL	PARAMETER	WAVEFORM	74AC11194					UNIT
			T_A = +25°C			T_A = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	1	100	125		100		MHz
t_{PLH} t_{PHL}	Propagation delay CP to Q_n	1	1.5 1.5	6.4 7.1	8.9 9.5	1.5 1.5	9.5 10.2	ns
t_{PHL}	Propagation delay $\overline{MR}$ to Q_n	2	1.5	7.6	10.2	1.5	10.9	ns
t_S	Setup time, High or Low D_n, D_{SR}, D_{SL} to CP	3	4.0			4.0		ns
t_H	Hold time, High or Low CP to D_n, D_{SR}, D_{SL}	3	0.0			0.0		ns
t_S	Setup time, High or Low S_n to CP	3	5.5			5.5		ns
t_H	Hold time, High or Low CP to S_n	3	1.0			1.0		ns
t_W	Clock pulse width (load) High or Low	1	5.0			5.0		ns
t_W	Clock pulse width (count) High or Low	1	5.0			5.0		ns
t_W	$\overline{MR}$ pulse width, Low	2	4.0			4.0		ns
t_{REC}	Recovery time $\overline{MR}$ to CP	2	0.5			0.5		ns

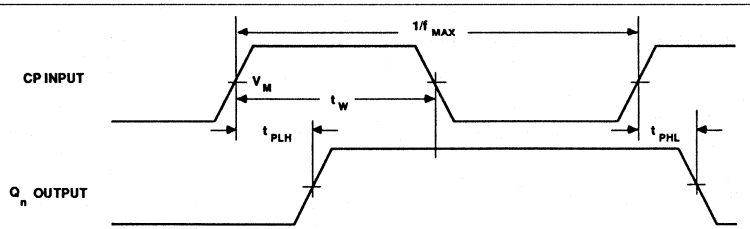
AC ELECTRICAL CHARACTERISTICS AT 5.0V ±0.5V

SYMBOL	PARAMETER	WAVEFORM	74AC11194					UNIT
			T_A = +25°C			T_A = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	1	125	150		125		MHz
t_{PLH} t_{PHL}	Propagation delay CP to Q_n	1	1.5 1.5	4.5 5.0	6.6 7.1	1.5 1.5	7.1 7.7	ns
t_{PHL}	Propagation delay $\overline{MR}$ to Q_n	2	1.5	5.4	7.5	1.5	8.1	ns
t_S	Setup time, High or Low D_n, D_{SR}, D_{SL} to CP	3	0.5			0.5		ns
t_H	Hold time, High or Low CP to D_n, D_{SR}, D_{SL}	3	1.0			1.0		ns
t_S	Setup time, High or Low S_n to CP	3	4.0			4.0		ns
t_H	Hold time, High or Low CP to S_n	3	1.0			1.0		ns
t_W	Clock pulse width (load) High or Low	1	4.0			4.0		ns
t_W	Clock pulse width (count) High or Low	1	4.0			4.0		ns
t_W	$\overline{MR}$ pulse width, Low	2	4.0			4.0		ns
t_{REC}	Recovery time $\overline{MR}$ to CP	2	1.0			1.0		ns

AC ELECTRICAL CHARACTERISTICS AT 5.0V ±0.5V

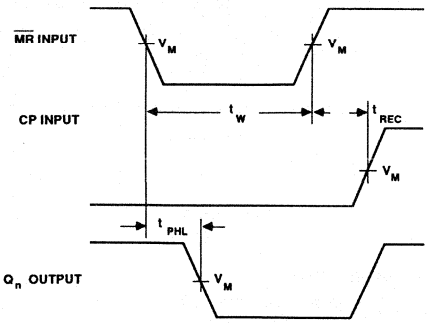
SYMBOL	PARAMETER	WAVEFORM	74ACT11194					UNIT
			T_A = +25°C			T_A = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	1	100	130		100		MHz
t_{PLH} t_{PHL}	Propagation delay CP to Q_n	1	1.5 1.5	5.5 6.1	6.8 7.6	1.5 1.5	7.3 8.3	ns
t_{PHL}	Propagation delay $\overline{MR}$ to Q_n	2	1.5	7.5	9.1	1.5	9.8	ns
t_S	Setup time, High or Low D_n, D_{SR}, D_{SL} to CP	3	4.5			4.5		ns
t_H	Hold time, High or Low CP to D_n, D_{SR}, D_{SL}	3	1.0			1.0		ns
t_S	Setup time, High or Low S_n to CP	3	6.0			6.0		ns
t_H	Hold time, High or Low CP to S_n	3	2.0			2.0		ns
t_W	Clock pulse width (load) High or Low	1	5.0			5.0		ns
t_W	Clock pulse width (count) High or Low	1	5.0			5.0		ns
t_W	$\overline{MR}$ pulse width, Low	2	4.5			4.5		ns
t_{REC}	Recovery time $\overline{MR}$ to CP	2	1.0			1.0		ns

AC WAVEFORMS

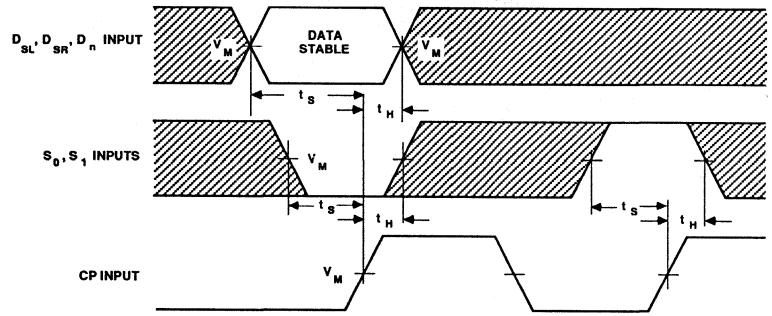


Waveform 1. Waveforms Showing Clock to Outputs Propagation Delays and Clock Pulse Width

AC WAVEFORMS (Continued)



Waveform 2. Waveforms Showing the Master Reset ($\overline{MR}$) Pulse Width, the Master Reset to Output (Q_n) Propagation Delays, and the Master Reset to Clock (CP) Recovery Time

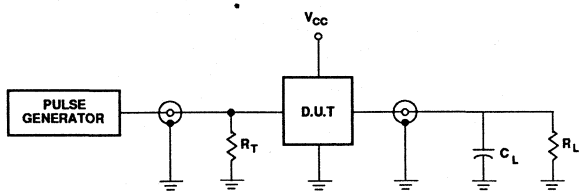


Waveform 3. Waveforms Showing the Data Set-up and Hold Times for the Input (D_n, D_{SL}, D_{SR}) and for S_0 and S_1 Inputs

WAVEFORM CONDITIONS

	INPUTS	OUTPUTS
AC	V_{IN} = GND to V_{CC}, V_M = 50% V_{CC}	V_{OUT} = V_{OL} to V_{OH}
ACT	V_{IN} = GND to 3.0V, V_M = 1.5V	V_M = 50% V_{CC}

TEST CIRCUIT



Test Circuit

DEFINITIONS

C_L = Load capacitance, 50pF; includes jig and probe capacitance

R_L = Load resistor, 500Ω

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators

Input pulses: PRR ≤ 10MHz

$t_r = t_f$ = 3ns

74AC/ACT11208

Dual 1-to-4 Clock Line Driver; 3-State

Objective Specification

FEATURES

- **3-State outputs drive bus lines or buffer memory address registers**
- **Output capability: ±24 mA**
- **CMOS (AC) and TTL (ACT) voltage level inputs**
- **50Ω incident wave switching**
- **Center-pin V_{CC} and ground configuration to minimize high-speed switching noise**
- **I_{CC} category: MSI**

DESCRIPTION

The 74AC/ACT11208 high-performance CMOS devices combine very high speed and high output drive comparable to the most advanced TTL families.

The 74AC/ACT11208 device contains dual line driver circuits which multiplex one input signal to four-outputs with minimum skew. It also has two output enable pins ($1\overline{OE}_1$, $1\overline{OE}_2$, $2\overline{OE}_1$, $2\overline{OE}_2$) for each circuit, which allow the outputs to be disabled to a high-impedance state or to a logical Low or High level.

GENERAL INFORMATION

SYMBOL	PARAMETER	CONDITIONS T_A = 25°C; GND = 0V V_{CC} = 5.0V		TYPICAL AC	TYPICAL ACT	UNIT
t_{PLH}/ t_{PHL}	Propagation delay nA to nY_n	C_L = 50pF		7.1	8.3	ns
t_{SKEW}	Propagation delay skew	C_L = 50pF		0.5	0.5	ns
C_{PD}	Power dissipation capacitance per line driver[1]	f = 1MHz; C_L = 50pF	Enabled	130	125	pF
			Disabled	13	15	
C_{IN}	Input capacitance	V_I = 0V or V_{CC}		4.0	4.0	pF
C_{OUT}	Output capacitance	V_I = 0V or V_{CC}; Disabled		9.0	9.0	pF
I_{LATCH}	Latch-up current	Per Jedec JC40.2 Standard 17		500	500	mA

Note:

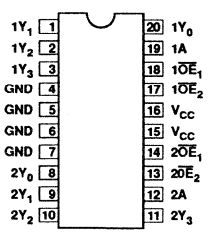
1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_I + \Sigma (C_L \times V_{CC}^2 \times f_O)$ where:
   f_I = input frequency in MHz, C_L = output load capacitance in pF,
   f_O = output frequency in MHz, V_{CC} = supply voltage in V,
   $\Sigma (C_L \times V_{CC}^2 \times f_O)$ = sum of outputs

ORDERING INFORMATION

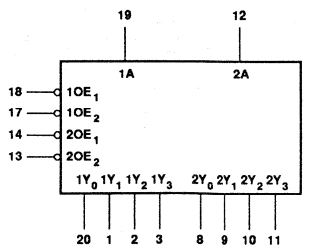
PACKAGES	TEMPERATURE RANGE	ORDER CODE
20-pin plastic DIP (300mil-wide)	-40°C to +85°C	74AC11208N 74ACT11208N
20-pin plastic SO (300mil-wide)	-40°C to +85°C	74AC11208D 74ACT11208D

PIN CONFIGURATION

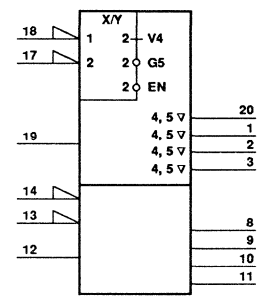
N and D Packages



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



PIN DESCRIPTION

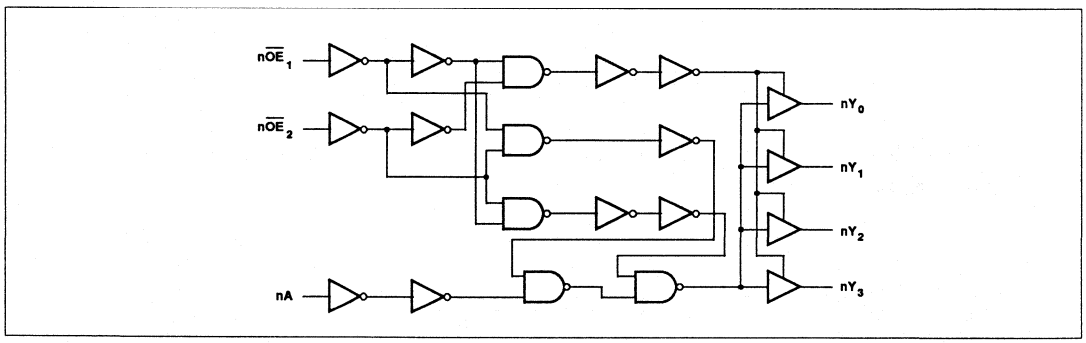
PIN NUMBER	SYMBOL	NAME AND FUNCTION
18, 17	$1\overline{OE}_1$, $1\overline{OE}_2$	3-state output enables (active Low), Side 1
19	1A	Data inputs/outputs, Side 1
20, 1, 2, 3	$1Y_0$ - $1Y_3$	3-State outputs, Side 1
14, 13	$2\overline{OE}_1$, $2\overline{OE}_2$	3-state output enables (active Low), Side 2
12	2A	Data inputs/outputs, Side 2
8, 9, 10, 11	$2Y_0$ - $2Y_3$	3-State outputs, Side 2
4, 5, 6, 7	GND	Ground (0V)
15, 16	V_{CC}	Positive supply voltage

FUNCTION TABLE

INPUTS			OUTPUTS			
$n\overline{OE}_1$	$n\overline{OE}_2$	nA	nY_0	nY_1	nY_2	nY_3
L	L	L	L	L	L	L
L	L	H	H	H	H	H
L	H	X	L	L	L	L
H	L	X	H	H	H	H
H	H	X	Z	Z	Z	Z

H = High voltage level
L = Low volatge level
Z = High-impedance (OFF) state

LOGIC DIAGRAM



RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	74AC11208			74ACT11208			UNIT
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	DC supply voltage	3.0[1]	5.0	5.5	4.5	5.0	5.5	V
V_I	Input voltage	0		V_{CC}	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	0		V_{CC}	V
$\Delta t/\Delta v$	Input transition rise or fall rate	0		10	0		10	ns/V
T_A	Operating free-air temperature	-40		+85	-40		+85	°C

NOTE:
1. No electrical or switching characteristics are specified at $V_{CC} < 3V$. Operation between 2V and 3V is not recommended, but within that range, a device output will maintain a previously established logic state.

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	TEST CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 to+7.0	V
I_{IK} or V_I	DC input diode current[2]	$V_I < 0$	-20	mA
		$V_I > V_{CC}$	20	
	DC input voltage		-0.5 to V_{CC} +0.5	V
I_{OK} or V_O	DC output diode current[2]	$V_O < 0$	-50	mA
		$V_O > V_{CC}$	50	
	DC output voltage		-0.5 to V_{CC} +0.5	V
I_O	DC output source or sink current per output pin	V_O = 0 to V_{CC}	±50	mA
I_{CC} or I_{GND}	DC V_{CC} current		±200	mA
	DC ground current		±200	
T_{STG}	Storage temperature		-65 to 150	°C
P_{TOT}	Power dissipation per package Plastic DIP	Above 70°C:derate linearly by 8mW/K	500	mW
	Power dissipation per package Plastic surface mount (SO)	Above 70°C:derate linearly by 6mW/K	400	mW

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		V_{CC}	74AC11208				74ACT11208				UNIT
					T_A = +25°C		T_A = -40°C to +85°C		T_A = +25°C		T_A = -40°C to +85°C		
				V	Min	Max	Min	Max	Min	Max	Min	Max	
V_{IH}	High-level input voltage			3.0	2.10		2.10						V
				4.5	3.15		3.15		2.0		2.0		
				5.5	3.85		3.85		2.0		2.0		
V_{IL}	Low-level input voltage			3.0		0.90		0.90					V
				4.5		1.35		1.35		0.8		0.8	
				5.5		1.65		1.65		0.8		0.8	
V_{OH}	High-level output voltage	V_I = V_{IL} or V_{IH}	I_{OH} = -50μA	3.0	2.9		2.9						V
				4.5	4.4		4.4		4.4		4.4		
				5.5	5.4		5.4		5.4		5.4		
			I_{OH} = -4mA	3.0	2.58		2.48						
			I_{OH} = -24mA	4.5	3.94		3.8		3.94		3.8		
				5.5	4.94		4.8		4.94		4.8		
			I_{OH} = -75mA[1]	5.5			3.85				3.85		
V_{OL}	Low-level output voltage	V_I = V_{IL} or V_{IH}	I_{OL} = 50μA	3.0		0.1		0.1					V
				4.5		0.1		0.1		0.1		0.1	
				5.5		0.1		0.1		0.1		0.1	
			I_{OL} = 12mA	3.0		0.36		0.44					
			I_{OL} = 24mA	4.5		0.36		0.44		0.36		0.44	
				5.5		0.36		0.44		0.36		0.44	
			I_{OL} = 75mA[1]	5.5				1.65				1.65	
I_I	Input leakage current	V_I = V_{CC} or GND		5.5		±0.1		±1.0		±0.1		±1.0	μA
I_{OZ}	3-State output off-state current	V_I = V_{IL} or V_{IH}, V_O = V_{CC} or GND		5.5		±0.5		±5.0		±0.5		±5.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC} or GND, I_O = 0		5.5		8.0		80		8.0		80	μA
ΔI_{CC}	Supply current, TTL inputs High[2]	One input at 3.4V, other inputs at V_{CC} or GND		5.5						0.9		1.0	mA

NOTES:
1. Not more than one output should be tested at a time, and the duration of the test should not exceed 10ms.
2. This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0V or V_{CC}.

74AC/ACT11238

3-to-8 Line Decoder/ Demultiplexer

Product Specification

FEATURES

- **Multiple input enable for easy expansion**
- **Ideal for memory chip select decoding**
- **Non-inverting outputs**
- **Output capability: ±24 mA**
- **CMOS (AC) and TTL (ACT) voltage level inputs**
- **50Ω incident wave switching**
- **Center-pin V_{CC} and ground configuration to minimize high-speed switching noise**
- **I_{CC} category: MSI**

DESCRIPTION

The 74AC/ACT11238 high-performance CMOS devices combine very high speed and high output drive comparable to the most advanced TTL families.

The 74AC/ACT11238 decoders accept three binary weighted inputs (A_0, A_1, A_2) and when enabled, provide eight mutually exclusive, active-High outputs (Y_0 - Y_7). The devices feature three enable inputs; two active-Low ($\overline{E}_1$, $\overline{E}_2$) and one active-High (E_3). Every output will be Low unless $\overline{E}_1$ and $\overline{E}_2$ are Low and E_3 is High. This multiple enable function allows easy parallel expansion of the devices to a 1-of-32 (5 lines to 32 lines) decoder with just four '11238's and one inverter.

The devices can be used as eight output demultiplexers by using one of the active-Low enable inputs as the data input and the remaining enable inputs as strobes.

GENERAL INFORMATION

SYMBOL	PARAMETER	CONDITIONS T_A = 25°C; GND = 0V; V_{CC} = 5.0V	TYPICAL		UNIT
			AC	ACT	
t_{PLH}/ t_{PHL}	Propagation delay A_n to Y_n	C_L = 50pF	5.9	5.4	ns
C_{PD}	Power dissipation capacitance[1]	f = 1MHz; C_L = 50pF	55	57	pF
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	3.5	3.5	pF
I_{LATCH}	Latch-up current	Per Jedec JC40.2 Standard 17	500	500	mA

Note:

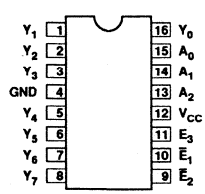
1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_I + \Sigma (C_L \times V_{CC}^2 \times f_O)$ where:
   f_I = input frequency in MHz, C_L = output load capacitance in pF,
   f_O = output frequency in MHz, V_{CC} = supply voltage in V,
   $\Sigma (C_L \times V_{CC}^2 \times f_O)$ = sum of outputs

ORDERING INFORMATION

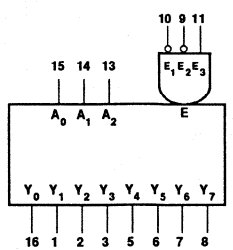
PACKAGES	TEMPERATURE RANGE	ORDER CODE
16-pin plastic DIP (300mil-wide)	-40°C to +85°C	74AC11238N 74ACT11238N
16-pin plastic SO (150mil-wide)	-40°C to +85°C	74AC11238D 74ACT11238D

PIN CONFIGURATION

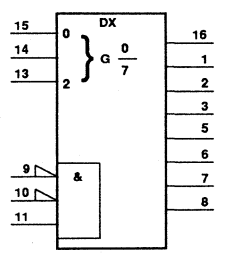
N and D Packages



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



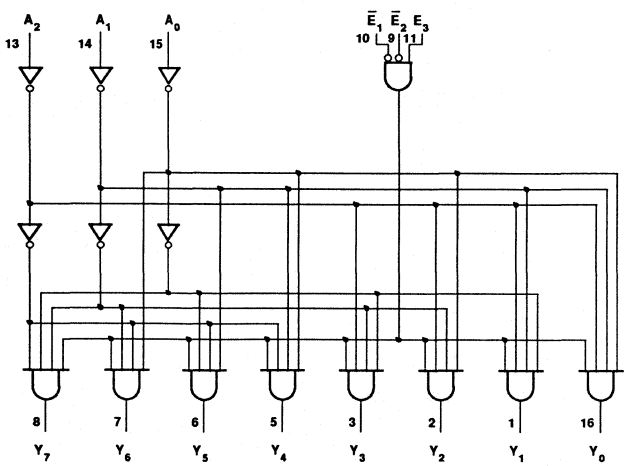
PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
15, 14, 13	A_0 to A_2	Address inputs
10, 9	$\overline{E}_1$, $\overline{E}_2$	Enable inputs (active Low)
11	E_3	Enable input (active High)
16, 8, 7, 6, 5, 3, 2, 1	Y_0 to Y_7	Outputs
4	GND	Ground (0V)
12	V_{CC}	Positive supply voltage

FUNCTION TABLE

INPUTS						OUTPUTS							
$\overline{E}_1$	$\overline{E}_2$	E_3	A_0	A_1	A_2	Y_0	Y_1	Y_2	Y_3	Y_4	Y_5	Y_6	Y_7
H	X	X	X	X	X	L	L	L	L	L	L	L	L
X	H	X	X	X	X	L	L	L	L	L	L	L	L
X	X	L	X	X	X	L	L	L	L	L	L	L	L
L	L	H	L	L	L	H	L	L	L	L	L	L	L
L	L	H	H	L	L	L	H	L	L	L	L	L	L
L	L	H	L	H	L	L	L	H	L	L	L	L	L
L	L	H	H	H	L	L	L	L	H	L	L	L	L
L	L	H	L	L	H	L	L	L	L	H	L	L	L
L	L	H	H	L	H	L	L	L	L	L	H	L	L
L	L	H	L	H	H	L	L	L	L	L	L	H	L
L	L	H	H	H	H	L	L	L	L	L	L	L	H

LOGIC DIAGRAM



RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	74AC11238			74ACT11238			UNIT
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	DC supply voltage	3.0[1]	5.0	5.5	4.5	5.0	5.5	V
V_I	Input voltage	0		V_{CC}	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	0		V_{CC}	V
$\Delta t/\Delta v$	Input transition rise or fall rate	0		10	0		10	ns/V
T_A	Operating free-air temperature	-40		+85	-40		+85	°C

NOTE:
1. No electrical or switching characteristics are specified at V_{CC} < 3V. Operation between 2V and 3V is not recommended, but within that range, a device output will maintain a previously established logic state.

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	TEST CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 to+7.0	V
I_{IK} or V_I	DC input diode current[2]	$V_I < 0$	-20	mA
		$V_I > V_{CC}$	20	
	DC input voltage		-0.5 to V_{CC} +0.5	V
I_{OK} or V_O	DC output diode current[2]	$V_O < 0$	-50	mA
		$V_O > V_{CC}$	50	
	DC output voltage		-0.5 to V_{CC} +0.5	V
I_O	DC output source or sink current per output pin	V_O = 0 to V_{CC}	±50	mA
I_{CC} or I_{GND}	DC V_{CC} current		±200	mA
	DC ground current		±200	
T_{STG}	Storage temperature		-65 to 150	°C
P_{TOT}	Power dissipation per package Plastic DIP	Above 70°C:derate linearly by 8mW/K	500	mW
	Power dissipation per package Plastic surface mount (SO)	Above 70°C:derate linearly by 6mW/K	400	mW

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		V_{CC}	74AC11238				74ACT11238				UNIT
					T_A = +25°C		T_A = -40°C to +85°C		T_A = +25°C		T_A = -40°C to +85°C		
				V	Min	Max	Min	Max	Min	Max	Min	Max	
V_{IH}	High-level input voltage			3.0	2.10		2.10						V
				4.5	3.15		3.15		2.0		2.0		
				5.5	3.85		3.85		2.0		2.0		
V_{IL}	Low-level input voltage			3.0		0.90		0.90					V
				4.5		1.35		1.35		0.8		0.8	
				5.5		1.65		1.65		0.8		0.8	
V_{OH}	High-level output voltage	V_I = V_{IL} or V_{IH}	I_{OH} = -50μA	3.0	2.9		2.9						V
				4.5	4.4		4.4		4.4		4.4		
				5.5	5.4		5.4		5.4		5.4		
			I_{OH} = -4mA	3.0	2.58		2.48						
			I_{OH} = -24mA	4.5	3.94		3.8		3.94		3.8		
				5.5	4.94		4.8		4.94		4.8		
			I_{OH} = -75mA[1]	5.5			3.85				3.85		
V_{OL}	Low-level output voltage	V_I = V_{IL} or V_{IH}	I_{OL} = 50μA	3.0		0.1		0.1					V
				4.5		0.1		0.1		0.1		0.1	
				5.5		0.1		0.1		0.1		0.1	
			I_{OL} = 12mA	3.0		0.36		0.44					
			I_{OL} = 24mA	4.5		0.36		0.44		0.36		0.44	
				5.5		0.36		0.44		0.36		0.44	
			I_{OL} = 75mA[1]	5.5				1.65				1.65	
I_I	Input leakage current	V_I = V_{CC} or GND		5.5		±0.1		±1.0		±0.1		±1.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC} or GND, I_O = 0		5.5		8.0		80		8.0		80	μA
ΔI_{CC}	Supply current, TTL inputs High[2]	One input at 3.4V, other inputs at V_{CC} or GND		5.5						0.9		1.0	mA

NOTES:
1. Not more than one output should be tested at a time, and the duration of the test should not exceed 10ms.
2. This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0V or V_{CC}.

AC ELECTRICAL CHARACTERISTICS AT 3.3V ±0.3V

SYMBOL	PARAMETER	WAVEFORM	74AC11238					UNIT
			T_A = +25°C			T_A = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay A_n to Y_n	1	1.5 1.5	8.5 9.6	10.6 11.9	1.5 1.5	11.7 13.3	ns
t_{PLH} t_{PHL}	Propagation delay E_3 to Y_n	2	1.5 1.5	8.2 9.6	10.3 11.7	1.5 1.5	11.4 13.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{E}_n$ to Y_n	2	1.5 1.5	9.1 10.7	11.2 12.9	1.5 1.5	12.5 14.5	ns

AC ELECTRICAL CHARACTERISTICS AT 5.0V ±0.5V

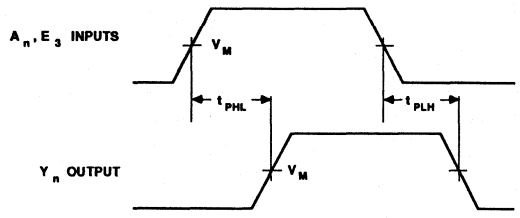
SYMBOL	PARAMETER	WAVEFORM	74AC11238					UNIT
			T_A = +25°C			T_A = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay A_n to Y_n	1	1.5 1.5	5.4 6.3	7.0 8.2	1.5 1.5	8.2 9.7	ns
t_{PLH} t_{PHL}	Propagation delay E_3 to Y_n	2	1.5 1.5	5.2 6.5	6.7 8.2	1.5 1.5	7.9 9.6	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{E}_n$ to Y_n	2	1.5 1.5	5.6 7.2	7.1 8.9	1.5 1.5	8.5 9.6	ns

AC ELECTRICAL CHARACTERISTICS AT 5.0V ±0.5V

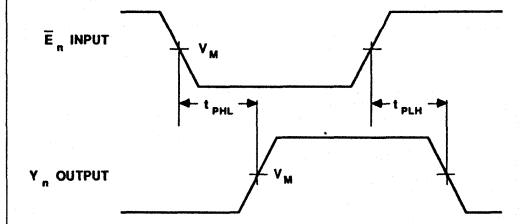
SYMBOL	PARAMETER	WAVEFORM	74ACT11238					UNIT
			T_A = +25°C			T_A = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay A_n to Y_n	1	1.5 1.5	5.0 5.7	8.6 9.7	1.5 1.5	9.6 10.8	ns
t_{PLH} t_{PHL}	Propagation delay E_3 to Y_n	2	1.5 1.5	6.0 6.9	8.4 10.2	1.5 1.5	9.4 11.4	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{E}_n$ to Y_n	2	1.5 1.5	5.9 7.8	9.0 10.7	1.5 1.5	10.1 12.1	ns

AC WAVEFORMS

AC : V_M = 50% V_{CC}, V_{IN} = GND to V_{CC}. ACT : V_M = 1.5V, V_{IN} = GND to 3.0V



Waveform 1. Waveforms Showing the Inputs (A_n, E_3) to Output (Y_n) Propagation Delays

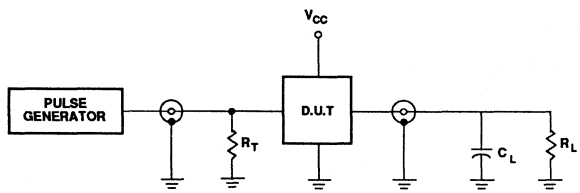


Waveform 2. Waveforms Showing the Input ($\overline{E}_n$) to Output (Y_n) Propagation Delays

WAVEFORM CONDITIONS

	INPUTS	OUTPUTS
AC	V_{IN} = GND to V_{CC}, V_M = 50% V_{CC}	V_{OUT} = V_{OL} to V_{OH}
ACT	V_{IN} = GND to 3.0V, V_M = 1.5V	V_M = 50% V_{CC}

TEST CIRCUIT



Test Circuit

DEFINITIONS

C_L = Load capacitance, 50pF; includes jig and probe capacitance

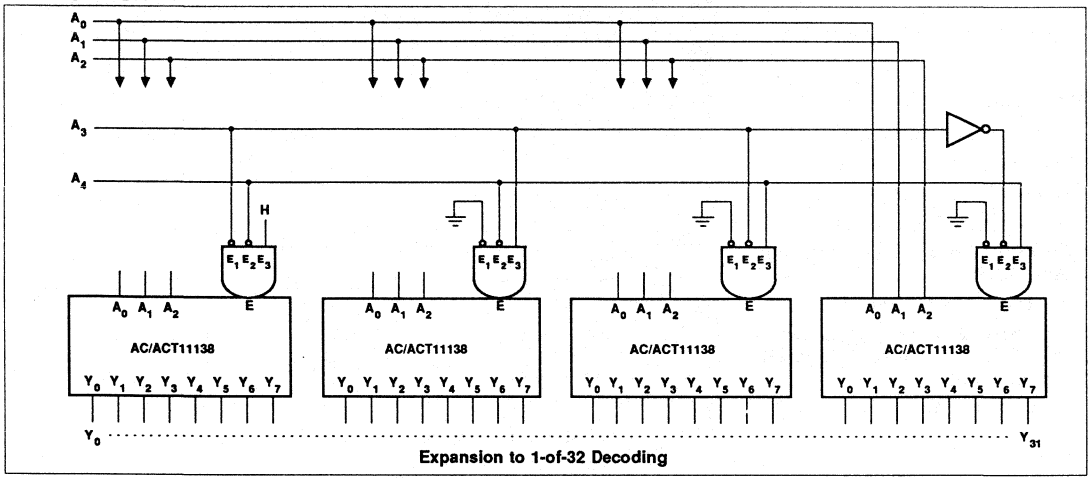
R_L = Load resistor, 500Ω

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators

Input pulses: PRR ≤ 10MHz

$t_r = t_f$ = 3ns

APPLICATION



Expansion to 1-of-32 Decoding

74AC/ACT11239

Dual 2-to-4 Line Decoder/ Demultiplexer; Active-High

AC11239: Product Specification
ACT11239: Objective Specification

FEATURES

- **Demultiplexing capability**
- **Two independent 1-of-4 decoders**
- **Non-inverting outputs**
- **Output capability: ±24 mA**
- **CMOS (AC) and TTL (ACT) voltage level inputs**
- **50Ω incident wave switching**
- **Center-pin V_{CC} and ground configuration to minimize high-speed switching noise**
- **I_{CC} category: MSI**

DESCRIPTION

The 74AC/ACT11239 high-performance CMOS devices combine very high speed and high output drive comparable to the most advanced TTL families.

The 74AC/ACT11239 has two independent decoders, each accepting two binary weighted inputs (nA_0, nA_1) and providing four mutually exclusive active-High outputs (nY_0 - nY_3). Each decoder has an active-Low Enable ($n\overline{E}$). When $\overline{E}$ is High, every output is forced Low. The Enable can be used as the Data input for a 1-of-4 demultiplexer application.

GENERAL INFORMATION

SYMBOL	PARAMETER	CONDITIONS T_A = 25°C; GND = 0V; V_{CC} = 5.0V	TYPICAL		UNIT
			AC	ACT	
t_{PLH}/ t_{PHL}	Propagation delay nA_n to nY_n	C_L = 50pF	3.9	6.0	ns
C_{PD}	Power dissipation capacitance per decoder[1]	f = 1MHz; C_L = 50pF	48	57	pF
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	3.5	3.5	pF
I_{LATCH}	Latch-up current	Per Jedec JC40.2 Standard 17	500	500	mA

Note:

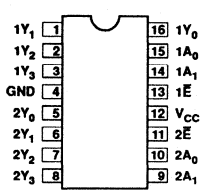
1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_I + \Sigma (C_L \times V_{CC}^2 \times f_O)$ where:
   f_I = input frequency in MHz, C_L = output load capacitance in pF,
   f_O = output frequency in MHz, V_{CC} = supply voltage in V,
   $\Sigma (C_L \times V_{CC}^2 \times f_O)$ = sum of outputs

ORDERING INFORMATION

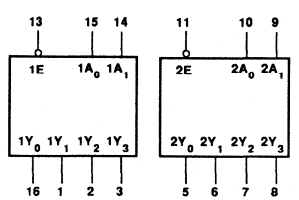
PACKAGES	TEMPERATURE RANGE	ORDER CODE
16-pin plastic DIP (300mil-wide)	-40°C to +85°C	74AC11239N 74ACT11239N
16-pin plastic SO (150mil-wide)	-40°C to +85°C	74AC11239D 74ACT11239D

PIN CONFIGURATION

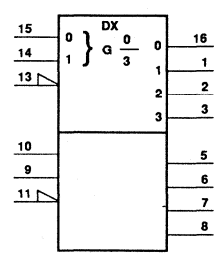
N and D Packages



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



Dual 2-to-4 Line Decoder/Demultiplexer; Active-High

74AC/ACT11239

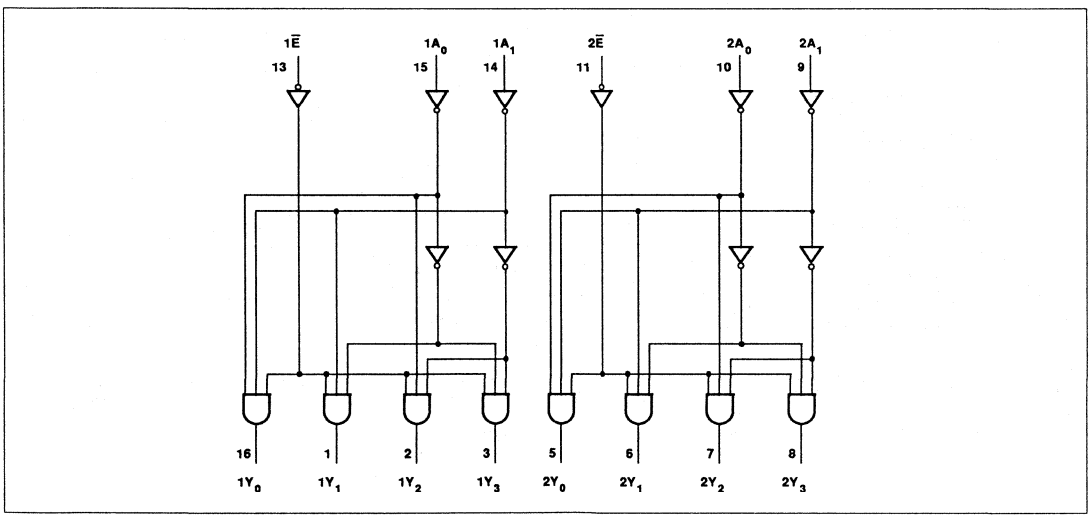
PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
15, 14	$1A_0$, $1A_1$	Address inputs, decoder 1
13	$1\overline{E}$	Enable input (active Low), decoder 1
16, 1, 2, 3	$1Y_0$ to $1Y_3$	Outputs, decoder 1
10, 9	$2A_0$, $2A_1$	Address inputs, decoder 2
11	$2\overline{E}$	Enable input (active Low), decoder 2
5, 6, 7, 8	$2Y_0$ to $2Y_3$	Outputs, decoder 2
4	GND	Ground (0V)
12	V_{CC}	Positive supply voltage

FUNCTION TABLE

INPUTS			OUTPUTS			
$\overline{E}$	A_0	A_1	Y_0	Y_1	Y_2	Y_3
H	X	X	L	L	L	L
L	L	L	H	L	L	L
L	H	L	L	H	L	L
L	L	H	L	L	H	L
L	H	H	L	L	L	H

LOGIC DIAGRAM



RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	74AC11239			74ACT11239			UNIT
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	DC supply voltage	3.0[1]	5.0	5.5	4.5	5.0	5.5	V
V_I	Input voltage	0		V_{CC}	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	0		V_{CC}	V
$\Delta t/\Delta v$	Input transition rise or fall rate	0		10	0		10	ns/V
T_A	Operating free-air temperature	-40		+85	-40		+85	°C

NOTE:

1. No electrical or switching characteristics are specified at V_{CC} < 3V. Operation between 2V and 3V is not recommended, but within that range, a device output will maintain a previously established logic state.

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	TEST CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 to+7.0	V
I_{IK} or V_I	DC input diode current[2]	$V_I < 0$	-20	mA
		$V_I > V_{CC}$	20	
	DC input voltage		-0.5 to V_{CC} +0.5	V
I_{OK} or V_O	DC output diode current[2]	$V_O < 0$	-50	mA
		$V_O > V_{CC}$	50	
	DC output voltage		-0.5 to V_{CC} +0.5	V
I_O	DC output source or sink current per output pin	V_O = 0 to V_{CC}	±50	mA
I_{CC} or I_{GND}	DC V_{CC} current		±200	mA
	DC ground current		±200	
T_{STG}	Storage temperature		-65 to 150	°C
P_{TOT}	Power dissipation per package Plastic DIP	Above 70°C:derate linearly by 8mW/K	500	mW
	Power dissipation per package Plastic surface mount (SO)	Above 70°C:derate linearly by 6mW/K	400	mW

NOTES:

1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

Dual 2-to-4 Line Decoder/Demultiplexer; Active-High

74AC/ACT11239

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		V_{CC}	74AC11239				74ACT11239				UNIT
					T_A = +25°C		T_A = -40°C to +85°C		T_A = +25°C		T_A = -40°C to +85°C		
				V	Min	Max	Min	Max	Min	Max	Min	Max	
V_{IH}	High-level input voltage			3.0	2.10		2.10						V
				4.5	3.15		3.15		2.0		2.0		
				5.5	3.85		3.85		2.0		2.0		
V_{IL}	Low-level input voltage			3.0		0.90		0.90					V
				4.5		1.35		1.35		0.8		0.8	
				5.5		1.65		1.65		0.8		0.8	
V_{OH}	High-level output voltage	V_I = V_{IL} or V_{IH}	I_{OH} = -50μA	3.0	2.9		2.9						V
				4.5	4.4		4.4		4.4		4.4		
				5.5	5.4		5.4		5.4		5.4		
			I_{OH} = -4mA	3.0	2.58		2.48						
			I_{OH} = -24mA	4.5	3.94		3.8		3.94		3.8		
				5.5	4.94		4.8		4.94		4.8		
			I_{OH} = -75mA[1]	5.5			3.85				3.85		
V_{OL}	Low-level output voltage	V_I = V_{IL} or V_{IH}	I_{OL} = 50μA	3.0		0.1		0.1					V
				4.5		0.1		0.1		0.1		0.1	
				5.5		0.1		0.1		0.1		0.1	
			I_{OL} = 12mA	3.0		0.36		0.44					
			I_{OL} = 24mA	4.5		0.36		0.44		0.36		0.44	
				5.5		0.36		0.44		0.36		0.44	
			I_{OL} = 75mA[1]	5.5				1.65				1.65	
I_I	Input leakage current	V_I = V_{CC} or GND		5.5		±0.1		±1.0		±0.1		±1.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC} or GND, I_O = 0		5.5		8.0		80		8.0		80	μA
ΔI_{CC}	Supply current, TTL inputs High[2]	One input at 3.4V, other inputs at V_{CC} or GND		5.5						0.9		1.0	mA

NOTES:
1. Not more than one output should be tested at a time, and the duration of the test should not exceed 10ms.
2. This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0V or V_{CC}.

Dual 2-to-4 Line Decoder/Demultiplexer; Active-High

74AC/ACT11239

AC ELECTRICAL CHARACTERISTICS AT 3.3V ±0.3V

SYMBOL	PARAMETER	WAVEFORM	74AC11239					UNIT
			T_A = +25°C			T_A = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay nA_n to nY_n	1 and 2	1.5 1.5	6.2 5.6	8.5 8.0	1.5 1.5	9.5 9.0	ns
t_{PLH} t_{PHL}	Propagation delay $n\overline{E}$ to nY_n	2	1.5 1.5	5.4 5.7	7.1 7.3	1.5 1.5	7.9 8.1	ns

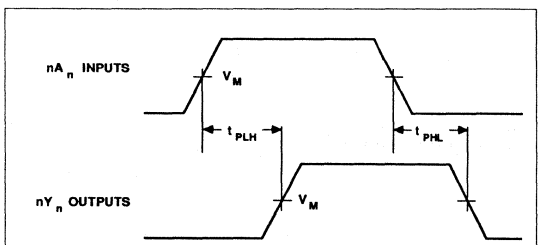
AC ELECTRICAL CHARACTERISTICS AT 5.0V ±0.5V

SYMBOL	PARAMETER	WAVEFORM	74AC11239					UNIT
			T_A = +25°C			T_A = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay nA_n to nY_n	1 and 2	1.5 1.5	4.0 3.7	6.1 6.1	1.5 1.5	6.7 6.8	ns
t_{PLH} t_{PHL}	Propagation delay $n\overline{E}$ to nY_n	2	1.5 1.5	3.5 3.9	5.3 5.6	1.5 1.5	5.8 6.2	ns

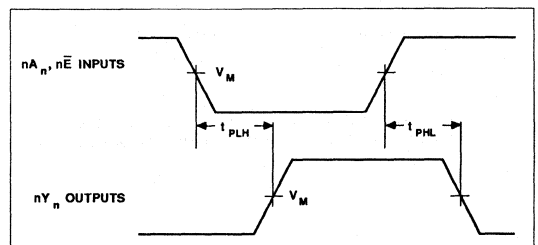
AC ELECTRICAL CHARACTERISTICS AT 5.0V ±0.5V

SYMBOL	PARAMETER	WAVEFORM	74ACT11239					UNIT
			T_A = +25°C			T_A = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay nA_n to nY_n	1 and 2	1.5 1.5			1.5 1.5		ns
t_{PLH} t_{PHL}	Propagation delay $n\overline{E}$ to nY_n	2	1.5 1.5			1.5 1.5		ns

AC WAVEFORMS



Waveform 1. Waveforms Showing the Inputs (nA_n) to Output (nY_n) Propagation Delays



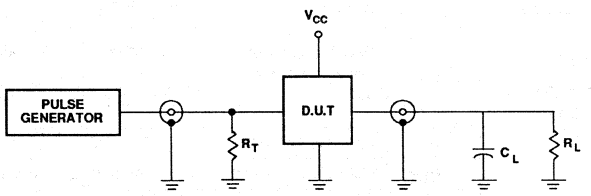
Waveform 2. Waveforms Showing the Inputs (nA_n, $n\overline{E}$) to Output (nY_n) Propagation Delays

Dual 2-to-4 Line Decoder/Demultiplexer; Active-High

WAVEFORM CONDITIONS

	INPUTS	OUTPUTS
AC	V_{IN} = GND to V_{CC}, V_M = 50% V_{CC}	V_{OUT} = V_{OL} to V_{OH}
ACT	V_{IN} = GND to 3.0V, V_M = 1.5V	V_M = 50% V_{CC}

TEST CIRCUIT



Test Circuit

DEFINITIONS

C_L = Load capacitance, 50pF; includes jig and probe capacitance

R_L = Load resistor, 500Ω

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators

Input pulses: PRR ≤ 10MHz

$t_r = t_f$ = 3ns

74AC/ACT11240

Octal Buffer/Line Driver; 3-State; INV

Product Specification

FEATURES

- **Octal bus interface**
- **3-State buffers**
- **Output capability: ±24 mA**
- **CMOS (AC) and TTL (ACT) voltage level inputs**
- **50Ω incident wave switching**
- **Center-pin V_{CC} and ground configuration to minimize high-speed switching noise**
- **I_{CC} category: MSI**

DESCRIPTION

The 74AC/ACT11240 high-performance CMOS devices combine very high speed and high output drive comparable to the most advanced TTL families.

The 74AC/ACT11240 device is an octal buffer that is ideal for driving bus lines or buffer memory address registers. The device features two Output Enables ($\overline{OE}$), each controlling four of the 3-State outputs.

GENERAL INFORMATION

SYMBOL	PARAMETER	CONDITIONS T_A = 25°C; GND = 0V; V_{CC} = 5.0V		TYPICAL AC	TYPICAL ACT	UNIT
t_{PLH}/t_{PHL}	Propagation delay A_n to $\overline{Y}_n$	C_L = 50pF		5.0	6.3	ns
C_{PD}	Power dissipation capacitance per buffer[1]	f = 1MHz;	Enabled	39	47	pF
		C_L = 50pF	Disabled	12	13	pF
C_{IN}	Input capacitance	V_I = 0V or V_{CC}		4.0	4.0	pF
C_{OUT}	Output capacitance	V_I = 0V or V_{CC}; Disabled		10	10	pF
I_{LATCH}	Latch-up current	Per Jedec JC40.2 Standard 17		500	500	mA

Note:

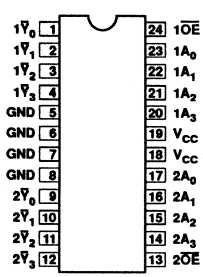
1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_I + \Sigma (C_L \times V_{CC}^2 \times f_O)$ where:
   f_I = input frequency in MHz, C_L = output load capacitance in pF,
   f_O = output frequency in MHz, V_{CC} = supply voltage in V,
   $\Sigma (C_L \times V_{CC}^2 \times f_O)$ = sum of outputs

ORDERING INFORMATION

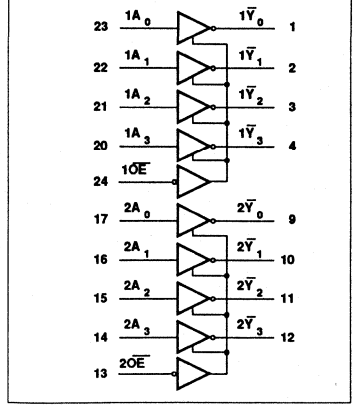
PACKAGES	TEMPERATURE RANGE	ORDER CODE
24-pin plastic DIP (300mil-wide)	-40°C to +85°C	74AC11240N 74ACT11240N
24-pin plastic SO (300mil-wide)	-40°C to +85°C	74AC11240D 74ACT11240D

PIN CONFIGURATION

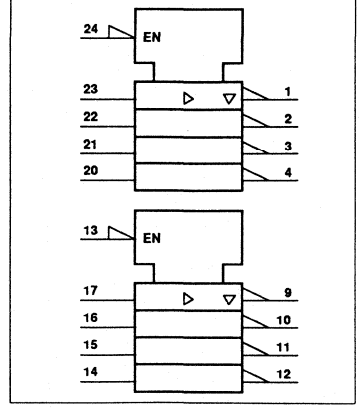
N and D Packages



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
23, 22, 21, 20	$1A_0$ - $1A_3$	Data inputs
17, 16, 15, 14	$2A_0$ - $2A_3$	Data inputs
1, 2, 3, 4	$1\overline{Y}_0$ - $1\overline{Y}_3$	Data outputs
9, 10, 11, 12	$2\overline{Y}_0$ - $2\overline{Y}_3$	Data outputs
24, 13	$1\overline{OE}$, $2\overline{OE}$	Output enables
5, 6, 7, 8	GND	Ground (0V)
18, 19	V_{CC}	Positive supply voltage

FUNCTION TABLE

INPUTS				OUTPUT	
$1\overline{OE}$	$1A_n$	$2\overline{OE}$	$2A_n$	$1\overline{Y}_n$	$2\overline{Y}_n$
L	L	L	L	H	H
L	H	L	H	L	L
H	X	H	X	Z	Z

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		74AC11240			74ACT11240			UNIT
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	DC supply voltage		3.0[1]	5.0	5.5	4.5	5.0	5.5	V
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
$\Delta t/\Delta v$	Input transition rise or fall rate	Data	0		10	0		10	ns/V
		Output enable	0		5	0		10	
T_A	Operating free-air temperature		-40		+85	-40		+85	°C

NOTE:

1. No electrical or switching characteristics are specified at V_{CC} < 3V. Operation between 2V and 3V is not recommended, but within that range, a device output will maintain a previously established logic state.

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	TEST CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 to+7.0	V
I_{IK} or V_I	DC input diode current[2]	V_I < 0	-20	mA
		V_I > V_{CC}	20	
	DC input voltage		-0.5 to V_{CC} +0.5	V
I_{OK} or V_O	DC output diode current[2]	V_O < 0	-50	mA
		V_O > V_{CC}	50	
	DC output voltage		-0.5 to V_{CC} +0.5	V
I_O	DC output source or sink current per output pin	V_O = 0 to V_{CC}	±50	mA
I_{CC} or I_{GND}	DC V_{CC} current		±200	mA
	DC ground current		±200	
T_{STG}	Storage temperature		-65 to 150	°C
P_{TOT}	Power dissipation per package Plastic DIP	Above 70°C:derate linearly by 8mW/K	500	mW
	Power dissipation per package Plastic surface mount (SO)	Above 70°C:derate linearly by 6mW/K	400	mW

NOTES:

1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		V_{CC}	74AC11240				74ACT11240				UNIT
					T_A = +25°C		T_A = -40°C to +85°C		T_A = +25°C		T_A = -40°C to +85°C		
				V	Min	Max	Min	Max	Min	Max	Min	Max	
V_{IH}	High-level input voltage			3.0	2.10		2.10						V
				4.5	3.15		3.15		2.0		2.0		
				5.5	3.85		3.85		2.0		2.0		
V_{IL}	Low-level input voltage			3.0		0.90		0.90					V
				4.5		1.35		1.35		0.8		0.8	
				5.5		1.65		1.65		0.8		0.8	
V_{OH}	High-level output voltage	V_I = V_{IL} or V_{IH}	I_{OH} = -50μA	3.0	2.9		2.9						V
				4.5	4.4		4.4		4.4		4.4		
				5.5	5.4		5.4		5.4		5.4		
			I_{OH} = -4mA	3.0	2.58		2.48						
			I_{OH} = -24mA	4.5	3.94		3.8		3.94		3.8		
				5.5	4.94		4.8		4.94		4.8		
			I_{OH} = -75mA[1]	5.5			3.85				3.85		
V_{OL}	Low-level output voltage	V_I = V_{IL} or V_{IH}	I_{OL} = 50μA	3.0		0.1		0.1					V
				4.5		0.1		0.1		0.1		0.1	
				5.5		0.1		0.1		0.1		0.1	
			I_{OL} = 12mA	3.0		0.36		0.44					
			I_{OL} = 24mA	4.5		0.36		0.44		0.36		0.44	
				5.5		0.36		0.44		0.36		0.44	
			I_{OL} = 75mA[1]	5.5				1.65				1.65	
I_I	Input leakage current	V_I = V_{CC} or GND		5.5		±0.1		±1.0		±0.1		±1.0	μA
I_{OZ}	3-State output off-state current	V_I = V_{IL} or V_{IH}; V_O = V_{CC} or GND		5.5		±0.5		±5.0		±0.5		±5.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC} or GND, I_O = 0		5.5		8.0		80		8.0		80	μA
ΔI_{CC}	Supply current, TTL inputs High[2]	One input at 3.4V, other inputs at V_{CC} or GND		5.5						0.9		1.0	mA

NOTES:
1. Not more than one output should be tested at a time, and the duration of the test should not exceed 10ms.
2. This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0V or V_{CC}.

AC ELECTRICAL CHARACTERISTICS AT 3.3V ±0.3V

SYMBOL	PARAMETER	WAVEFORM	74AC11240					UNIT
			T_A = +25°C			T_A = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay A_n to $\overline{Y}_n$	1	1.5 1.5	7.6 6.3	10.5 8.6	1.5 1.5	11.7 9.5	ns
t_{PZH} t_{PZL}	Output enable time to High and Low Level	2	1.5 1.5	8.2 7.6	11.6 10.8	1.5 1.5	12.7 12.0	ns
t_{PHZ} t_{PLZ}	Output disable time from High and Low Level	2	1.5 1.5	5.5 6.7	7.5 9.4	1.5 1.5	7.8 9.8	ns

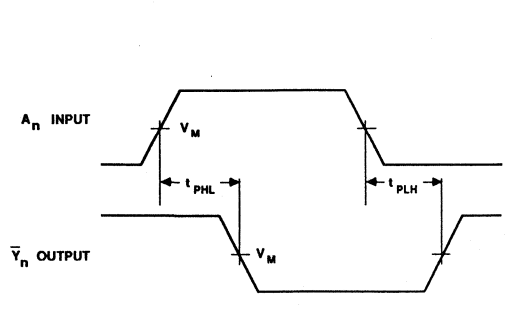
AC ELECTRICAL CHARACTERISTICS AT 5.0V ±0.5V

SYMBOL	PARAMETER	WAVEFORM	74AC11240					UNIT
			T_A = +25°C			T_A = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay A_n to $\overline{Y}_n$	1	1.5 1.5	5.4 4.6	7.5 6.6	1.5 1.5	8.4 7.2	ns
t_{PZH} t_{PZL}	Output enable time to High and Low Level	2	1.5 1.5	5.7 5.3	8.2 7.7	1.5 1.5	9.2 8.7	ns
t_{PHZ} t_{PLZ}	Output disable time from High and Low Level	2	1.5 1.5	4.7 5.2	6.3 7.3	1.5 1.5	6.6 7.7	ns

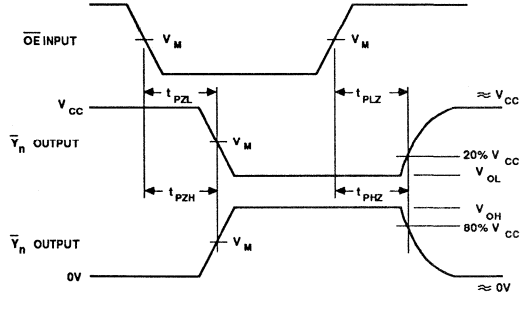
AC ELECTRICAL CHARACTERISTICS AT 5.0V ±0.5V

SYMBOL	PARAMETER	WAVEFORM	74ACT11240					UNIT
			T_A = +25°C			T_A = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay A_n to $\overline{Y}_n$	1	1.5 1.5	6.5 6.0	9.9 8.0	1.5 1.5	10.6 8.7	ns
t_{PZH} t_{PZL}	Output enable time to High and Low Level	2	1.5 1.5	7.5 7.3	11.7 11.5	1.5 1.5	12.5 12.3	ns
t_{PHZ} t_{PLZ}	Output disable time from High and Low Level	2	1.5 1.5	7.3 7.9	9.4 10.3	1.5 1.5	10.0 10.8	ns

AC WAVEFORMS



Waveform 1. Waveforms Showing the Input (A_n) to Output ($\overline{Y}_n$) Propagation Delays

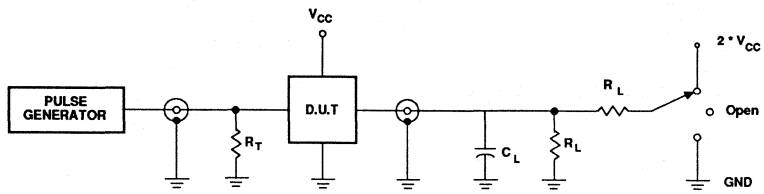


Waveform 2. Waveforms Showing the 3-State Output Enable and Disable Times

WAVEFORM CONDITIONS

	INPUTS	OUTPUTS
AC	V_{IN} = GND to V_{CC}, V_M = 50% V_{CC}	$V_{OUT} = V_{OL}$ to V_{OH}
ACT	V_{IN} = GND to 3.0V, V_M = 1.5V	V_M = 50% V_{CC}

TEST CIRCUIT



Test Circuit

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2*VCC
t_{PHZ}/t_{PZH}	GND

SWITCH POSITION

DEFINITIONS

C_L = Load capacitance, 50pF; includes jig and probe capacitance

R_L = Load resistor, 500Ω

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators

Input pulses: PRR ≤ 10MHz

$t_r = t_f$ = 3ns

74AC/ACT11241

Octal Buffer/Line Driver; 3-State

Product Specification

FEATURES

- **Octal bus interface**
- **3-State buffers**
- **Output capability: ±24 mA**
- **CMOS (AC) and TTL (ACT) voltage level inputs**
- **50Ω incident wave switching**
- **Center-pin V_{CC} and ground configuration to minimize high-speed switching noise**
- **I_{CC} category: MSI**

DESCRIPTION

The 74AC/ACT11241 high-performance CMOS devices combine very high speed and high output drive comparable to the most advanced TTL families.

The 74AC/ACT11241 device is an octal buffer that is ideal for driving bus lines or buffer memory address registers. The device features two Output Enables ($1\overline{OE}$ and 2OE), each controlling four of the 3-State outputs.

GENERAL INFORMATION

SYMBOL	PARAMETER	CONDITIONS T_A = 25°C; GND = 0V; V_{CC} = 5.0V		TYPICAL AC	TYPICAL ACT	UNIT
t_{PLH}/t_{PHL}	Propagation delay A_n to Y_n	C_L = 50pF		4.7	6.5	ns
C_{PD}	Power dissipation capacitance per buffer[1]	f = 1MHz; C_L = 50pF	Enabled	26	27	pF
			Disabled	10	9	
C_{IN}	Input capacitance	V_I = 0V or V_{CC}		4.0	4.0	pF
C_{OUT}	Output capacitance	V_I = 0V or V_{CC}; Disabled		10	10	pF
I_{LATCH}	Latch-up current	Per Jedec JC40.2 Standard 17		500	500	mA

Note:

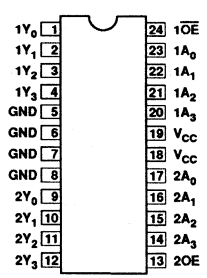
1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_I + \Sigma (C_L \times V_{CC}^2 \times f_O)$ where:
   f_I = input frequency in MHz, C_L = output load capacitance in pF,
   f_O = output frequency in MHz, V_{CC} = supply voltage in V,
   $\Sigma (C_L \times V_{CC}^2 \times f_O)$ = sum of outputs

ORDERING INFORMATION

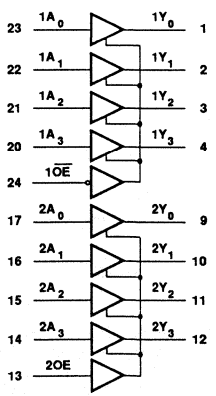
PACKAGES	TEMPERATURE RANGE	ORDER CODE
24-pin plastic DIP (300mil-wide)	-40°C to +85°C	74AC11241N 74ACT11241N
24-pin plastic SO (300mil-wide)	-40°C to +85°C	74AC11241D 74ACT11241D

PIN CONFIGURATION

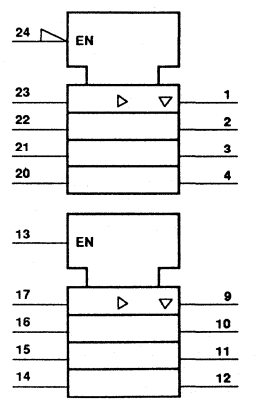
N and D Packages



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
23, 22, 21, 20	$1A_0$ - $1A_3$	Data inputs
17, 16, 15, 14	$2A_0$ - $2A_3$	Data inputs
1, 2, 3, 4	$1Y_0$ - $1Y_3$	Data outputs
9, 10, 11, 12	$2Y_0$ - $2Y_3$	Data outputs
24, 13	$1\overline{OE}$, 2OE	Output enables
5, 6, 7, 8	GND	Ground (0V)
18, 19	V_{CC}	Positive supply voltage

FUNCTION TABLE

INPUTS				OUTPUT	
$1\overline{OE}$	$1A_n$	2OE	$2A_n$	$1Y_n$	$2Y_n$
L	L	H	L	L	L
L	H	H	H	H	H
H	X	L	X	Z	Z

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		74AC11241			74ACT11241			UNIT
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	DC supply voltage		3.0[1]	5.0	5.5	4.5	5.0	5.5	V
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
$\Delta t/\Delta v$	Input transition rise or fall rate	Data	0		10	0		10	ns/V
		Output enable	0		5	0		10	
T_A	Operating free-air temperature		-40		+85	-40		+85	°C

NOTE:

1. No electrical or switching characteristics are specified at $V_{CC} < 3V$. Operation between 2V and 3V is not recommended, but within that range, a device output will maintain a previously established logic state.

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	TEST CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 to+7.0	V
I_{IK} or V_I	DC input diode current[2]	$V_I < 0$	-20	mA
		$V_I > V_{CC}$	20	
	DC input voltage		-0.5 to V_{CC} +0.5	V
I_{OK} or V_O	DC output diode current[2]	$V_O < 0$	-50	mA
		$V_O > V_{CC}$	50	
	DC output voltage		-0.5 to V_{CC} +0.5	V
I_O	DC output source or sink current per output pin	V_O = 0 to V_{CC}	±50	mA
I_{CC} or I_{GND}	DC V_{CC} current		±200	mA
	DC ground current		±200	
T_{STG}	Storage temperature		-65 to 150	°C
P_{TOT}	Power dissipation per package Plastic DIP	Above 70°C:derate linearly by 8mW/K	500	mW
	Power dissipation per package Plastic surface mount (SO)	Above 70°C:derate linearly by 6mW/K	400	mW

NOTES:

1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		V_{CC}	74AC11241				74ACT11241				UNIT
					T_A = +25°C		T_A = -40°C to +85°C		T_A = +25°C		T_A = -40°C to +85°C		
				V	Min	Max	Min	Max	Min	Max	Min	Max	
V_{IH}	High-level input voltage			3.0	2.10		2.10						V
				4.5	3.15		3.15		2.0		2.0		
				5.5	3.85		3.85		2.0		2.0		
V_{IL}	Low-level input voltage			3.0		0.90		0.90					V
				4.5		1.35		1.35		0.8		0.8	
				5.5		1.65		1.65		0.8		0.8	
V_{OH}	High-level output voltage	V_I = V_{IL} or V_{IH}	I_{OH} = -50μA	3.0	2.9		2.9						V
				4.5	4.4		4.4		4.4		4.4		
				5.5	5.4		5.4		5.4		5.4		
			I_{OH} = -4mA	3.0	2.58		2.48						
			I_{OH} = -24mA	4.5	3.94		3.8		3.94		3.8		
				5.5	4.94		4.8		4.94		4.8		
			I_{OH} = -75mA[1]	5.5			3.85				3.85		
V_{OL}	Low-level output voltage	V_I = V_{IL} or V_{IH}	I_{OL} = 50μA	3.0		0.1		0.1					V
				4.5		0.1		0.1		0.1		0.1	
				5.5		0.1		0.1		0.1		0.1	
			I_{OL} = 12mA	3.0		0.36		0.44					
			I_{OL} = 24mA	4.5		0.36		0.44		0.36		0.44	
				5.5		0.36		0.44		0.36		0.44	
			I_{OL} = 75mA[1]	5.5				1.65				1.65	
I_I	Input leakage current	V_I = V_{CC} or GND		5.5		±0.1		±1.0		±0.1		±1.0	μA
I_{OZ}	3-State output off-state current	V_I = V_{IL} or V_{IH}, V_O = V_{CC} or GND		5.5		±0.5		±5.0		±0.5		±5.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC} or GND, I_O = 0		5.5		8.0		80		8.0		80	μA
ΔI_{CC}	Supply current, TTL inputs High[2]	One input at 3.4V, other inputs at V_{CC} or GND		5.5						0.9		1.0	mA

NOTES:
1. Not more than one output should be tested at a time, and the duration of the test should not exceed 10ms.
2. This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0V or V_{CC}.

AC ELECTRICAL CHARACTERISTICS AT 3.3V ±0.3V

SYMBOL	PARAMETER	WAVEFORM	74AC11241					UNIT
			T_A = +25°C			T_A = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay A_n to Y_n	1	1.5 1.5	7.0 6.2	10.0 8.4	1.5 1.5	11.4 9.2	ns
t_{PZH} t_{PZL}	Output enable time to High and Low level	2	1.5 1.5	7.8 7.7	11.4 10.6	1.5 1.5	12.9 11.7	ns
t_{PHZ} t_{PLZ}	Output disable time from High and Low level	2	1.5 1.5	5.8 7.1	7.6 9.3	1.5 1.5	7.9 9.9	ns

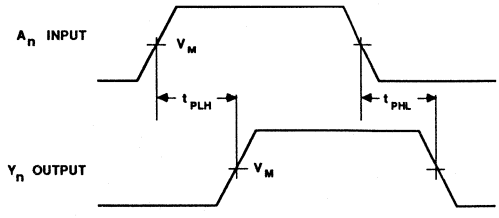
AC ELECTRICAL CHARACTERISTICS AT 5.0V ±0.5V

SYMBOL	PARAMETER	WAVEFORM	74AC11241					UNIT
			T_A = +25°C			T_A = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay A_n to Y_n	1	1.5 1.5	4.9 4.5	7.1 6.3	1.5 1.5	8.0 6.8	ns
t_{PZH} t_{PZL}	Output enable time to High and Low level	2	1.5 1.5	5.4 5.3	8.0 7.6	1.5 1.5	9.0 8.4	ns
t_{PHZ} t_{PLZ}	Output disable time from High and Low level	2	1.5 1.5	4.9 5.6	6.6 7.5	1.5 1.5	6.9 8.0	ns

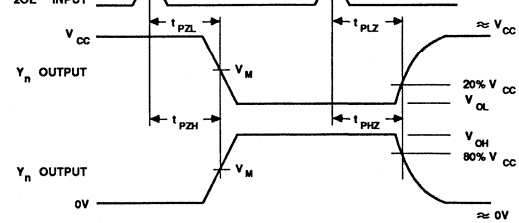
AC ELECTRICAL CHARACTERISTICS AT 5.0V ±0.5V

SYMBOL	PARAMETER	WAVEFORM	74ACT11241					UNIT
			T_A = +25°C			T_A = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay A_n to Y_n	1	1.5 1.5	6.6 6.3	9.0 8.5	1.5 1.5	10.0 9.1	ns
t_{PZH} t_{PZL}	Output enable time to High and Low level	2	1.5 1.5	7.5 7.4	11.3 10.5	1.5 1.5	12.3 11.3	ns
t_{PHZ} t_{PLZ}	Output disable time from High and Low level	2	1.5 1.5	7.6 8.2	10.6 11.2	1.5 1.5	11.0 11.7	ns

AC WAVEFORMS



Waveform 1. Waveforms Showing the Input (A_n) to Output (Y_n) Propagation Delays

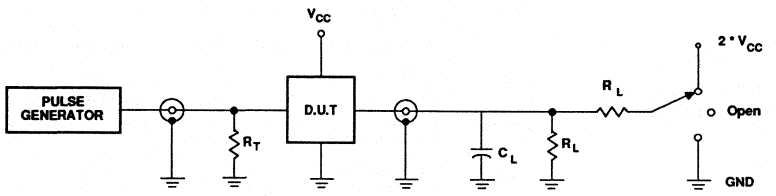


Waveform 2. Waveforms Showing the 3-State Output Enable and Disable Times

WAVEFORM CONDITIONS

	INPUTS	OUTPUTS
AC	V_{IN} = GND to V_{CC}, V_M = 50% V_{CC}	V_{OUT} = V_{OL} to V_{OH}
ACT	V_{IN} = GND to 3.0V, V_M = 1.5V	V_M = 50% V_{CC}

TEST CIRCUIT



Test Circuit

TEST	S1
t_{PLH}/t_{PHL}	Open
$t_{PLZ}t_{PZL}$	2*VCC
t_{PHZ}/t_{PZH}	GND

SWITCH POSITION

DEFINITIONS

C_L = Load capacitance, 50pF; includes jig and probe capacitance

R_L = Load resistor, 500Ω

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators

Input pulses: PRR ≤ 10MHz

$t_r = t_f$ = 3ns

74AC/ACT11244

Octal Buffer/Line Driver; 3-State

Product Specification

FEATURES

- **Octal bus interface**
- **3-State buffers**
- **Output capability: ±24 mA**
- **CMOS (AC) and TTL (ACT) voltage level inputs**
- **50Ω incident wave switching**
- **Center-pin V_{CC} and ground configuration to minimize high-speed switching noise**
- **I_{CC} category: MSI**

DESCRIPTION

The 74AC/ACT11244 high-performance CMOS devices combine very high speed and high output drive comparable to the most advanced TTL families.

The 74AC/ACT11244 device is an octal buffer that is ideal for driving bus lines or buffer memory address registers. The device features two Output Enables ($1\overline{OE}$, $2\overline{OE}$), each controlling four of the 3-State outputs.

GENERAL INFORMATION

SYMBOL	PARAMETER	CONDITIONS T_A = 25°C; GND = 0V; V_{CC} = 5.0V		TYPICAL AC	TYPICAL ACT	UNIT
t_{PLH}/t_{PHL}	Propagation delay A_n to Y_n	C_L = 50pF		4.7	5.7	ns
C_{PD}	Power dissipation capacitance per buffer[1]	f = 1MHz; C_L = 50pF	Enabled	27	27	pF
			Disabled	9	9	
C_{IN}	Input capacitance	V_I = 0V or V_{CC}		4.0	4.0	pF
C_{OUT}	Output capacitance	V_I = 0V or V_{CC}; Disabled		10	10	pF
I_{LATCH}	Latch-up current	Per Jedec JC40.2 Standard 17		500	500	mA

Note:

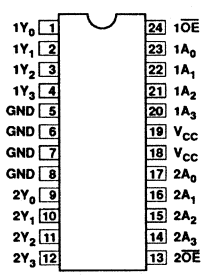
1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_I + \Sigma (C_L \times V_{CC}^2 \times f_O)$ where:
   f_I = input frequency in MHz, C_L = output load capacitance in pF,
   f_O = output frequency in MHz, V_{CC} = supply voltage in V,
   $\Sigma (C_L \times V_{CC}^2 \times f_O)$ = sum of outputs

ORDERING INFORMATION

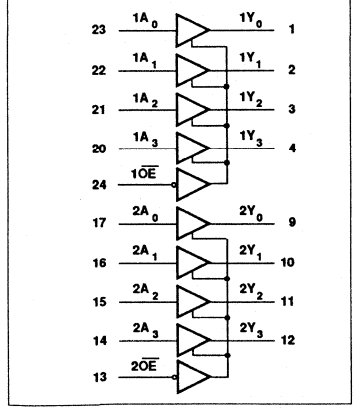
PACKAGES	TEMPERATURE RANGE	ORDER CODE
24-pin plastic DIP (300mil-wide)	-40°C to +85°C	74AC11244N 74ACT11244N
24-pin plastic SO (300mil-wide)	-40°C to +85°C	74AC11244D 74ACT11244D

PIN CONFIGURATION

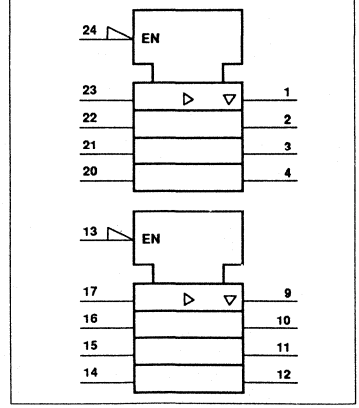
N and D Packages



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
23, 22, 21, 20	$1A_0$ - $1A_3$	Data inputs
17, 16, 15, 14	$2A_0$ - $2A_3$	Data inputs
1, 2, 3, 4	$1Y_0$ - $1Y_3$	Data outputs
9, 10, 11, 12	$2Y_0$ - $2Y_3$	Data outputs
24, 13	$1\overline{OE}$, $2\overline{OE}$	Output enables
5, 6, 7, 8	GND	Ground (0V)
18, 19	V_{CC}	Positive supply voltage

FUNCTION TABLE

INPUTS				OUTPUT	
$1\overline{OE}$	$1A_n$	$2\overline{OE}$	$2A_n$	$1Y_n$	$2Y_n$
L	L	L	L	L	L
L	H	L	H	H	H
H	X	H	X	Z	Z

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		74AC11244			74ACT11244			UNIT
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	DC supply voltage		3.0[1]	5.0	5.5	4.5	5.0	5.5	V
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
$\Delta t/\Delta v$	Input transition rise or fall rate	Data	0		10	0		10	ns/V
		Output enable	0		5	0		10	
T_A	Operating free-air temperature		-40		+85	-40		+85	°C

NOTE:

1. No electrical or switching characteristics are specified at V_{CC} < 3V. Operation between 2V and 3V is not recommended, but within that range, a device output will maintain a previously established logic state.

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	TEST CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 to+7.0	V
I_{IK} or V_I	DC input diode current[2]	$V_I < 0$	-20	mA
		$V_I > V_{CC}$	20	
	DC input voltage		-0.5 to V_{CC} +0.5	V
I_{OK} or V_O	DC output diode current[2]	$V_O < 0$	-50	mA
		$V_O > V_{CC}$	50	
	DC output voltage		-0.5 to V_{CC} +0.5	V
I_O	DC output source or sink current per output pin	V_O = 0 to V_{CC}	±50	mA
I_{CC} or I_{GND}	DC V_{CC} current		±200	mA
	DC ground current		±200	
T_{STG}	Storage temperature		-65 to 150	°C
P_{TOT}	Power dissipation per package Plastic DIP	Above 70°C:derate linearly by 8mW/K	500	mW
	Power dissipation per package Plastic surface mount (SO)	Above 70°C:derate linearly by 6mW/K	400	mW

NOTES:

1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		V_{CC}	74AC11244				74ACT11244				UNIT
					T_A = +25°C		T_A = -40°C to +85°C		T_A = +25°C		T_A = -40°C to +85°C		
				V	Min	Max	Min	Max	Min	Max	Min	Max	
V_{IH}	High-level input voltage			3.0	2.10		2.10						V
				4.5	3.15		3.15		2.0		2.0		
				5.5	3.85		3.85		2.0		2.0		
V_{IL}	Low-level input voltage			3.0		0.90		0.90					V
				4.5		1.35		1.35		0.8		0.8	
				5.5		1.65		1.65		0.8		0.8	
V_{OH}	High-level output voltage	V_I = V_{IL} or V_{IH}	I_{OH} = -50μA	3.0	2.9		2.9						V
				4.5	4.4		4.4		4.4		4.4		
				5.5	5.4		5.4		5.4		5.4		
			I_{OH} = -4mA	3.0	2.58		2.48						
			I_{OH} = -24mA	4.5	3.94		3.8		3.94		3.8		
				5.5	4.94		4.8		4.94		4.8		
			I_{OH} = -75mA[1]	5.5			3.85				3.85		
V_{OL}	Low-level output voltage	V_I = V_{IL} or V_{IH}	I_{OL} = 50μA	3.0		0.1		0.1					V
				4.5		0.1		0.1		0.1		0.1	
				5.5		0.1		0.1		0.1		0.1	
			I_{OL} = 12mA	3.0		0.36		0.44					
			I_{OL} = 24mA	4.5		0.36		0.44		0.36		0.44	
				5.5		0.36		0.44		0.36		0.44	
			I_{OL} = 75mA[1]	5.5				1.65				1.65	
I_I	Input leakage current	V_I = V_{CC} or GND		5.5		±0.1		±1.0		±0.1		±1.0	μA
I_{OZ}	3-State output off-state current	V_I = V_{IL} or V_{IH}; V_O = V_{CC} or GND		5.5		±0.5		±5.0		±0.5		±5.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC} or GND, I_O = 0		5.5		8.0		80		8.0		80	μA
ΔI_{CC}	Supply current, TTL inputs High[2]	One input at 3.4V, other inputs at V_{CC} or GND		5.5						0.9		1.0	mA

NOTES:
1. Not more than one output should be tested at a time, and the duration of the test should not exceed 10ms.
2. This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0V or V_{CC}.

AC ELECTRICAL CHARACTERISTICS AT 3.3V ±0.3V

SYMBOL	PARAMETER	WAVEFORM	74AC11244					UNIT
			T_A = +25°C			T_A = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay A_n to Y_n	1	1.5 1.5	7.1 6.3	9.3 8.6	1.5 1.5	10.2 9.5	ns
t_{PZH} t_{PZL}	Output enable time to High and Low level	2	1.5 1.5	8.0 7.9	10.7 10.6	1.5 1.5	11.8 11.9	ns
t_{PHZ} t_{PLZ}	Output disable time from High and Low level	2	1.5 1.5	5.9 7.2	7.9 9.4	1.5 1.5	8.3 9.9	ns

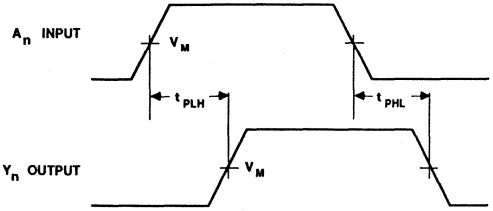
AC ELECTRICAL CHARACTERISTICS AT 5.0V ±0.5V

SYMBOL	PARAMETER	WAVEFORM	74AC11244					UNIT
			T_A = +25°C			T_A = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay A_n to Y_n	1	1.5 1.5	4.9 4.5	6.7 6.4	1.5 1.5	7.3 6.9	ns
t_{PZH} t_{PZL}	Output enable time to High and Low level	2	1.5 1.5	5.4 5.4	7.7 7.6	1.5 1.5	8.5 8.5	ns
t_{PHZ} t_{PLZ}	Output disable time from High and Low level	2	1.5 1.5	5.2 5.8	7.0 7.8	1.5 1.5	7.3 8.2	ns

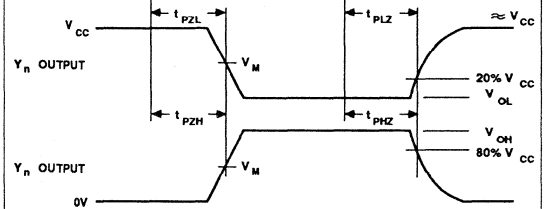
AC ELECTRICAL CHARACTERISTICS AT 5.0V ±0.5V

SYMBOL	PARAMETER	WAVEFORM	74ACT11244					UNIT
			T_A = +25°C			T_A = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay A_n to Y_n	1	1.5 1.5	6.0 5.4	8.9 8.6	1.5 1.5	9.9 9.2	ns
t_{PZH} t_{PZL}	Output enable time to High and Low level	2	1.5 1.5	6.6 6.7	11.3 10.5	1.5 1.5	12.5 11.4	ns
t_{PHZ} t_{PLZ}	Output disable time from High and Low level	2	1.5 1.5	7.4 7.8	9.8 10.6	1.5 1.5	10.4 11.2	ns

AC WAVEFORMS



Waveform 1. Waveforms Showing the Input (A_n) to Output (Y_n) Propagation Delays

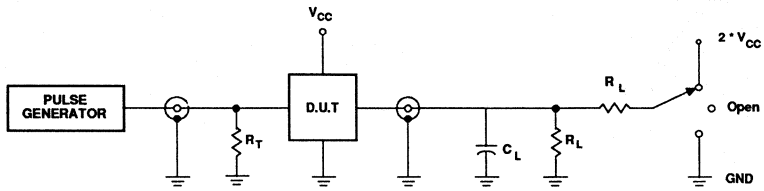


Waveform 2. Waveforms Showing the 3-State Output Enable and Disable Times

WAVEFORM CONDITIONS

	INPUTS	OUTPUTS
AC	V_{IN} = GND to V_{CC}, V_M = 50% V_{CC}	$V_{OUT} = V_{OL}$ to V_{OH}
ACT	V_{IN} = GND to 3.0V, V_M = 1.5V	V_M = 50% V_{CC}

TEST CIRCUIT



Test Circuit

TEST	S1
t_{PLH}/t_{PHL}	Open
$t_{PLZ}t_{PZL}$	2*VCC
t_{PHZ}/t_{PZH}	GND

SWITCH POSITION

DEFINITIONS

C_L = Load capacitance, 50pF; includes jig and probe capacitance

R_L = Load resistor, 500Ω

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators

Input pulses: PRR ≤ 10MHz

$t_r = t_f$ = 3ns

74AC/ACT11245

Octal Transceiver with Direction Pin; 3-State

Product Specification

FEATURES

- **Octal bidirectional bus interface**
- **3-State buffers**
- **Output capability: ±24 mA**
- **CMOS (AC) and TTL (ACT) voltage level inputs**
- **50Ω incident wave switching**
- **Center-pin V_{CC} and ground configuration to minimize high-speed switching noise**
- **I_{CC} category: MSI**

DESCRIPTION

The 74AC/ACT11245 high-performance CMOS devices combine very high speed and high output drive comparable to the most advanced TTL families.

The 74AC/ACT11245 device is an octal transceiver featuring noninverting 3-State bus compatible outputs in both send and receive directions. The control function implementation minimizes external timing requirements. The device features an Output Enable ($\overline{OE}$) input for easy cascading and a Direction (DIR) input for direction control.

GENERAL INFORMATION

SYMBOL	PARAMETER	CONDITIONS T_A = 25°C; GND = 0V; V_{CC} = 5.0V		TYPICAL AC	TYPICAL ACT	UNIT
t_{PLH}/t_{PHL}	Propagation delay A_n to B_n, or B_n to A_n	C_L = 50pF		4.5	5.8	ns
C_{PD}	Power dissipation capacitance per transceiver[1]	f = 1MHz; C_L = 50pF	Enabled	64	66	pF
			Disabled	16	19	
C_{IN}	Input capacitance	V_I = 0V or V_{CC}		4.0	4.0	pF
C_{OUT}	Output capacitance	V_I = 0V or V_{CC}; Disabled		12	12	pF
I_{LATCH}	Latch-up current	Per Jedec JC40.2 Standard 17		500	500	mA

Note:

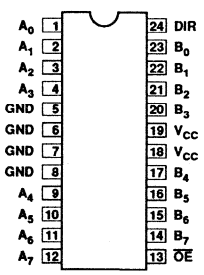
1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_I + \Sigma (C_L \times V_{CC}^2 \times f_O)$ where:
   f_I = input frequency in MHz, C_L = output load capacitance in pF,
   f_O = output frequency in MHz, V_{CC} = supply voltage in V,
   $\Sigma (C_L \times V_{CC}^2 \times f_O)$ = sum of outputs

ORDERING INFORMATION

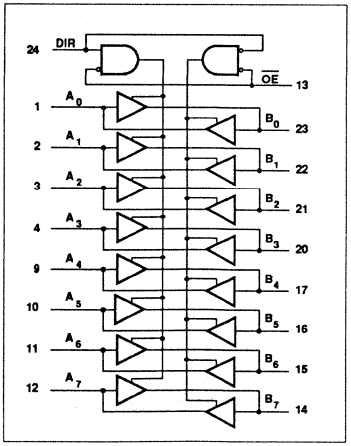
PACKAGES	TEMPERATURE RANGE	ORDER CODE
24-pin plastic DIP (300mil-wide)	-40°C to +85°C	74AC11245N 74ACT11245N
24-pin plastic SO (300mil-wide)	-40°C to +85°C	74AC11245D 74ACT11245D

PIN CONFIGURATION

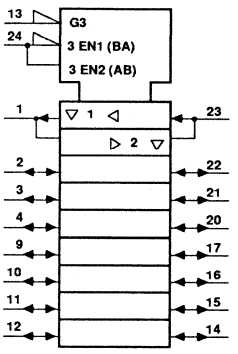
N and D Packages



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
24	DIR	Direction control input
1, 2, 3, 4, 9, 10, 11, 12	A_0 - A_7	Data inputs/outputs (A side)
23, 22, 21, 20, 17, 16, 15, 14	B_0 - B_7	Data inputs/outputs (B side)
13	$\overline{OE}$	Output enable
5, 6, 7, 8	GND	Ground (0V)
18, 19	V_{CC}	Positive supply voltage

FUNCTION TABLE

INPUTS		INPUTS/OUTPUTS	
$\overline{OE}$	DIR	A_n	B_n
L	L	A = B	inputs
L	H	inputs	B = A
H	X	Z	Z

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	74AC11245			74ACT11245			UNIT
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	DC supply voltage	3.0[1]	5.0	5.5	4.5	5.0	5.5	V
V_I	Input voltage	0		V_{CC}	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	0		V_{CC}	V
$\Delta t/\Delta v$	Input transition rise or fall rate	0		10	0		10	ns/V
T_A	Operating free-air temperature	-40		+85	-40		+85	°C

NOTE:

1. No electrical or switching characteristics are specified at V_{CC} < 3V. Operation between 2V and 3V is not recommended, but within that range, a device output will maintain a previously established logic state.

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	TEST CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 to+7.0	V
I_{IK} or V_I	DC input diode current[2]	V_I < 0	-20	mA
		V_I > V_{CC}	20	
	DC input voltage		-0.5 to V_{CC} +0.5	V
I_{OK} or V_O	DC output diode current[2]	V_O < 0	-50	mA
		V_O > V_{CC}	50	
	DC output voltage		-0.5 to V_{CC} +0.5	V
I_O	DC output source or sink current per output pin	V_O = 0 to V_{CC}	±50	mA
I_{CC} or I_{GND}	DC V_{CC} current		±200	mA
	DC ground current		±200	
T_{STG}	Storage temperature		-65 to 150	°C
P_{TOT}	Power dissipation per package Plastic DIP	Above 70°C:derate linearly by 8mW/K	500	mW
	Power dissipation per package Plastic surface mount (SO)	Above 70°C:derate linearly by 6mW/K	400	mW

NOTES:

1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		V_{CC}	74AC11245				74ACT11245				UNIT
					T_A = +25°C		T_A = -40°C to +85°C		T_A = +25°C		T_A = -40°C to +85°C		
				V	Min	Max	Min	Max	Min	Max	Min	Max	
V_{IH}	High-level input voltage			3.0	2.10		2.10						V
				4.5	3.15		3.15		2.0		2.0		
				5.5	3.85		3.85		2.0		2.0		
V_{IL}	Low-level input voltage			3.0		0.90		0.90					V
				4.5		1.35		1.35		0.8		0.8	
				5.5		1.65		1.65		0.8		0.8	
V_{OH}	High-level output voltage	V_I = V_{IL} or V_{IH}	I_{OH} = -50μA	3.0	2.9		2.9						V
				4.5	4.4		4.4		4.4		4.4		
				5.5	5.4		5.4		5.4		5.4		
			I_{OH} = -4mA	3.0	2.58		2.48						
			I_{OH} = -24mA	4.5	3.94		3.8		3.94		3.8		
				5.5	4.94		4.8		4.94		4.8		
			I_{OH} = -75mA[1]	5.5			3.85				3.85		
V_{OL}	Low-level output voltage	V_I = V_{IL} or V_{IH}	I_{OL} = 50μA	3.0		0.1		0.1					V
				4.5		0.1		0.1		0.1		0.1	
				5.5		0.1		0.1		0.1		0.1	
			I_{OL} = 12mA	3.0		0.36		0.44					
			I_{OL} = 24mA	4.5		0.36		0.44		0.36		0.44	
				5.5		0.36		0.44		0.36		0.44	
			I_{OL} = 75mA[1]	5.5				1.65				1.65	
I_I	Input leakage current	V_I = V_{CC} or GND		5.5		±0.1		±1.0		±0.1		±1.0	μA
I_{OZ}	3-State output off-state current	V_I = V_{IL} or V_{IH}, V_O = V_{CC} or GND		5.5		±0.5		±5.0		±0.5		±5.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC} or GND, I_O = 0		5.5		8.0		80		8.0		80	μA
ΔI_{CC}	Supply current, TTL inputs High[2]	One input at 3.4V, other inputs at V_{CC} or GND		5.5						0.9		1.0	mA

NOTES:
1. Not more than one output should be tested at a time, and the duration of the test should not exceed 10ms.
2. This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0V or V_{CC}.

AC ELECTRICAL CHARACTERISTICS AT 3.3V ±0.3V

SYMBOL	PARAMETER	WAVEFORM	74AC11245					UNIT
			T_A = +25°C			T_A = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay A_n to B_n, B_n to A_n	1	1.5 1.5	6.5 5.7	11.2 8.5	1.5 1.5	12.5 9.7	ns
t_{PZH} t_{PZL}	Output enable time to High and Low level	2	1.5 1.5	8.6 8.2	14.2 11.5	1.5 1.5	15.9 12.7	ns
t_{PHZ} t_{PLZ}	Output disable time from High and Low level	2	1.5 1.5	7.7 8.5	10.5 12.0	1.5 1.5	11.3 13.0	ns

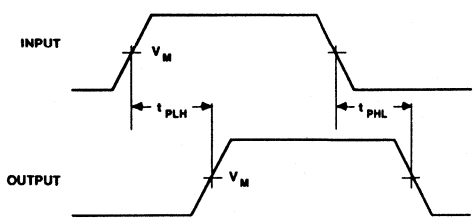
AC ELECTRICAL CHARACTERISTICS AT 5.0V ±0.5V

SYMBOL	PARAMETER	WAVEFORM	74AC11245					UNIT
			T_A = +25°C			T_A = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay A_n to B_n, B_n to A_n	1	1.5 1.5	4.8 4.1	8.5 6.3	1.5 1.5	9.5 6.9	ns
t_{PZH} t_{PZL}	Output enable time to High and Low level	2	1.5 1.5	6.2 5.9	10.2 8.6	1.5 1.5	11.4 9.5	ns
t_{PHZ} t_{PLZ}	Output disable time from High and Low level	2	1.5 1.5	6.4 7.0	8.8 9.6	1.5 1.5	9.5 10.4	ns

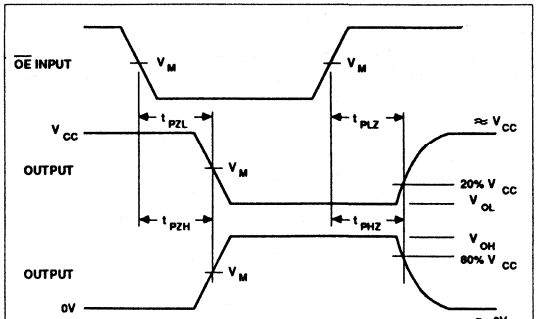
AC ELECTRICAL CHARACTERISTICS AT 5.0V ±0.5V

SYMBOL	PARAMETER	WAVEFORM	74ACT11245					UNIT
			T_A = +25°C			T_A = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay A_n to B_n, B_n to A_n	1	1.5 1.5	6.2 5.4	9.2 8.6	1.5 1.5	10.0 9.1	ns
t_{PZH} t_{PZL}	Output enable time to High and Low level	2	1.5 1.5	8.1 8.2	12.0 11.7	1.5 1.5	13.2 12.9	ns
t_{PHZ} t_{PLZ}	Output disable time from High and Low level	2	1.5 1.5	9.3 9.8	11.8 12.9	1.5 1.5	12.9 13.9	ns

AC WAVEFORMS



Waveform 1. Waveforms Showing the Input to Output Propagation Delays

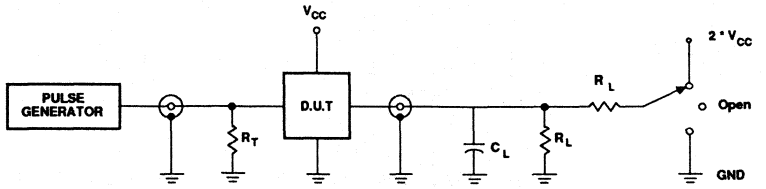


Waveform 2. Waveforms Showing the 3-State Output Enable and Disable Times

WAVEFORM CONDITIONS

	INPUTS	OUTPUTS
AC	V_{IN} = GND to V_{CC}, V_M = 50% V_{CC}	$V_{OUT} = V_{OL}$ to V_{OH}
ACT	V_{IN} = GND to 3.0V, V_M = 1.5V	V_M = 50% V_{CC}

TEST CIRCUIT



Test Circuit

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2*VCC
t_{PHZ}/t_{PZH}	GND

SWITCH POSITION

DEFINITIONS

C_L = Load capacitance, 50pF; includes jig and probe capacitance

R_L = Load resistor, 500Ω

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators

Input pulses: PRR ≤ 10MHz

$t_r = t_f$ = 3ns

74AC/ACT11250

16-Input Multiplexer (3-State), Inverting

Objective Specification

FEATURES

- **Output capability: ±24 mA**
- **CMOS (AC) and TTL (ACT) voltage level inputs**
- **50Ω incident wave switching**
- **Center-pin V_{CC} and ground configuration to minimize high-speed switching noise**
- **I_{CC} category: MSI**

DESCRIPTION

The 74AC/ACT11250 high-performance CMOS devices combine very high speed and high output drive comparable to the most advanced TTL families.

The 74AC/ACT11250 provides a 16-to-1 multiplexer with four select lines and an output enable. The state of the Select (S_n) inputs determines the particular input line from which the data comes. The output Enable ($\overline{OE}$) input is active-Low. When $\overline{OE}$ is High, the $\overline{Y}$ output is in the High-impedance "OFF" state regardless of all other input conditions.

The device is the logic implementation of a single pole, 16 position switch where the position of the switch is determined by the logic levels supplied to the Select inputs.

GENERAL INFORMATION

SYMBOL	PARAMETER	CONDITIONS T_A = 25°C; GND = 0V; V_{CC} = 5.0V		TYPICAL AC	TYPICAL ACT	UNIT
t_{PLH}/t_{PHL}	Propagation delay I_n to $\overline{Y}$	C_L = 50pF		5.8	7.5	ns
C_{PD}	Power dissipation capacitance[1]	f = 1MHz; C_L = 50pF	Enabled	56	64	pF
			Disabled	22	22	
C_{IN}	Input capacitance	V_I = 0V or V_{CC}		4.0	4.0	pF
C_{OUT}	Output capacitance	V_O = 0V or V_{CC}; Disabled		10	10	pF
I_{LATCH}	Latch-up current	Per Jedec JC40.2 Standard 17		500	500	mA

Note:

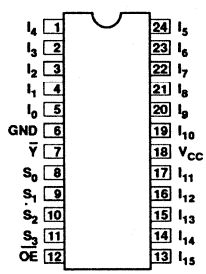
1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_I + \Sigma (C_L \times V_{CC}^2 \times f_O)$ where:
   f_I = input frequency in MHz, C_L = output load capacitance in pF,
   f_O = output frequency in MHz, V_{CC} = supply voltage in V,
   $\Sigma (C_L \times V_{CC}^2 \times f_O)$ = sum of outputs

ORDERING INFORMATION

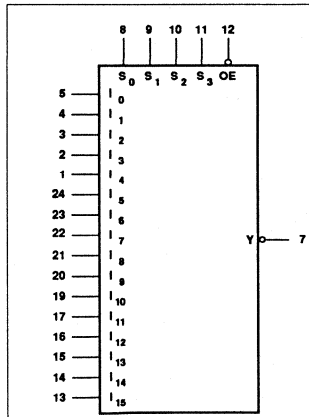
PACKAGES	TEMPERATURE RANGE	ORDER CODE
24-pin plastic DIP (300mil-wide)	-40°C to +85°C	74AC11250N 74ACT11250N
24-pin plastic SO (300mil-wide)	-40°C to +85°C	74AC11250D 74ACT11250D

PIN CONFIGURATION

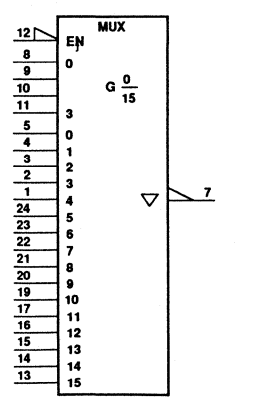
N and D Packages



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



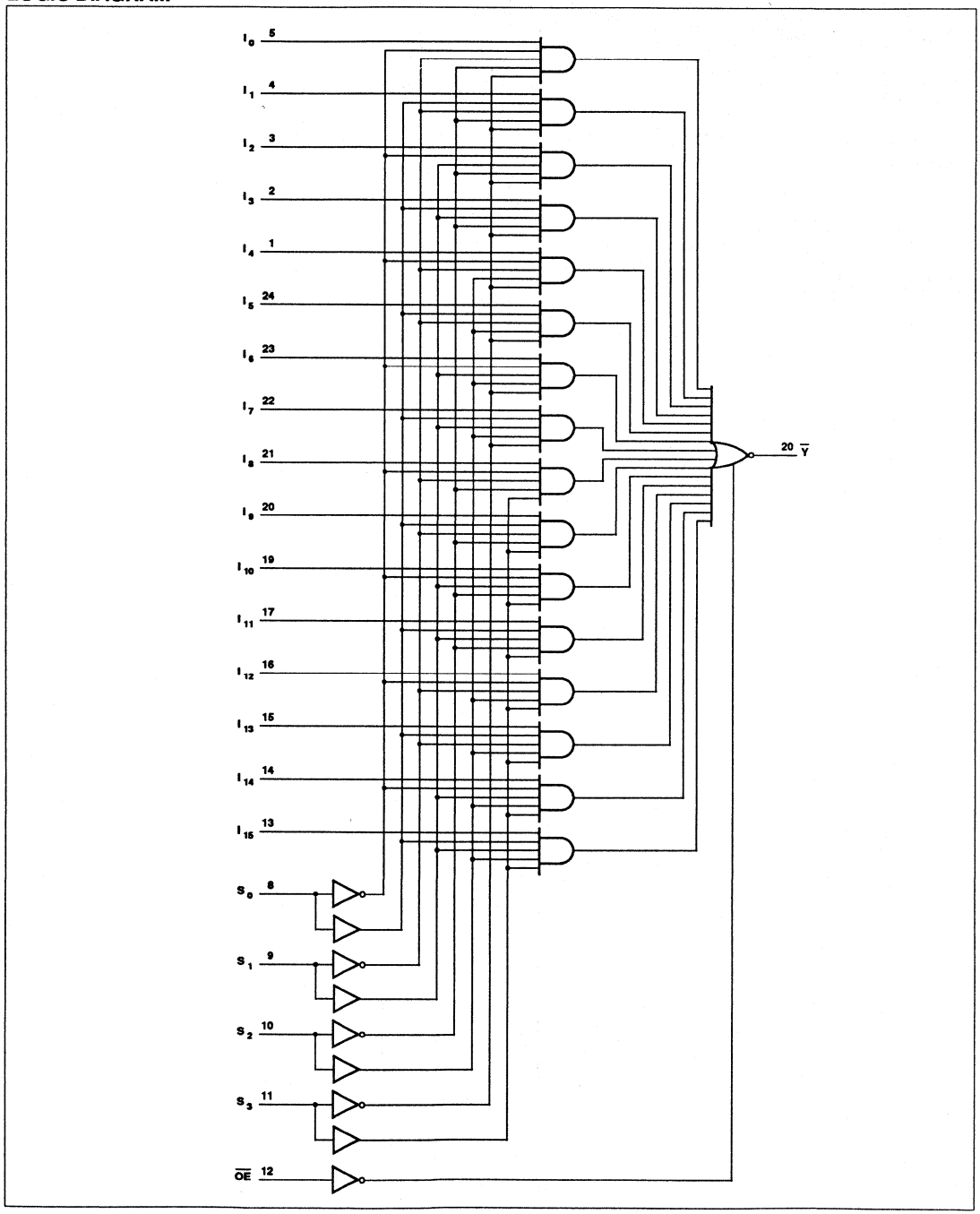
PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
12	$\overline{OE}$	Output enable input (active Low)
8, 9, 10, 11	S_0 - S_3	Select inputs
5, 4, 3, 2, 1, 24, 23, 22, 21, 20, 19, 17, 16, 15, 14, 13	I_0 - I_{15}	Data inputs
7	$\overline{Y}$	3-State data output
6	GND	Ground (0V)
18	V_{CC}	Positive supply voltage

FUNCTION TABLE

INPUT						OUTPUT
$\overline{E}$	S_3	S_2	S_1	S_0	I_n	$\overline{Y}$
L	L	L	L	L	I_0	$\overline{I_0}$
L	L	L	L	H	I_1	$\overline{I_1}$
L	L	L	H	L	I_2	$\overline{I_2}$
L	L	L	H	H	I_3	$\overline{I_3}$
L	L	H	L	L	I_4	$\overline{I_4}$
L	L	H	L	H	I_5	$\overline{I_5}$
L	L	H	H	L	I_6	$\overline{I_6}$
L	L	H	H	H	I_7	$\overline{I_7}$
L	H	L	L	L	I_8	$\overline{I_8}$
L	H	L	L	H	I_9	$\overline{I_9}$
L	H	L	H	L	I_{10}	$\overline{I_{10}}$
L	H	L	H	H	I_{11}	$\overline{I_{11}}$
L	H	H	L	L	I_{12}	$\overline{I_{12}}$
L	H	H	L	H	I_{13}	$\overline{I_{13}}$
L	H	H	H	L	I_{14}	$\overline{I_{14}}$
L	H	H	H	H	I_{15}	$\overline{I_{15}}$
H	X	X	X	X	X	Z

LOGIC DIAGRAM



RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	74AC11250			74ACT11250			UNIT
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	DC supply voltage	3.0[1]	5.0	5.5	4.5	5.0	5.5	V
V_I	Input voltage	0		V_{CC}	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	0		V_{CC}	V
$\Delta t/\Delta v$	Input transition rise or fall rate	0		10	0		10	ns/V
T_A	Operating free-air temperature	-40		+85	-40		+85	°C

NOTE:
1. No electrical or switching characteristics are specified at $V_{CC} < 3V$. Operation between 2V and 3V is not recommended, but within that range, a device output will maintain a previously established logic state.

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	TEST CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 to+7.0	V
I_{IK} or V_I	DC input diode current[2]	$V_I < 0$	-20	mA
		$V_I > V_{CC}$	20	
	DC input voltage		-0.5 to V_{CC} +0.5	V
I_{OK} or V_O	DC output diode current[2]	$V_O < 0$	-50	mA
		$V_O > V_{CC}$	50	
	DC output voltage		-0.5 to V_{CC} +0.5	V
I_O	DC output source or sink current per output pin	V_O = 0 to V_{CC}	±50	mA
I_{CC} or I_{GND}	DC V_{CC} current		±100	mA
	DC ground current		±100	
T_{STG}	Storage temperature		-65 to 150	°C
P_{TOT}	Power dissipation per package Plastic DIP	Above 70°C:derate linearly by 8mW/K	500	mW
	Power dissipation per package Plastic surface mount (SO)	Above 70°C:derate linearly by 6mW/K	400	mW

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		V_{CC}	74AC11250				74ACT11250				UNIT
					T_A = +25°C		T_A = -40°C to +85°C		T_A = +25°C		T_A = -40°C to +85°C		
				V	Min	Max	Min	Max	Min	Max	Min	Max	
V_{IH}	High-level input voltage			3.0	2.10		2.10						V
				4.5	3.15		3.15		2.0		2.0		
				5.5	3.85		3.85		2.0		2.0		
V_{IL}	Low-level input voltage			3.0		0.90		0.90					V
				4.5		1.35		1.35		0.8		0.8	
				5.5		1.65		1.65		0.8		0.8	
V_{OH}	High-level output voltage	V_I = V_{IL} or V_{IH}	I_{OH} = -50μA	3.0	2.9		2.9						V
				4.5	4.4		4.4		4.4		4.4		
				5.5	5.4		5.4		5.4		5.4		
			I_{OH} = -4mA	3.0	2.58		2.48						
			I_{OH} = -24mA	4.5	3.94		3.8		3.94		3.8		
				5.5	4.94		4.8		4.94		4.8		
			I_{OH} = -75mA[1]	5.5			3.85				3.85		
V_{OL}	Low-level output voltage	V_I = V_{IL} or V_{IH}	I_{OL} = 50μA	3.0		0.1		0.1					V
				4.5		0.1		0.1		0.1		0.1	
				5.5		0.1		0.1		0.1		0.1	
			I_{OL} = 12mA	3.0		0.36		0.44					
			I_{OL} = 24mA	4.5		0.36		0.44		0.36		0.44	
				5.5		0.36		0.44		0.36		0.44	
			I_{OL} = 75mA[1]	5.5				1.65				1.65	
I_I	Input leakage current	V_I = V_{CC} or GND		5.5		±0.1		±1.0		±0.1		±1.0	μA
I_{OZ}	3-State output off-state current	V_I = V_{IL} or V_{IH}, V_O = V_{CC} or GND		5.5		±0.5		±5.0		±0.5		±5.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC} or GND, I_O = 0		5.5		8.0		80		8.0		80	μA
ΔI_{CC}	Supply current, TTL inputs High[2]	One input at 3.4V, other inputs at V_{CC} or GND		5.5						0.9		1.0	mA

NOTES:
1. Not more than one output should be tested at a time, and the duration of the test should not exceed 10ms.
2. This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0V or V_{CC}.

74AC/ACT11251

8-Input Multiplexer (3-State)

Preliminary Specification

FEATURES

- **Output capability: ±24 mA**
- **CMOS (AC) and TTL (ACT) voltage level inputs**
- **50Ω incident wave switching**
- **Center-pin V_{CC} and ground configuration to minimize high-speed switching noise**
- **I_{CC} category: MSI**

DESCRIPTION

The 74AC/ACT11251 high-performance CMOS devices combine very high speed and high output drive comparable to the most advanced TTL families.

The 74AC/ACT11251 provides an 8-to-1 multiplexer with three select lines and a common output enable. The state of the Select (S_n) inputs determines the particular input line from which the data comes. The Output Enable ($\overline{OE}$) input is active-Low. When $\overline{OE}$ is High, both the Y output and the $\overline{Y}$ output are in the High-impedance "OFF" state regardless of all other input conditions.

The device is the logic implementation of a single pole, 8 position switch where the position of the switch is determined by the logic levels supplied to the Select inputs.

GENERAL INFORMATION

SYMBOL	PARAMETER	CONDITIONS T_A = 25°C; GND = 0V; V_{CC} = 5.0V		TYPICAL AC	TYPICAL ACT	UNIT
t_{PLH}/ t_{PHL}	Propagation delay I_n to Y	C_L = 50pF		4.8	6.6	ns
C_{PD}	Power dissipation capacitance[1]	f = 1MHz;	Enabled	55	60	pF
		C_L = 50pF	Disabled	13	16	
C_{IN}	Input capacitance	V_I = 0V or V_{CC}		3.5	3.5	pF
C_{OUT}	Output capacitance	V_O = 0V or V_{CC}; Disabled		8.0	8.0	pF

Note:

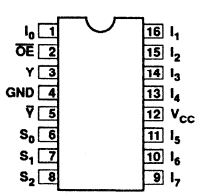
1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_I + \Sigma (C_L \times V_{CC}^2 \times f_O)$ where:
   f_I = input frequency in MHz, C_L = output load capacitance in pF,
   f_O = output frequency in MHz, V_{CC} = supply voltage in V,
   $\Sigma (C_L \times V_{CC}^2 \times f_O)$ = sum of outputs

ORDERING INFORMATION

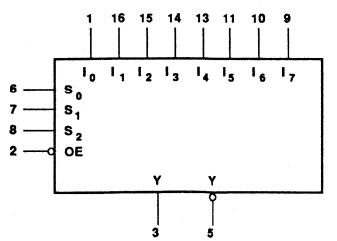
PACKAGES	TEMPERATURE RANGE	ORDER CODE
16-pin plastic DIP (300mil-wide)	-40°C to +85°C	74AC11251N 74ACT11251N
16-pin plastic SO (150mil-wide)	-40°C to +85°C	74AC11251D 74ACT11251D

PIN CONFIGURATION

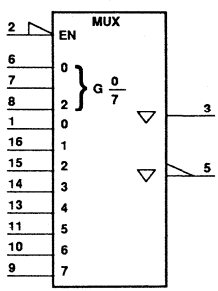
N and D Packages



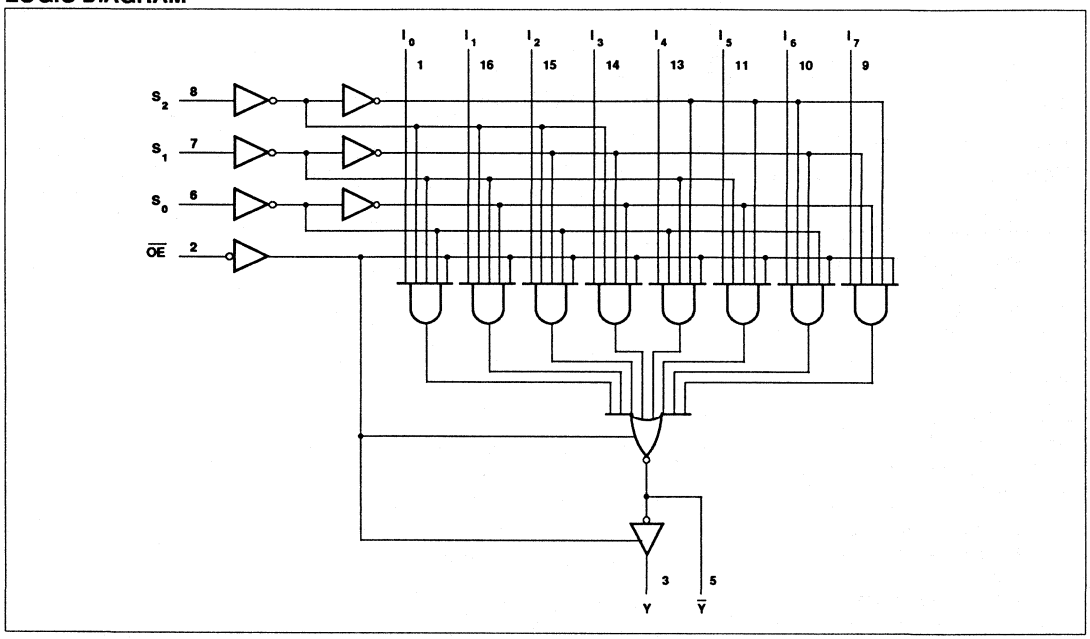
LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



LOGIC DIAGRAM



PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
6, 7, 8	S_n	Select inputs
2	$\overline{OE}$	Output enable input
1, 16, 15, 14 13, 11, 10, 9	I_0 - I_7	Data inputs
3, 5	Y, $\overline{Y}$	Data outputs
4	GND	Ground (0V)
12	V_{CC}	Positive supply voltage

FUNCTION TABLE

INPUTS				OUTPUTS	
S_2	S_1	S_0	$\overline{OE}$	Y	$\overline{Y}$
X	X	X	H	Z	Z
L	L	L	L	I_0	$\overline{I}_0$
L	L	H	L	I_1	$\overline{I}_1$
L	H	L	L	I_2	$\overline{I}_2$
L	H	H	L	I_3	$\overline{I}_3$
H	L	L	L	I_4	$\overline{I}_4$
H	L	H	L	I_5	$\overline{I}_5$
H	H	L	L	I_6	$\overline{I}_6$
H	H	H	L	I_7	$\overline{I}_7$

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	74AC11151			74ACT11151			UNIT
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	DC supply voltage	3.0[1]	5.0	5.5	4.5	5.0	5.5	V
V_I	Input voltage	0		V_{CC}	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	0		V_{CC}	V
$\Delta t/\Delta v$	Input transition rise or fall rate	0		10	0		10	ns/V
T_A	Operating free-air temperature	-40		+85	-40		+85	°C

NOTE:
1. No electrical or switching characteristics are specified at V_{CC} < 3V. Operation between 2V and 3V is not recommended, but within that range, a device output will maintain a previously established logic state.

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	TEST CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 to+7.0	V
I_{IK} or V_I	DC input diode current[2]	$V_I < 0$	-20	mA
		$V_I > V_{CC}$	20	
	DC input voltage		-0.5 to V_{CC} +0.5	V
I_{OK} or V_O	DC output diode current[2]	$V_O < 0$	-50	mA
		$V_O > V_{CC}$	50	
	DC output voltage		-0.5 to V_{CC} +0.5	V
I_O	DC output source or sink current per output pin	V_O = 0 to V_{CC}	±50	mA
I_{CC} or I_{GND}	DC V_{CC} current		±100	mA
	DC ground current		±100	
T_{STG}	Storage temperature		-65 to 150	°C
P_{TOT}	Power dissipation per package Plastic DIP	Above 70°C:derate linearly by 8mW/K	500	mW
	Power dissipation per package Plastic surface mount (SO)	Above 70°C:derate linearly by 6mW/K	400	mW

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		V_{CC}	74AC11251				74ACT11251				UNIT
					T_A = +25°C		T_A = -40°C to +85°C		T_A = +25°C		T_A = -40°C to +85°C		
				V	Min	Max	Min	Max	Min	Max	Min	Max	
V_{IH}	High-level input voltage			3.0	2.10		2.10						V
				4.5	3.15		3.15		2.0		2.0		
				5.5	3.85		3.85		2.0		2.0		
V_{IL}	Low-level input voltage			3.0		0.90		0.90					V
				4.5		1.35		1.35		0.8		0.8	
				5.5		1.65		1.65		0.8		0.8	
V_{OH}	High-level output voltage	V_I = V_{IL} or V_{IH}	I_{OH} = -50μA	3.0	2.9		2.9						V
				4.5	4.4		4.4		4.4		4.4		
				5.5	5.4		5.4		5.4		5.4		
			I_{OH} = -4mA	3.0	2.58		2.48						
			I_{OH} = -24mA	4.5	3.94		3.8		3.94		3.8		
				5.5	4.94		4.8		4.94		4.8		
			I_{OH} = -75mA[1]	5.5			3.85				3.85		
V_{OL}	Low-level output voltage	V_I = V_{IL} or V_{IH}	I_{OL} = 50μA	3.0		0.1		0.1					V
				4.5		0.1		0.1		0.1		0.1	
				5.5		0.1		0.1		0.1		0.1	
			I_{OL} = 12mA	3.0		0.36		0.44					
			I_{OL} = 24mA	4.5		0.36		0.44		0.36		0.44	
				5.5		0.36		0.44		0.36		0.44	
			I_{OL} = 75mA[1]	5.5				1.65				1.65	
I_I	Input leakage current	V_I = V_{CC} or GND		5.5		±0.1		±1.0		±0.1		±1.0	μA
I_{OZ}	3-State output off-state current	V_I = V_{IL} or V_{IH}, V_O = V_{CC} or GND		5.5		±0.5		±5.0		±0.5		±5.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC} or GND, I_O = 0		5.5		8.0		80		8.0		80	μA
ΔI_{CC}	Supply current, TTL inputs High[2]	One input at 3.4V, other inputs at V_{CC} or GND		5.5						0.9		1.0	mA

NOTES:
1. Not more than one output should be tested at a time, and the duration of the test should not exceed 10ms.
2. This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0V or V_{CC}.

AC ELECTRICAL CHARACTERISTICS AT 3.3V ±0.3V

SYMBOL	PARAMETER	WAVEFORM	74AC11251					UNIT
			T_A = +25°C			T_A = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay I_n to Y	1	1.5 1.5	7.0 6.9	8.6 8.3	1.5 1.5	9.3 8.9	ns
t_{PLH} t_{PHL}	Propagation delay I_n to $\overline{Y}$	1	1.5 1.5	6.1 6.6	7.5 8.0	1.5 1.5	8.1 8.8	ns
t_{PLH} t_{PHL}	Propagation delay S_n to Y	1	1.5 1.5	10.0 9.6	11.6 11.1	1.5 1.5	12.6 12.1	ns
t_{PLH} t_{PHL}	Propagation delay S_n to $\overline{Y}$	1	1.5 1.5	8.9 9.6	10.4 11.1	1.5 1.5	11.3 12.1	ns
t_{PZH} t_{PZL}	Propagation delay $\overline{OE}$ to Y	2	1.5 1.5	4.6 5.5	5.9 6.8	1.5 1.5	6.3 7.2	ns
t_{PZH} t_{PZL}	Propagation delay $\overline{OE}$ to $\overline{Y}$	2	1.5 1.5	4.1 5.0	5.4 6.3	1.5 1.5	5.8 6.8	ns
t_{PHZ} t_{PLZ}	Propagation delay $\overline{OE}$ to Y	2	1.5 1.5	4.3 5.0	5.5 6.2	1.5 1.5	5.7 6.4	ns
t_{PHZ} t_{PLZ}	Propagation delay $\overline{OE}$ to $\overline{Y}$	2	1.5 1.5	4.0 4.4	5.1 5.6	1.5 1.5	5.4 5.8	ns

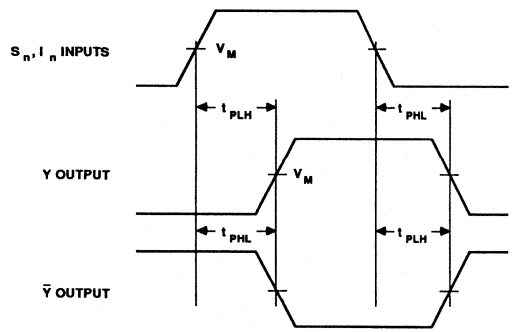
AC ELECTRICAL CHARACTERISTICS AT 5.0V ±0.5V

SYMBOL	PARAMETER	WAVEFORM	74AC11251					UNIT
			T_A = +25°C			T_A = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay I_n to Y	1	1.5 1.5	4.8 4.7	6.1 6.0	1.5 1.5	6.7 6.5	ns
t_{PLH} t_{PHL}	Propagation delay I_n to $\overline{Y}$	1	1.5 1.5	4.1 4.5	5.4 5.9	1.5 1.5	5.8 6.4	ns
t_{PLH} t_{PHL}	Propagation delay S_n to Y	1	1.5 1.5	6.6 6.5	7.9 7.8	1.5 1.5	8.6 8.5	ns
t_{PLH} t_{PHL}	Propagation delay S_n to $\overline{Y}$	1	1.5 1.5	5.9 6.3	7.2 7.7	1.5 1.5	7.8 8.4	ns
t_{PZH} t_{PZL}	Propagation delay $\overline{OE}$ to Y	2	1.5 1.5	3.2 3.8	4.5 5.1	1.5 1.5	4.7 5.4	ns
t_{PZH} t_{PZL}	Propagation delay $\overline{OE}$ to $\overline{Y}$	2	1.5 1.5	2.9 3.5	4.2 4.8	1.5 1.5	4.4 5.1	ns
t_{PHZ} t_{PLZ}	Propagation delay $\overline{OE}$ to Y	2	1.5 1.5	4.0 4.4	5.3 5.6	1.5 1.5	5.4 5.9	ns
t_{PHZ} t_{PLZ}	Propagation delay $\overline{OE}$ to $\overline{Y}$	2	1.5 1.5	3.6 3.7	4.8 4.9	1.5 1.5	5.0 5.1	ns

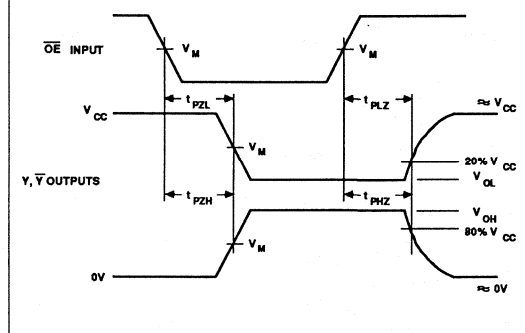
AC ELECTRICAL CHARACTERISTICS AT 5.0V ±0.5V

SYMBOL	PARAMETER	WAVEFORM	74ACT11251					UNIT
			T_A = +25°C			T_A = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay I_n to Y	1	1.5 1.5	6.4 6.7	7.8 8.1	1.5 1.5	8.5 8.7	ns
t_{PLH} t_{PHL}	Propagation delay I_n to $\overline{Y}$	1	1.5 1.5	6.0 5.9	7.4 7.3	1.5 1.5	7.9 7.9	ns
t_{PLH} t_{PHL}	Propagation delay S_n to Y	1	1.5 1.5	9.3 8.2	10.9 9.8	1.5 1.5	11.8 10.7	ns
t_{PLH} t_{PHL}	Propagation delay S_n to $\overline{Y}$	1	1.5 1.5	7.8 8.8	9.5 10.4	1.5 1.5	10.2 11.4	ns
t_{PZH} t_{PZL}	Propagation delay $\overline{OE}$ to Y	2	1.5 1.5	5.3 4.8	6.7 6.2	1.5 1.5	7.0 6.6	ns
t_{PZH} t_{PZL}	Propagation delay $\overline{OE}$ to $\overline{Y}$	2	1.5 1.5	5.2 4.7	6.5 6.0	1.5 1.5	7.0 6.4	ns
t_{PHZ} t_{PLZ}	Propagation delay $\overline{OE}$ to Y	2	1.5 1.5	6.0 5.2	7.3 6.4	1.5 1.5	7.7 6.7	ns
t_{PHZ} t_{PLZ}	Propagation delay $\overline{OE}$ to $\overline{Y}$	2	1.5 1.5	5.9 4.9	7.2 6.2	1.5 1.5	7.6 6.4	ns

AC WAVEFORMS



Waveform 1. Waveforms Showing the Data Inputs (I_n) and Select Input (S_n) to Output (Y, $\overline{Y}$) Propagation Delays

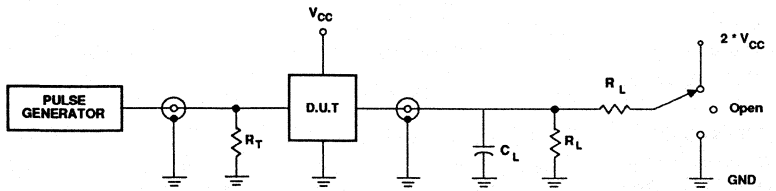


Waveform 2. Waveforms Showing the Output Enable Input ($\overline{OE}$) to Output (Y, $\overline{Y}$) Propagation Delays

WAVEFORM CONDITIONS

	INPUTS	OUTPUTS
AC	V_{IN} = GND to V_{CC}, V_M = 50% V_{CC}	V_{OUT} = V_{OL} to V_{OH}
ACT	V_{IN} = GND to 3.0V, V_M = 1.5V	V_M = 50% V_{CC}

TEST CIRCUIT



Test Circuit

TEST	S1
t_{PLH}/t_{PHL}	Open
$t_{PLZ}t_{PZL}$	2*VCC
t_{PHZ}/t_{PZH}	GND

SWITCH POSITION

DEFINITIONS

C_L = Load capacitance, 50pF; includes jig and probe capacitance

R_L = Load resistor, 500Ω

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators

Input pulses: PRR ≤ 10MHz

$t_r = t_f$ = 3ns

74AC/ACT11253

Dual 4-Input Multiplexer; 3-State

Product Specification

FEATURES

- **3-State outputs for bus interface and multiplex expansion**
- **Separate 3-State Output Enable inputs**
- **Common Select inputs**
- **Output capability: ±24 mA**
- **CMOS (AC) and TTL (ACT) voltage level inputs**
- **50Ω incident wave switching**
- **Center-pin V_{CC} and ground configuration to minimize high-speed switching noise**
- **I_{CC} category: MSI**

DESCRIPTION

The 74AC/ACT11253 high-performance CMOS devices combine very high speed and high output drive comparable to the most advanced TTL families.

The 74AC/ACT11253 device provides two identical 4-input multiplexers with 3-State outputs which select two bits from four sources selected by common select inputs (S_0, S_1). When the individual output enable ($1\overline{OE}$, $2\overline{OE}$) inputs of the 4-input multiplexers are High, the outputs are forced to a high impedance state.

GENERAL INFORMATION

SYMBOL	PARAMETER	CONDITIONS T_A = 25°C; GND = 0V; V_{CC} = 5.0V		TYPICAL AC	TYPICAL ACT	UNIT
t_{PLH}/t_{PHL}	Propagation delay $1I_n$, $2I_n$ to nY	C_L = 50pF		4.7	6.5	ns
C_{PD}	Power dissipation capacitance per multiplexer[1]	f = 1MHz; C_L = 50pF	Enabled	35	41	pF
			Disabled	11	15	
C_{IN}	Input capacitance	V_I = 0V or V_{CC}		3.5	3.5	pF
C_{OUT}	Output capacitance	V_I = 0V or V_{CC}; Disabled		8	8	pF
I_{LATCH}	Latch-up current	Per Jedec JC40.2 Standard 17		500	500	mA

Note:

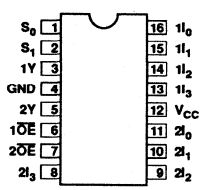
1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_I + \Sigma (C_L \times V_{CC}^2 \times f_O)$ where:
   f_I = input frequency in MHz, C_L = output load capacitance in pF,
   f_O = output frequency in MHz, V_{CC} = supply voltage in V,
   $\Sigma (C_L \times V_{CC}^2 \times f_O)$ = sum of outputs

ORDERING INFORMATION

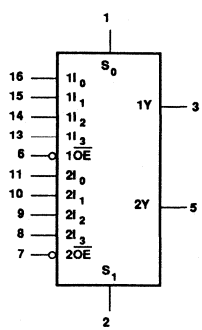
PACKAGES	TEMPERATURE RANGE	ORDER CODE
16-pin plastic DIP (300mil-wide)	-40°C to +85°C	74AC11253N 74ACT11253N
16-pin plastic SO (150mil-wide)	-40°C to +85°C	74AC11253D 74ACT11253D

PIN CONFIGURATION

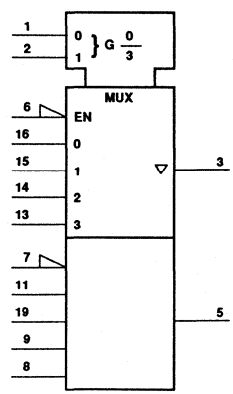
N and D Packages



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



The 74AC/ACT11253 devices are the logic implementation of a 2-pole, 4-position switch; the position of the switch being determined by the logic levels supplied to the two select inputs.

The '11253 is the non-inverting version of the '11353.

PIN DESCRIPTION

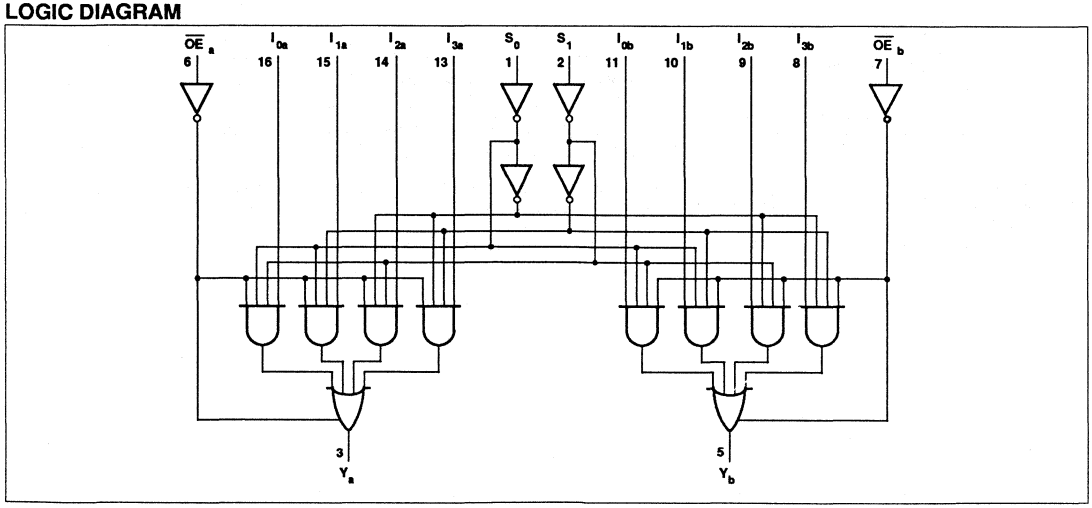
PIN NUMBER	SYMBOL	NAME AND FUNCTION
1, 2	S_0, S_1	Common select inputs
16, 15, 14, 13	$1I_0$ - $1I_3$	Port A data inputs
11, 10, 9, 8	$2I_0$ - $2I_3$	Port B data inputs
6	$1\overline{OE}$	Port A output enable input
7	$2\overline{OE}$	Port B output enable input
3, 5	1Y, 2Y	3-State data outputs
4	GND	Ground (0V)
12	V_{CC}	Positive supply voltage

FUNCTION TABLE

INPUTS							OUTPUT
$\overline{OE}_n$	S_1	S_0	I_{0n}	I_{1n}	I_{2n}	I_{3n}	Y_n
H	X	X	X	X	X	X	Z
L	L	L	L	X	X	X	L
L	L	L	H	X	X	X	H
L	L	H	X	L	X	X	L
L	L	H	X	H	X	X	H
L	H	L	X	X	L	X	L
L	H	L	X	X	H	X	H
L	H	H	X	X	X	L	L
L	H	H	X	X	X	H	H

H = High voltage level steady state
L = Low voltage level steady state
X = Don't care
Z = High-impedance "OFF" state

LOGIC DIAGRAM



RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	74AC11253			74ACT11253			UNIT
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	DC supply voltage	3.0[1]	5.0	5.5	4.5	5.0	5.5	V
V_I	Input voltage	0		V_{CC}	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	0		V_{CC}	V
$\Delta t/\Delta v$	Input transition rise or fall rate	0		10	0		10	ns/V
T_A	Operating free-air temperature	-40		+85	-40		+85	°C

NOTE:

1. No electrical or switching characteristics are specified at V_{CC} < 3V. Operation between 2V and 3V is not recommended, but within that range, a device output will maintain a previously established logic state.

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	TEST CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 to+7.0	V
I_{IK} or V_I	DC input diode current[2]	$V_I < 0$	-20	mA
		$V_I > V_{CC}$	20	
	DC input voltage		-0.5 to V_{CC} +0.5	V
I_{OK} or V_O	DC output diode current[2]	$V_O < 0$	-50	mA
		$V_O > V_{CC}$	50	
	DC output voltage		-0.5 to V_{CC} +0.5	V
I_O	DC output source or sink current per output pin	V_O = 0 to V_{CC}	±50	mA
I_{CC} or I_{GND}	DC V_{CC} current		±100	mA
	DC ground current		±100	
T_{STG}	Storage temperature		-65 to 150	°C
P_{TOT}	Power dissipation per package Plastic DIP	Above 70°C:derate linearly by 8mW/K	500	mW
	Power dissipation per package Plastic surface mount (SO)	Above 70°C:derate linearly by 6mW/K	400	mW

NOTES:

1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		V_{CC}	74AC11253				74ACT11253				UNIT
					T_A = +25°C		T_A = -40°C to +85°C		T_A = +25°C		T_A = -40°C to +85°C		
				V	Min	Max	Min	Max	Min	Max	Min	Max	
V_{IH}	High-level input voltage			3.0	2.10		2.10						V
				4.5	3.15		3.15		2.0		2.0		
				5.5	3.85		3.85		2.0		2.0		
V_{IL}	Low-level input voltage			3.0		0.90		0.90					V
				4.5		1.35		1.35		0.8		0.8	
				5.5		1.65		1.65		0.8		0.8	
V_{OH}	High-level output voltage	V_I = V_{IL} or V_{IH}	I_{OH} = -50μA	3.0	2.9		2.9						V
				4.5	4.4		4.4		4.4		4.4		
				5.5	5.4		5.4		5.4		5.4		
			I_{OH} = -4mA	3.0	2.58		2.48						
			I_{OH} = -24mA	4.5	3.94		3.8		3.94		3.8		
				5.5	4.94		4.8		4.94		4.8		
			I_{OH} = -75mA[1]	5.5			3.85				3.85		
V_{OL}	Low-level output voltage	V_I = V_{IL} or V_{IH}	I_{OL} = 50μA	3.0		0.1		0.1					V
				4.5		0.1		0.1		0.1		0.1	
				5.5		0.1		0.1		0.1		0.1	
			I_{OL} = 12mA	3.0		0.36		0.44					
			I_{OL} = 24mA	4.5		0.36		0.44		0.36		0.44	
				5.5		0.36		0.44		0.36		0.44	
			I_{OL} = 75mA[1]	5.5				1.65				1.65	
I_I	Input leakage current	V_I = V_{CC} or GND		5.5		±0.1		±1.0		±0.1		±1.0	μA
I_{OZ}	3-State output off-state current	V_I = V_{IL} or V_{IH}; V_O = V_{CC} or GND		5.5		±0.5		±5.0		±0.5		±5.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC} or GND, I_O = 0		5.5		8.0		80		8.0		80	μA
ΔI_{CC}	Supply current, TTL inputs High[2]	One input at 3.4V, other inputs at V_{CC} or GND		5.5						0.9		1.0	mA

NOTES:
1. Not more than one output should be tested at a time, and the duration of the test should not exceed 10ms.
2. This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0V or V_{CC}.

AC ELECTRICAL CHARACTERISTICS AT 3.3V ±0.3V

SYMBOL	PARAMETER	WAVEFORM	74AC11253					UNIT
			T_A = +25°C			T_A = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay I_n to nY	1	1.5 1.5	6.8 7.0	8.3 8.8	1.5 1.5	9.3 9.6	ns
t_{PLH} t_{PHL}	Propagation delay nS to nY	1	1.5 1.5	7.1 7.5	9.7 10.1	1.5 1.5	11.0 11.4	ns
t_{PZH} t_{PZL}	Output enable time to High and Low level	2	1.5 1.5	4.8 5.8	6.2 7.4	1.5 1.5	6.8 8.2	ns
t_{PHZ} t_{PLZ}	Output disable time from High and Low level	2	1.5 1.5	5.0 5.2	6.3 6.5	1.5 1.5	6.7 6.9	ns

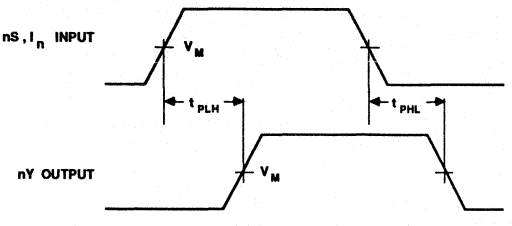
AC ELECTRICAL CHARACTERISTICS AT 5.0V ±0.5V

SYMBOL	PARAMETER	WAVEFORM	74AC11253					UNIT
			T_A = +25°C			T_A = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay I_n to nY	1	1.5 1.5	4.5 4.8	5.9 6.3	1.5 1.5	6.6 6.9	ns
t_{PLH} t_{PHL}	Propagation delay nS to nY	1	1.5 1.5	4.9 5.2	7.0 7.3	1.5 1.5	7.9 8.2	ns
t_{PZH} t_{PZL}	Output enable time to High and Low level	2	1.5 1.5	3.4 4.0	4.6 5.3	1.5 1.5	5.1 5.8	ns
t_{PHZ} t_{PLZ}	Output disable time from High and Low level	2	1.5 1.5	4.7 4.6	6.0 5.9	1.5 1.5	6.3 6.2	ns

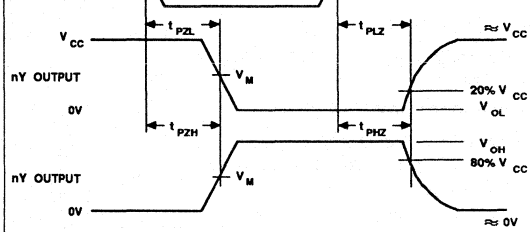
AC ELECTRICAL CHARACTERISTICS AT 5.0V ±0.5V

SYMBOL	PARAMETER	WAVEFORM	74ACT11253					UNIT
			T_A = +25°C			T_A = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay I_n to nY	1	1.5 1.5	5.7 7.2	7.4 10.5	1.5 1.5	8.3 11.7	ns
t_{PLH} t_{PHL}	Propagation delay nS to nY	1	1.5 1.5	6.8 9.1	9.8 12.6	1.5 1.5	11.0 14.3	ns
t_{PZH} t_{PZL}	Output enable time to High and Low level	2	1.5 1.5	5.0 4.8	7.6 7.3	1.5 1.5	8.5 8.1	ns
t_{PHZ} t_{PLZ}	Output disable time from High and Low level	2	1.5 1.5	6.4 5.9	8.6 7.4	1.5 1.5	9.2 7.8	ns

AC WAVEFORMS



Waveform 1. Waveforms Showing the Input (I_n and nS) to Output (nY) Propagation Delays

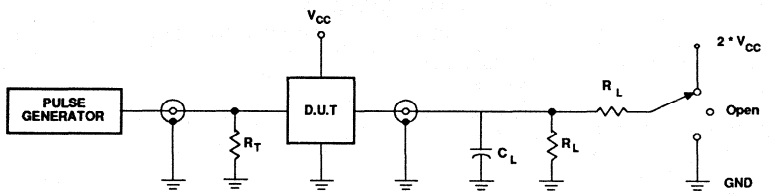


Waveform 2. Waveforms Showing the 3-State Output Enable and Disable Times

WAVEFORM CONDITIONS

	INPUTS	OUTPUTS
AC	V_{IN} = GND to V_{CC}, V_M = 50% V_{CC}	V_{OUT} = V_{OL} to V_{OH}
ACT	V_{IN} = GND to 3.0V, V_M = 1.5V	V_M = 50% V_{CC}

TEST CIRCUIT



Test Circuit

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2*VCC
t_{PHZ}/t_{PZH}	GND

SWITCH POSITION

DEFINITIONS

C_L = Load capacitance, 50pF; includes jig and probe capacitance

R_L = Load resistor, 500Ω

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators

Input pulses: PRR ≤ 10MHz

$t_r = t_f$ = 3ns

74AC/ACT11257

Quad 2-Input Multiplexer (3-State)

Product Specification

FEATURES

- **Output capability: ±24 mA**
- **CMOS (AC) and TTL (ACT) voltage level inputs**
- **50Ω incident wave switching**
- **Center-pin V_{CC} and ground configuration to minimize high-speed switching noise**
- **I_{CC} category: MSI**

DESCRIPTION

The 74AC/ACT11257 high-performance CMOS devices combine very high speed and high output drive comparable to the most advanced TTL families.

The 74AC/ACT11257 provides four 2-to-1 multiplexers with 3-State outputs which have a common selector and a common output enable. The state of the Select (S) input determines the particular input from which the data comes. The Output Enable ($\overline{OE}$) input is active-Low. When $\overline{OE}$ is High, all of the outputs (Y) are forced to a High-impedance state regardless of all other input conditions.

The device is the logic implementation of a 4-pole, 2 position switch where the position of the switch is determined by the logic levels supplied to the Select input.

GENERAL INFORMATION

SYMBOL	PARAMETER	CONDITIONS T_A = 25°C; GND = 0V; V_{CC} = 5.0V		TYPICAL AC	TYPICAL ACT	UNIT
t_{PLH}/t_{PHL}	Propagation delay nI_0, nI_1 to nY	C_L = 50pF		3.9	5.7	ns
C_{PD}	Power dissipation capacitance per multiplexer[1]	f = 1MHz; C_L = 50pF	Enabled	37	41	pF
			Disabled	11	14	
C_{IN}	Input capacitance	V_I = 0V or V_{CC}		4.0	4.0	pF
C_{OUT}	Output capacitance	V_O = 0V or V_{CC}; Disabled		9.0	9.0	pF
I_{LATCH}	Latch-up current	Per Jedec JC40.2 Standard 17		500	500	mA

Note:

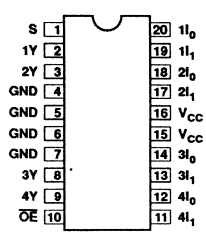
1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_I + \Sigma (C_L \times V_{CC}^2 \times f_O)$ where:
   f_I = input frequency in MHz, C_L = output load capacitance in pF,
   f_O = output frequency in MHz, V_{CC} = supply voltage in V,
   $\Sigma (C_L \times V_{CC}^2 \times f_O)$ = sum of outputs

ORDERING INFORMATION

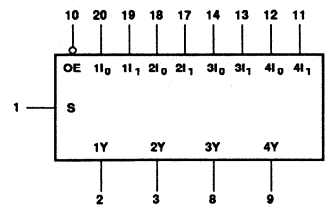
PACKAGES	TEMPERATURE RANGE	ORDER CODE
20-pin plastic DIP (300mil-wide)	-40°C to +85°C	74AC11257N 74ACT11257N
20-pin plastic SO (300mil-wide)	-40°C to +85°C	74AC11257D 74ACT11257D

PIN CONFIGURATION

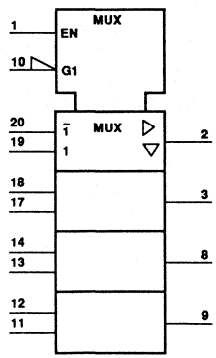
N and D Packages



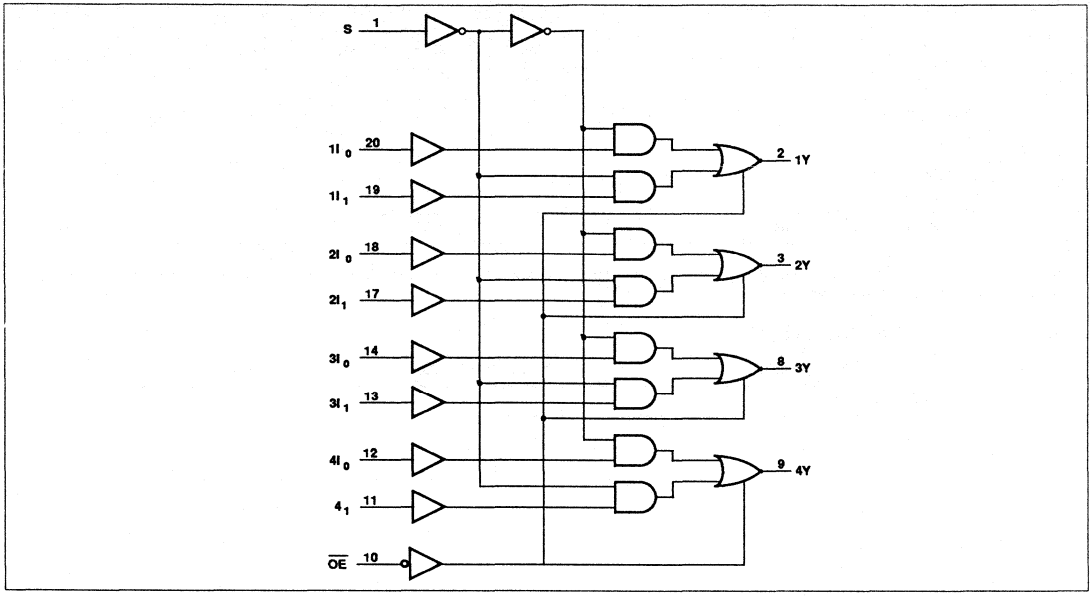
LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



LOGIC DIAGRAM



PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
1	S	Common select input
20, 18, 14, 12	$1I_0$ - $4I_0$	Data inputs
19, 17, 13, 11	$1I_1$ - $4I_1$	Data inputs
2, 3, 8, 9	1Y - 4Y	Data outputs
10	$\overline{OE}$	Output enable input
4, 5, 6, 7	GND	Ground (0V)
15, 16	V_{CC}	Positive supply voltage

FUNCTION TABLE

ENABLE	SELECT INPUT	DATA INPUTS		OUTPUT
$\overline{OE}$	S	nI_0	nI_1	nY
H	X	X	X	Z
L	L	L	X	L
L	L	H	X	H
L	H	X	L	L
L	H	X	H	H

H = High voltage level
L = Low voltage level
X = Don't care
Z = High-impedance (OFF) state

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	74AC11257			74ACT11257			UNIT
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	DC supply voltage	3.0[1]	5.0	5.5	4.5	5.0	5.5	V
V_I	Input voltage	0		V_{CC}	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	0		V_{CC}	V
$\Delta t/\Delta v$	Input transition rise or fall rate	0		10	0		10	ns/V
T_A	Operating free-air temperature	-40		+85	-40		+85	°C

NOTE:

1. No electrical or switching characteristics are specified at $V_{CC} < 3V$. Operation between 2V and 3V is not recommended, but within that range, a device output will maintain a previously established logic state.

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	TEST CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 to+7.0	V
I_{IK} or V_I	DC input diode current[2]	$V_I < 0$	-20	mA
		$V_I > V_{CC}$	20	
	DC input voltage		-0.5 to V_{CC} +0.5	V
I_{OK} or V_O	DC output diode current[2]	$V_O < 0$	-50	mA
		$V_O > V_{CC}$	50	
	DC output voltage		-0.5 to V_{CC} +0.5	V
I_O	DC output source or sink current per output pin	V_O = 0 to V_{CC}	±50	mA
I_{CC} or I_{GND}	DC V_{CC} current		±100	mA
	DC ground current		±100	
T_{STG}	Storage temperature		-65 to 150	°C
P_{TOT}	Power dissipation per package Plastic DIP	Above 70°C:derate linearly by 8mW/K	500	mW
	Power dissipation per package Plastic surface mount (SO)	Above 70°C:derate linearly by 6mW/K	400	mW

NOTES:

1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		V_{CC}	74AC11257				74ACT11257				UNIT
					T_A = +25°C		T_A = -40°C to +85°C		T_A = +25°C		T_A = -40°C to +85°C		
				V	Min	Max	Min	Max	Min	Max	Min	Max	
V_{IH}	High-level input voltage			3.0	2.10		2.10						V
				4.5	3.15		3.15		2.0		2.0		
				5.5	3.85		3.85		2.0		2.0		
V_{IL}	Low-level input voltage			3.0		0.90		0.90					V
				4.5		1.35		1.35		0.8		0.8	
				5.5		1.65		1.65		0.8		0.8	
V_{OH}	High-level output voltage	V_I = V_{IL} or V_{IH}	I_{OH} = -50μA	3.0	2.9		2.9						V
				4.5	4.4		4.4		4.4		4.4		
				5.5	5.4		5.4		5.4		5.4		
			I_{OH} = -4mA	3.0	2.58		2.48						
			I_{OH} = -24mA	4.5	3.94		3.8		3.94		3.8		
				5.5	4.94		4.8		4.94		4.8		
			I_{OH} = -75mA[1]	5.5			3.85				3.85		
V_{OL}	Low-level output voltage	V_I = V_{IL} or V_{IH}	I_{OL} = 50μA	3.0		0.1		0.1					V
				4.5		0.1		0.1		0.1		0.1	
				5.5		0.1		0.1		0.1		0.1	
			I_{OL} = 12mA	3.0		0.36		0.44					
			I_{OL} = 24mA	4.5		0.36		0.44		0.36		0.44	
				5.5		0.36		0.44		0.36		0.44	
			I_{OL} = 75mA[1]	5.5				1.65				1.65	
I_I	Input leakage current	V_I = V_{CC} or GND		5.5		±0.1		±1.0		±0.1		±1.0	μA
I_{OZ}	3-State output off-state current	V_I = V_{IL} or V_{IH}; V_O = V_{CC} or GND		5.5		±0.5		±5.0		±0.5		±5.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC} or GND, I_O = 0		5.5		8.0		80		8.0		80	μA
ΔI_{CC}	Supply current, TTL inputs High[2]	One input at 3.4V, other inputs at V_{CC} or GND		5.5						0.9		1.0	mA

NOTES:
1. Not more than one output should be tested at a time, and the duration of the test should not exceed 10ms.
2. This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0V or V_{CC}.

AC ELECTRICAL CHARACTERISTICS AT 3.3V ±0.3V

SYMBOL	PARAMETER	WAVEFORM	74AC11257					UNIT
			T_A = +25°C			T_A = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay nI_0, nI_1 to nY	1	1.5 1.5	5.6 6.2	8.1 9.0	1.5 1.5	8.9 10.1	ns
t_{PLH} t_{PHL}	Propagation delay S to nY	1	1.5 1.5	6.1 6.6	9.2 10.0	1.5 1.5	10.2 11.2	ns
t_{PZH} t_{PZL}	Output enable time to High and Low Level	2	1.5 1.5	5.6 7.5	8.2 10.4	1.5 1.5	9.1 11.8	ns
t_{PHZ} t_{PLZ}	Output disable time from High and Low Level	2	1.5 1.5	5.6 6.2	7.6 8.8	1.5 1.5	8.3 9.6	ns

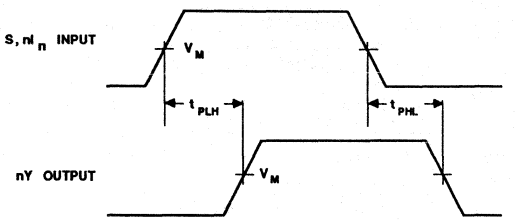
AC ELECTRICAL CHARACTERISTICS AT 5.0V ±0.5V

SYMBOL	PARAMETER	WAVEFORM	74AC11257					UNIT
			T_A = +25°C			T_A = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay nI_0, nI_1 to nY	1	1.5 1.5	3.6 4.1	5.8 6.5	1.5 1.5	6.4 7.2	ns
t_{PLH} t_{PHL}	Propagation delay S to nY	1	1.5 1.5	4.0 4.4	6.5 7.1	1.5 1.5	7.2 7.9	ns
t_{PZH} t_{PZL}	Output enable time to High and Low Level	2	1.5 1.5	3.8 5.0	5.9 7.6	1.5 1.5	6.5 8.6	ns
t_{PHZ} t_{PLZ}	Output disable time from High and Low Level	2	1.5 1.5	4.5 4.8	6.4 6.9	1.5 1.5	7.6 7.6	ns

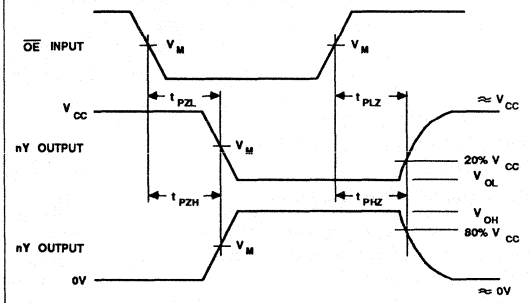
AC ELECTRICAL CHARACTERISTICS AT 5.0V ±0.5V

SYMBOL	PARAMETER	WAVEFORM	74ACT11257					UNIT
			T_A = +25°C			T_A = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay nI_0, nI_1 to nY	1	1.5 1.5	4.4 5.0	6.4 8.0	1.5 1.5	6.9 8.7	ns
t_{PLH} t_{PHL}	Propagation delay S to nY	1	1.5 1.5	4.7 5.7	7.6 8.5	1.5 1.5	8.2 9.4	ns
t_{PZH} t_{PZL}	Output enable time to High and Low Level	2	1.5 1.5	4.2 5.5	6.9 8.7	1.5 1.5	7.3 9.6	ns
t_{PHZ} t_{PLZ}	Output disable time from High and Low Level	2	1.5 1.5	5.7 6.0	7.6 7.9	1.5 1.5	8.4 8.5	ns

AC WAVEFORMS



Waveform 1. Waveforms Showing the Input (nI_n, S) to Output (nY) Propagation Delays

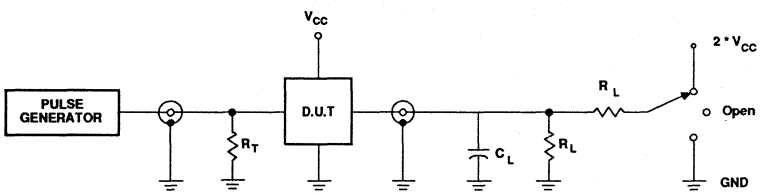


Waveform 2. Waveforms Showing the 3-State Output Enable and Disable Times

WAVEFORM CONDITIONS

	INPUTS	OUTPUTS
AC	V_{IN} = GND to V_{CC}, V_M = 50% V_{CC}	V_{OUT} = V_{OL} to V_{OH}
ACT	V_{IN} = GND to 3.0V, V_M = 1.5V	V_M = 50% V_{CC}

TEST CIRCUIT



Test Circuit

TEST	S1
t_{PLH}/t_{PHL}	Open
$t_{PLZ}t_{PZL}$	2*VCC
t_{PHZ}/t_{PZH}	GND

SWITCH POSITION

DEFINITIONS

C_L = Load capacitance, 50pF; includes jig and probe capacitance

R_L = Load resistor, 500Ω

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators

Input pulses: PRR ≤ 10MHz

$t_r = t_f$ = 3ns

74AC/ACT11258

Quad 2-Input Multiplexer (3-State), Inverting

Product Specification

FEATURES

- **Output capability: ±24 mA**
- **CMOS (AC) and TTL (ACT) voltage level inputs**
- **50Ω incident wave switching**
- **Center-pin V_{CC} and ground configuration to minimize high-speed switching noise**
- **I_{CC} category: MSI**

DESCRIPTION

The 74AC/ACT11258 high-performance CMOS devices combine very high speed and high output drive comparable to the most advanced TTL families.

The 74AC/ACT11258 provides four 2-to-1 multiplexers with 3-State inverting outputs which have a common selector and a common output enable. The state of the Select (S) input determines the particular register from which the data comes. The Output Enable ($\overline{OE}$) input is active-Low. When $\overline{OE}$ is High, all of the outputs ($\overline{Y}$) are forced to a High-impedance state regardless of all other input conditions.

The device is the logic implementation of a 4-pole, 2 position switch where the position of the switch is determined by the logic levels supplied to the Select input.

GENERAL INFORMATION

SYMBOL	PARAMETER	CONDITIONS T_A = 25°C; GND = 0V; V_{CC} = 5.0V		TYPICAL AC	TYPICAL ACT	UNIT
t_{PLH}/t_{PHL}	Propagation delay nI_0, nI_1 to $n\overline{Y}$	C_L = 50pF		3.6	5.6	ns
C_{PD}	Power dissipation capacitance per multiplexer[1]	f = 1MHz; C_L = 50pF	Enabled	33	35	pF
			Disabled	13	16	
C_{IN}	Input capacitance	V_I = 0V or V_{CC}		4.0	4.0	pF
C_{OUT}	Output capacitance	V_O = 0V or V_{CC}; Disabled		9.0	9.0	pF
I_{LATCH}	Latch-up current	Per Jedec JC40.2 Standard 17		500	500	mA

Note:

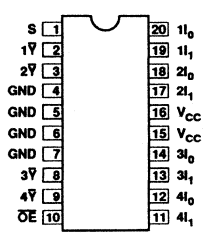
1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_I + \Sigma (C_L \times V_{CC}^2 \times f_O)$ where:
   f_I = input frequency in MHz, C_L = output load capacitance in pF,
   f_O = output frequency in MHz, V_{CC} = supply voltage in V,
   $\Sigma (C_L \times V_{CC}^2 \times f_O)$ = sum of outputs

ORDERING INFORMATION

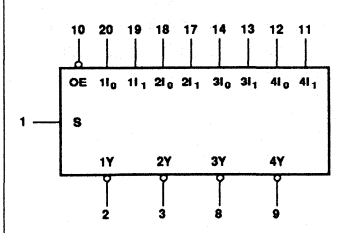
PACKAGES	TEMPERATURE RANGE	ORDER CODE
20-pin plastic DIP (300mil-wide)	-40°C to +85°C	74AC11258N 74ACT11258N
20-pin plastic SO (300mil-wide)	-40°C to +85°C	74AC11258D 74ACT11258D

PIN CONFIGURATION

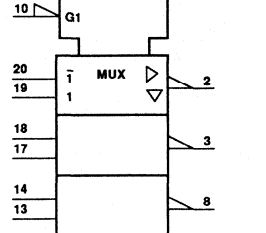
N and D Packages



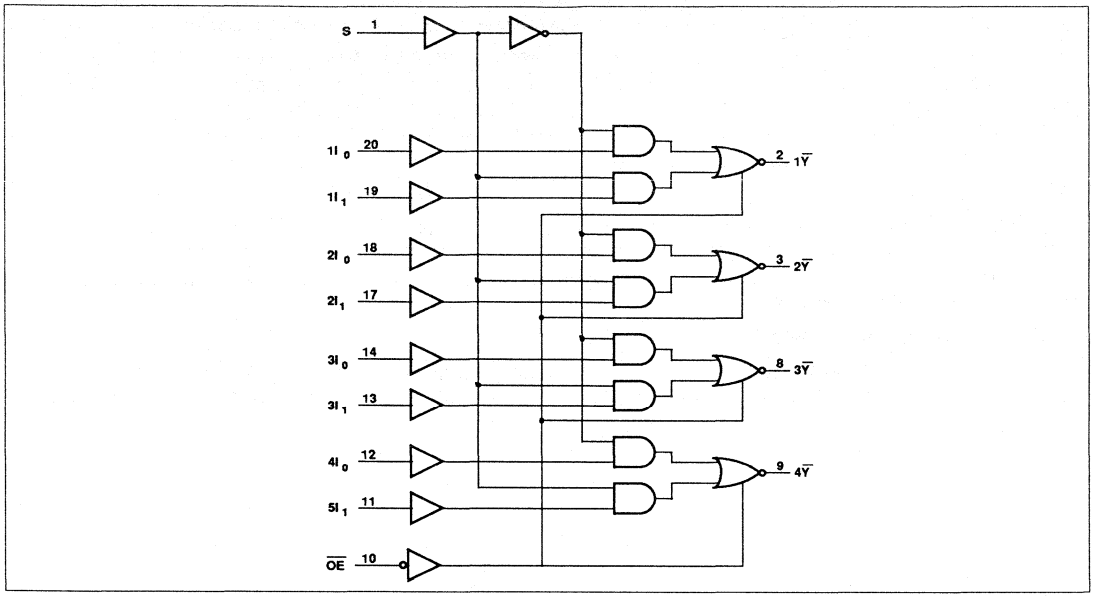
LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



LOGIC DIAGRAM



PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
1	S	Common select input
20, 18, 14, 12	nI_0 - nI_0	Data inputs
19, 17, 13, 11	nI_1 - nI_1	Data inputs
2, 3, 8, 9	$1\overline{Y}$ - $4\overline{Y}$	Data outputs
10	$\overline{OE}$	Output enable input
4, 5, 6, 7	GND	Ground (0V)
15, 16	V_{CC}	Positive supply voltage

FUNCTION TABLE

ENABLE	SELECT INPUT	DATA INPUTS		OUTPUT
$\overline{OE}$	S	nI_0	nI_1	$n\overline{Y}$
H	X	X	X	Z
L	L	L	X	H
L	L	H	X	L
L	H	X	L	H
L	H	X	H	L

H = High voltage level
L = Low voltage level
X = Don't care
Z = High-impedance (OFF) state

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	74AC11258			74ACT1258			UNIT
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	DC supply voltage	3.0[1]	5.0	5.5	4.5	5.0	5.5	V
V_I	Input voltage	0		V_{CC}	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	0		V_{CC}	V
$\Delta t/\Delta v$	Input transition rise or fall rate	0		10	0		10	ns/V
T_A	Operating free-air temperature	-40		+85	-40		+85	°C

NOTE:
1. No electrical or switching characteristics are specified at V_{CC} < 3V. Operation between 2V and 3V is not recommended, but within that range, a device output will maintain a previously established logic state.

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	TEST CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 to+7.0	V
I_{IK} or V_I	DC input diode current[2]	$V_I < 0$	-20	mA
		$V_I > V_{CC}$	20	
	DC input voltage		-0.5 to V_{CC} +0.5	V
I_{OK} or V_O	DC output diode current[2]	$V_O < 0$	-50	mA
		$V_O > V_{CC}$	50	
	DC output voltage		-0.5 to V_{CC} +0.5	V
I_O	DC output source or sink current per output pin	V_O = 0 to V_{CC}	±50	mA
I_{CC} or I_{GND}	DC V_{CC} current		±100	mA
	DC ground current		±100	
T_{STG}	Storage temperature		-65 to 150	°C
P_{TOT}	Power dissipation per package Plastic DIP	Above 70°C:derate linearly by 8mW/K	500	mW
	Power dissipation per package Plastic surface mount (SO)	Above 70°C:derate linearly by 6mW/K	400	mW

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		V_{CC}	74AC11258				74ACT11258				UNIT
					T_A = +25°C		T_A = -40°C to +85°C		T_A = +25°C		T_A = -40°C to +85°C		
				V	Min	Max	Min	Max	Min	Max	Min	Max	
V_{IH}	High-level input voltage			3.0	2.10		2.10						V
				4.5	3.15		3.15		2.0		2.0		
				5.5	3.85		3.85		2.0		2.0		
V_{IL}	Low-level input voltage			3.0		0.90		0.90					V
				4.5		1.35		1.35		0.8		0.8	
				5.5		1.65		1.65		0.8		0.8	
V_{OH}	High-level output voltage	V_I = V_{IL} or V_{IH}	I_{OH} = -50μA	3.0	2.9		2.9						V
				4.5	4.4		4.4		4.4		4.4		
				5.5	5.4		5.4		5.4		5.4		
			I_{OH} = -4mA	3.0	2.58		2.48						
			I_{OH} = -24mA	4.5	3.94		3.8		3.94		3.8		
				5.5	4.94		4.8		4.94		4.8		
			I_{OH} = -75mA[1]	5.5			3.85				3.85		
V_{OL}	Low-level output voltage	V_I = V_{IL} or V_{IH}	I_{OL} = 50μA	3.0		0.1		0.1					V
				4.5		0.1		0.1		0.1		0.1	
				5.5		0.1		0.1		0.1		0.1	
			I_{OL} = 12mA	3.0		0.36		0.44					
			I_{OL} = 24mA	4.5		0.36		0.44		0.36		0.44	
				5.5		0.36		0.44		0.36		0.44	
			I_{OL} = 75mA[1]	5.5				1.65				1.65	
I_I	Input leakage current	V_I = V_{CC} or GND		5.5		±0.1		±1.0		±0.1		±1.0	μA
I_{OZ}	3-State output off-state current	V_I = V_{IL} or V_{IH}; V_O = V_{CC} or GND		5.5		±0.5		±5.0		±0.5		±5.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC} or GND, I_O = 0		5.5		8.0		80		8.0		80	μA
ΔI_{CC}	Supply current, TTL inputs High[2]	One input at 3.4V, other inputs at V_{CC} or GND		5.5						0.9		1.0	mA

NOTES:
1. Not more than one output should be tested at a time, and the duration of the test should not exceed 10ms.
2. This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0V or V_{CC}.

AC ELECTRICAL CHARACTERISTICS AT 3.3V ±0.3V

SYMBOL	PARAMETER	WAVEFORM	74AC11258					UNIT
			T_A = +25°C			T_A = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay nI_0, nI_1 to $n\overline{Y}$	1	1.5 1.5	5.3 6.0	7.0 7.9	1.5 1.5	7.7 9.2	ns
t_{PLH} t_{PHL}	Propagation delay S to $n\overline{Y}$	1	1.5 1.5	5.6 6.7	7.9 9.1	1.5 1.5	8.7 10.1	ns
t_{PZH} t_{PZL}	Output enable time to High and Low Level	2	1.5 1.5	5.3 6.8	7.1 9.1	1.5 1.5	7.7 10.2	ns
t_{PHZ} t_{PLZ}	Output disable time from High and Low Level	2	1.5 1.5	5.4 6.0	6.9 7.8	1.5 1.5	7.4 8.4	ns

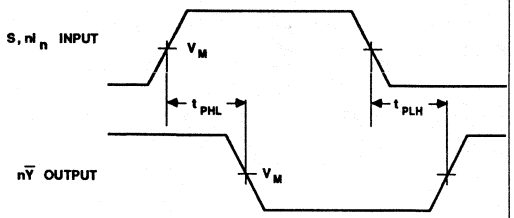
AC ELECTRICAL CHARACTERISTICS AT 5.0V ±0.5V

SYMBOL	PARAMETER	WAVEFORM	74AC11258					UNIT
			T_A = +25°C			T_A = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay nI_0, nI_1 to $n\overline{Y}$	1	1.5 1.5	3.3 4.0	5.0 6.1	1.5 1.5	5.4 6.8	ns
t_{PLH} t_{PHL}	Propagation delay S to $n\overline{Y}$	1	1.5 1.5	3.6 4.4	5.8 6.7	1.5 1.5	6.3 7.5	ns
t_{PZH} t_{PZL}	Output enable time to High and Low Level	2	1.5 1.5	3.5 4.5	5.3 6.8	1.5 1.5	5.7 7.5	ns
t_{PHZ} t_{PLZ}	Output disable time from High and Low Level	2	1.5 1.5	4.5 4.7	61 6.4	1.5 1.5	6.5 6.9	ns

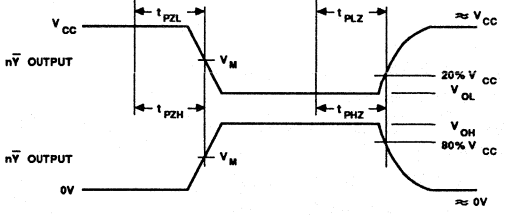
AC ELECTRICAL CHARACTERISTICS AT 5.0V ±0.5V

SYMBOL	PARAMETER	WAVEFORM	74ACT11258					UNIT
			T_A = +25°C			T_A = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay nI_0, nI_1 to $n\overline{Y}$	1	1.5 1.5	5.4 5.7	7.7 7.7	1.5 1.5	8.5 8.7	ns
t_{PLH} t_{PHL}	Propagation delay S to $n\overline{Y}$	1	1.5 1.5	5.7 6.7	8.0 9.4	1.5 1.5	8.8 10.4	ns
t_{PZH} t_{PZL}	Output enable time to High and Low Level	2	1.5 1.5	5.3 6.4	7.2 8.8	1.5 1.5	7.7 9.8	ns
t_{PHZ} t_{PLZ}	Output disable time from High and Low Level	2	1.5 1.5	6.1 6.3	7.5 8.3	1.5 1.5	7.7 9.0	ns

AC WAVEFORMS



Waveform 1. Waveforms Showing the Input (nI_n, S) to Output ($n\bar{Y}$) Propagation Delays

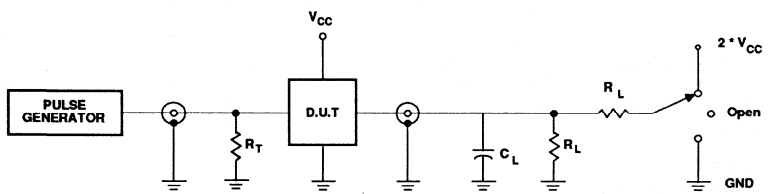


Waveform 2. Waveforms Showing the 3-State Output Enable and Disable Times

WAVEFORM CONDITIONS

	INPUTS	OUTPUTS
AC	V_{IN} = GND to V_{CC}, V_M = 50% V_{CC}	V_{OUT} = V_{OL} to V_{OH}
ACT	V_{IN} = GND to 3.0V, V_M = 1.5V	V_M = 50% V_{CC}

TEST CIRCUIT



Test Circuit

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2*VCC
t_{PHZ}/t_{PZH}	GND

SWITCH POSITION

DEFINITIONS

C_L = Load capacitance, 50pF; includes jig and probe capacitance

R_L = Load resistor, 500Ω

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators

Input pulses: PRR ≤ 10MHz

$t_r = t_f$ = 3ns

74AC/ACT11269

Synchronous Presettable 8-Bit Binary Up/Down Counter

Objective Specification

FEATURES

- **Synchronous counting and loading**
- **Up/Down counting**
- **Two Count Enable inputs for n-bit cascading**
- **Positive edge-triggered Clock**
- **Glitchless Terminal Count output**
- **Built-in look-ahead carry capability**
- **Presettable for programmable operation**
- **Output capability: ±24mA**
- **CMOS (AC) and TTL (ACT) voltage level inputs**
- **50Ω incident wave switching**
- **Center-pin V_{CC} and ground configuration to minimize high-speed switching noise**
- **I_{CC} category: MSI**

DESCRIPTION

The 74AC/ACT11269 high-performance CMOS devices combine very high speed and high output drive comparable to the most advanced TTL families.

The AC/ACT11269 is a synchronous, presettable 8-bit up/down binary counter featuring an internal Carry look-ahead for

GENERAL INFORMATION

SYMBOL	PARAMETER	CONDITIONS T_A = 25°C; GND = 0V; V_{CC} = 5.0V	TYPICAL AC	TYPICAL ACT	UNIT
t_{PLH}/t_{PHL}	Propagation delay CP to Q_n ($\overline{PE}$ = High)	C_L = 50pF	5.7	7.4	ns
C_{PD}	Power dissipation capacitance[1]	f = 1MHz; C_L = 50pF	215	200	pF
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	4.5	4.5	pF
I_{LATCH}	Latch-up current	Per Jedec JC40.2 Standard 17	500	500	mA
f_{MAX}	Maximum clock frequency	C_L = 50pF	160	150	MHz

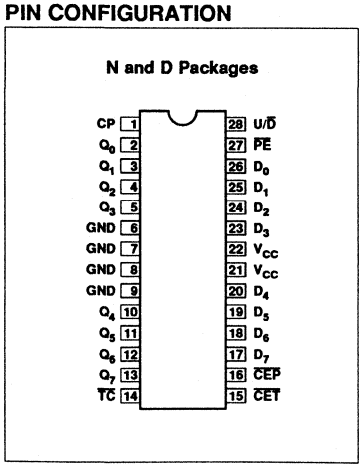
Note:

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_I + \Sigma (C_L \times V_{CC}^2 \times f_O)$ where:
   f_I = input frequency in MHz, C_L = output load capacitance in pF,
   f_O = output frequency in MHz, V_{CC} = supply voltage in V,
   $\Sigma (C_L \times V_{CC}^2 \times f_O)$ = sum of outputs

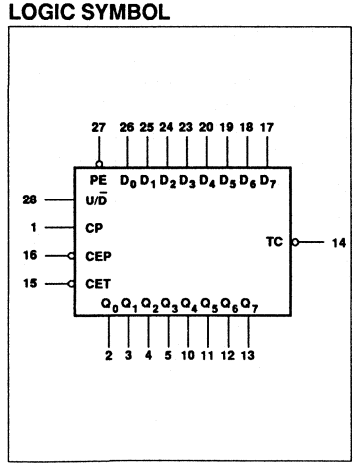
ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE
28-pin plastic DIP (300mil-wide)	-40°C to +85°C	74AC11269N 74ACT11269N
28-pin plastic SO (300mil-wide)	-40°C to +85°C	74AC11269D 74ACT11269D

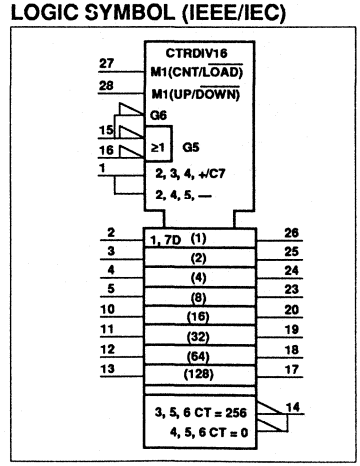
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



applications in high-speed counting designs. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when so instructed by the Count Enable inputs and internal gating. This mode of operation eliminates the output spikes which are normally associated with asynchronous (ripple clock) counters. A buffered Clock input triggers the flip-flops on the Low-to-High transition of the clock.

The counter is fully programmable; that is, the outputs may be preset to either level.

Presetting is synchronous with the clock and takes place regardless of the level of the Count Enable inputs. A Low level on the Parallel Enable ($\overline{PE}$) input disables the counter and causes the data at the D_n input to be loaded into the counter on the next Low-to-High transition of the clock.

The direction of counting is controlled by the Up/Down (U/$\overline{D}$) input; a High will cause the count to increase, a Low will cause the count to decrease.

The Carry look-ahead circuitry provides for cascading counters for n-bit synchronous applications without additional gating. Instrumental in accomplishing this function are two Count Enable inputs ($\overline{CET}$•$\overline{CEP}$) and a Terminal Count ($\overline{TC}$) output. Both Count Enable inputs must be Low to count. The $\overline{CET}$ input is fed forward to enable the $\overline{TC}$ output. The $\overline{TC}$ output thus enabled will produce a Low output pulse with a duration approximately equal to the High level portion or the Low level portion of the Q_0 output depending on the state of the U/$\overline{D}$ input. This Low level $\overline{TC}$ pulse is used to enable successive cascaded stages.

FUNCTIONAL DESCRIPTION

The AC/ACT11269 uses edge-triggered D-type flip-flops and has no constraints on changing the control or data input signals in either state of the Clock. The only requirement is that the various inputs attain the desired state at least a setup time before the rising edge of the Clock and remain valid for the recommended hold time thereafter. The parallel load operation takes precedence over the other operations, as indicated in the Mode Select Table. When $\overline{PE}$ is Low, the data on the D_0 - D_7 inputs enter the flip-flops on the next rising edge of the Clock. In order for counting to occur, both $\overline{CEP}$ and $\overline{CET}$ must be Low and $\overline{PE}$ must be High; the U/$\overline{D}$ input then determines the direction of counting. The Terminal Count ($\overline{TC}$) output is normally High and goes Low when a counter reaches zero in the Count Down mode or reaches 15 in the Count Up mode, provided that $\overline{CET}$ is Low. The $\overline{TC}$ output state is not a function of the Count Enable Parallel ($\overline{CEP}$) input level. The $\overline{TC}$ signal is derived by decoding the D-input signals of the counter flip-flops and using this decoded signal as the D-input driving the $\overline{TC}$ output. Use of this configuration gives a $\overline{TC}$ output which is free of decoding spikes. The possibility exists that on pwer-up that the $\overline{TC}$ output may not give a true indication of the state of the counter (i.e., $\overline{TC}$ may be Low while the counter is not at terminal count or High when it is at terminal count.) Should this occur, $\overline{TC}$ will always go to a correct state on the first Low-to-High transition of the clock.

PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
27	$\overline{PE}$	Parallel enable input
1	CP	Clock input
28	U/$\overline{D}$	Up-Down count control input
16	$\overline{CEP}$	Count enable parallel input (active-Low)
15	$\overline{CET}$	Count enable trickle input (active-Low)
26, 25, 24, 23, 20, 19, 18, 17	D_0 -D_7	Parallel data inputs
2, 3, 4, 5, 10, 11, 12, 13	Q_0 - Q_7	Flip-flop outputs
14	$\overline{TC}$	Terminal count output (active-Low)
6, 7, 8, 9	GND	Ground (0V)
21, 22	V_{CC}	Positive supply voltage

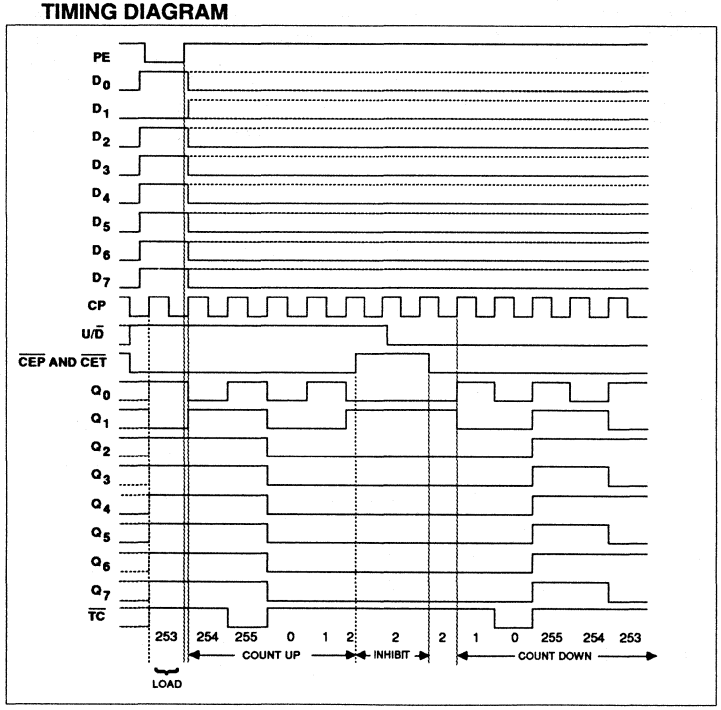
MODE SELECT—FUNCTION TABLE

OPERATING MODE	INPUTS						OUTPUTS	
	CP	U/$\overline{D}$	$\overline{CEP}$	$\overline{CET}$	$\overline{PE}$	D_n	Q_n	$\overline{TC}$
Parallel load	↑	X	X	X	l	l	L	(1)
	↑	X	X	X	l	h	H	(1)
Count up	↑	h	l	l	h	X	Count up	(1)
Count down	↑	l	l	l	h	X	Count down	(1)
Hold (do nothing)	↑	X	h	X	h	X	q_n	(1)
	↑	X	X	h	h	X	q_n	H

H = High voltage level steady state
h = High voltage level one setup time prior to the Low-to-High clock transition
L = Low voltage level steady state
l = Low voltage level one setup time prior to the Low-to-High clock transition
X = Don't care
q = State of the referenced output prior to the Low-to-High clock transition
↑ =Low-to-High clock transition

NOTES:
1. $\overline{TC}$ is Low when $\overline{CET}$ is Low and the counter is at Terminal Count. Terminal Count Up is with all Q_n outputs High and Terminal Count Down is with all Q_n outputs Low.

TIMING DIAGRAM



RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	74AC11269			74ACT11269			UNIT
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	DC supply voltage	3.0[1]	5.0	5.5	4.5	5.0	5.5	V
V_I	Input voltage	0		V_{CC}	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	0		V_{CC}	V
$\Delta t/\Delta v$	Input transition rise or fall rate	0		10	0		10	ns/V
T_A	Operating free-air temperature	-40		+85	-40		+85	°C

NOTE:

1. No electrical or switching characteristics are specified at $V_{CC} < 3V$. Operation between 2V and 3V is not recommended, but within that range, a device output will maintain a previously established logic state.

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	TEST CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 to+7.0	V
I_{IK} or V_I	DC input diode current[2]	$V_I < 0$	-20	mA
		$V_I > V_{CC}$	20	
	DC input voltage		-0.5 to V_{CC} +0.5	V
I_{OK} or V_O	DC output diode current[2]	$V_O < 0$	-50	mA
		$V_O > V_{CC}$	50	
	DC output voltage		-0.5 to V_{CC} +0.5	V
I_O	DC output source or sink current per output pin	V_O = 0 to V_{CC}	±50	mA
I_{CC} or I_{GND}	DC V_{CC} current		±225	mA
	DC ground current		±225	
T_{STG}	Storage temperature		-65 to 150	°C
P_{TOT}	Power dissipation per package Plastic DIP	Above 70°C:derate linearly by 8mW/K	500	mW
	Power dissipation per package Plastic surface mount (SO)	Above 70°C:derate linearly by 6mW/K	400	mW

NOTES:

1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

Synchronous Presettable 8-Bit Binary Up/Down Counter

74AC/ACT11269

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		V_{CC}	74AC11269				74ACT11269				UNIT
					T_A = +25°C		T_A = -40°C to +85°C		T_A = +25°C		T_A = -40°C to +85°C		
				V	Min	Max	Min	Max	Min	Max	Min	Max	
V_{IH}	High-level input voltage			3.0	2.10		2.10						V
				4.5	3.15		3.15		2.0		2.0		
				5.5	3.85		3.85		2.0		2.0		
V_{IL}	Low-level input voltage			3.0		0.90		0.90					V
				4.5		1.35		1.35		0.8		0.8	
				5.5		1.65		1.65		0.8		0.8	
V_{OH}	High-level output voltage	V_I = V_{IL} or V_{IH}	I_{OH} = -50μA	3.0	2.9		2.9						V
				4.5	4.4		4.4		4.4		4.4		
				5.5	5.4		5.4		5.4		5.4		
			I_{OH} = -4mA	3.0	2.58		2.48						
			I_{OH} = -24mA	4.5	3.94		3.8		3.94		3.8		
				5.5	4.94		4.8		4.94		4.8		
			I_{OH} = -75mA[1]	5.5			3.85				3.85		
V_{OL}	Low-level output voltage	V_I = V_{IL} or V_{IH}	I_{OL} = 50μA	3.0		0.1		0.1					V
				4.5		0.1		0.1		0.1		0.1	
				5.5		0.1		0.1		0.1		0.1	
			I_{OL} = 12mA	3.0		0.36		0.44					
			I_{OL} = 24mA	4.5		0.36		0.44		0.36		0.44	
				5.5		0.36		0.44		0.36		0.44	
			I_{OL} = 75mA[1]	5.5				1.65				1.65	
I_I	Input leakage current	V_I = V_{CC} or GND		5.5		±0.1		±1.0		±0.1		±1.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC} or GND, I_O = 0		5.5		8.0		80		8.0		80	μA
ΔI_{CC}	Supply current, TTL inputs High[2]	One input at 3.4V, other inputs at V_{CC} or GND		5.5						0.9		1.0	mA

NOTES:
1. Not more than one output should be tested at a time, and the duration of the test should not exceed 10ms.
2. This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0V or V_{CC}.

74AC/ACT11273

Octal D-Type Flip-Flop with Reset

Objective Specification

FEATURES

- **Eight edge-triggered D-type flip-flops**
- **Buffered common clock**
- **Buffered, asynchronous Master Reset**
- **Output capability: ±24 mA**
- **CMOS (AC) and TTL (ACT) voltage level inputs**
- **50Ω incident wave switching**
- **Center-pin V_{CC} and ground configuration to minimize high-speed switching noise**
- **I_{CC} category: MSI**

DESCRIPTION

The 74AC/ACT11273 high-performance CMOS devices combine very high speed and high output drive comparable to the most advanced TTL families.

The 74AC/ACT11273 provides eight positive edge-triggered D-type flip-flops with individual Data inputs and Q outputs. The common buffered Clock (CP) and Master Reset ($\overline{MR}$) inputs load and reset (clear) all flip-flops simultaneously.

All outputs will be forced Low independently of Clock or Data inputs by a Low voltage level on the MR input. The device is useful for applications where the true output only is required and the Clock and Master Reset are common to all storage elements.

GENERAL INFORMATION

SYMBOL	PARAMETER	CONDITIONS T_A = 25°C; GND = 0V; V_{CC} = 5.0V	TYPICAL		UNIT
			AC	ACT	
t_{PLH}/t_{PHL}	Propagation delay CP to Q_n	C_L = 50pF			ns
C_{PD}	Power dissipation capacitance per flip-flop[1]	f = 1MHz; C_L = 50pF			pF
C_{IN}	Input capacitance	V_I = 0V or V_{CC}			pF
I_{LATCH}	Latch-up current	Per Jedec JC40.2 Standard 17			mA
f_{MAX}	Maximum clock frequency	C_L = 50pF			MHz

Note:

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):

   $P_D = C_{PD} \times V_{CC}^2 \times f_I + \Sigma (C_L \times V_{CC}^2 \times f_O)$ where:

   f_I = input frequency in MHz, C_L = output load capacitance in pF,

   f_O = output frequency in MHz, V_{CC} = supply voltage in V,

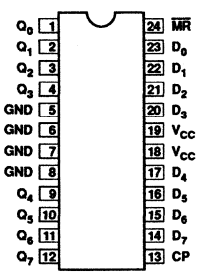
   $\Sigma (C_L \times V_{CC}^2 \times f_O)$ = sum of outputs

ORDERING INFORMATION

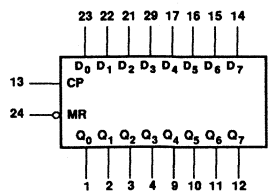
PACKAGES	TEMPERATURE RANGE	ORDER CODE
24-pin plastic DIP (300mil-wide)	-40°C to +85°C	74AC11273N 74ACT11273N
24-pin plastic SO (300mil-wide)	-40°C to +85°C	74AC 273D 74AC 273D

PIN CONFIGURATION

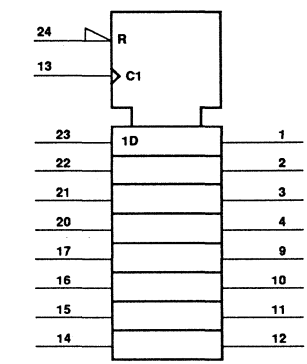
N and D Packages



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



PIN DESCRIPTION

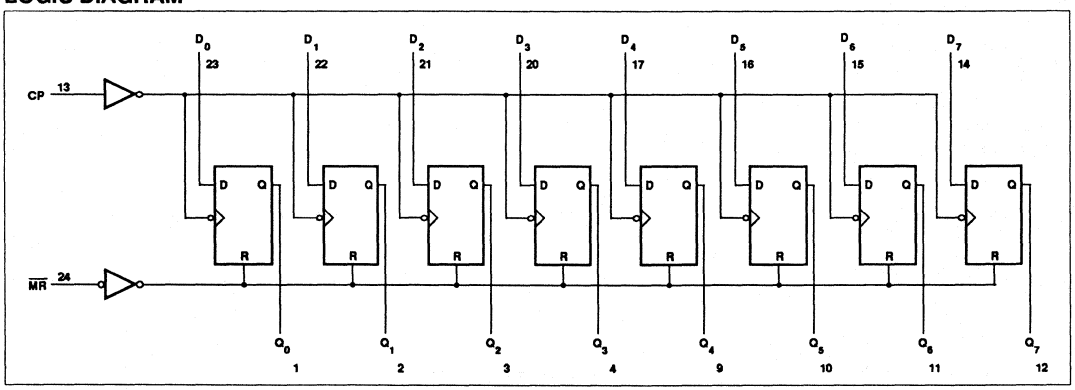
PIN NUMBER	SYMBOL	NAME AND FUNCTION
24	$\overline{MR}$	Master reset (active-Low)
13	CP	Clock pulse input
23, 22, 21, 20, 17, 16, 15, 14	D_0 - D_7	Data inputs
1, 2, 3, 4, 9, 10, 11, 12	Q_0 - Q_7	Data outputs
5, 6, 7, 8	GND	Ground (0V)
18, 19	V_{CC}	Positive supply voltage

MODE SELECT—FUNCTION TABLE

OPERATING MODE	INPUTS			OUTPUTS
	$\overline{MR}$	CP	D_n	Q_n
Reset (clear)	L	X	X	L
Load "1"	H	↑	h	H
Load "0"	H	↑	l	L

H = High voltage level steady state
h = High voltage level one setup time prior to the Low-to-High clock transition
L = Low voltage level steady state
l = Low voltage level one setup time prior to the Low-to-High clock transition
X = Don't care
↑ =Low-to-High clock transition

LOGIC DIAGRAM



RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	74AC11273			74ACT11273			UNIT
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	DC supply voltage	3.0[1]	5.0	5.5	4.5	5.0	5.5	V
V_I	Input voltage	0		V_{CC}	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	0		V_{CC}	V
$\Delta t/\Delta v$	Input transition rise or fall rate	0		10	0		10	ns/V
T_A	Operating free-air temperature	-40		+85	-40		+85	°C

NOTE:

1. No electrical or switching characteristics are specified at $V_{CC} < 3V$. Operation between 2V and 3V is not recommended, but within that range, a device output will maintain a previously established logic state.

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	TEST CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 to+7.0	V
I_{IK} or V_I	DC input diode current[2]	$V_I < 0$	-20	mA
		$V_I > V_{CC}$	20	
	DC input voltage		-0.5 to V_{CC} +0.5	V
I_{OK} or V_O	DC output diode current[2]	$V_O < 0$	-50	mA
		$V_O > V_{CC}$	50	
	DC output voltage		-0.5 to V_{CC} +0.5	V
I_O	DC output source or sink current per output pin	V_O = 0 to V_{CC}	±50	mA
I_{CC} or I_{GND}	DC V_{CC} current		±200	mA
	DC ground current		±200	
T_{STG}	Storage temperature		-65 to 150	°C
P_{TOT}	Power dissipation per package Plastic DIP	Above 70°C:derate linearly by 8mW/K	500	mW
	Power dissipation per package Plastic surface mount (SO)	Above 70°C:derate linearly by 6mW/K	400	mW

NOTES:

1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		V_{CC}	74AC11273				74ACT11273				UNIT
					T_A = +25°C		T_A = -40°C to +85°C		T_A = +25°C		T_A = -40°C to +85°C		
				V	Min	Max	Min	Max	Min	Max	Min	Max	
V_{IH}	High-level input voltage			3.0	2.10		2.10						V
				4.5	3.15		3.15		2.0		2.0		
				5.5	3.85		3.85		2.0		2.0		
V_{IL}	Low-level input voltage			3.0		0.90		0.90					V
				4.5		1.35		1.35		0.8		0.8	
				5.5		1.65		1.65		0.8		0.8	
V_{OH}	High-level output voltage	V_I = V_{IL} or V_{IH}	I_{OH} = -50µA	3.0	2.9		2.9						V
				4.5	4.4		4.4		4.4		4.4		
				5.5	5.4		5.4		5.4		5.4		
			I_{OH} = -4mA	3.0	2.58		2.48						
			I_{OH} = -24mA	4.5	3.94		3.8		3.94		3.8		
				5.5	4.94		4.8		4.94		4.8		
			I_{OH} = -75mA[1]	5.5			3.85				3.85		
V_{OL}	Low-level output voltage	V_I = V_{IL} or V_{IH}	I_{OL} = 50µA	3.0		0.1		0.1					V
				4.5		0.1		0.1		0.1		0.1	
				5.5		0.1		0.1		0.1		0.1	
			I_{OL} = 12mA	3.0		0.36		0.44					
			I_{OL} = 24mA	4.5		0.36		0.44		0.36		0.44	
				5.5		0.36		0.44		0.36		0.44	
			I_{OL} = 75mA[1]	5.5				1.65				1.65	
I_I	Input leakage current	V_I = V_{CC} or GND		5.5		±0.1		±1.0		±0.1		±1.0	µA
I_{CC}	Quiescent supply current	V_I = V_{CC} or GND, I_O = 0		5.5		8.0		80		8.0		80	µA
ΔI_{CC}	Supply current, TTL inputs High[2]	One input at 3.4V, other inputs at V_{CC} or GND		5.5						0.9		1.0	mA

NOTES:
1. Not more than one output should be tested at a time, and the duration of the test should not exceed 10ms.
2. This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0V or V_{CC}.

74AC/ACT11280

9-Bit Odd/Even Parity Generator/Checker

Product Specification

FEATURES

- **Word length easily expanded by cascading**
- **Output capability: ±24mA**
- **CMOS (AC) and TTL (ACT) voltage level inputs**
- **50Ω incident wave switching**
- **Center-pin V_{CC} and ground configuration to minimize high-speed switching noise**
- **I_{CC} category: MSI**

DESCRIPTION

The 74AC/ACT11280 high-performance CMOS devices combine very high speed and high output drive comparable to the most advanced TTL families.

The 74AC/ACT11280 9-bit parity generator or checker is commonly used to detect errors in high-speed data transmission or data retrieval systems. Both Even and Odd parity outputs are available for generating or checking even or odd parity on up to 9 bits.

The Even parity output (Σ_E) is High when an even number of Data inputs (I_0 - I_8) are High. The Odd parity output (Σ_O) is High when an odd number of Data inputs are High.

GENERAL INFORMATION

SYMBOL	PARAMETER	CONDITIONS T_A = 25°C; GND = 0V; V_{CC} = 5.0V	TYPICAL		UNIT
			AC	ACT	
t_{PLH}/ t_{PHL}	Propagation delay I_n to Σ_n	C_L = 50pF	6.4	7.3	ns
C_{PD}	Power dissipation capacitance[1]	f = 1MHz; C_L = 50pF	55	65	pF
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	3.5	3.5	pF
I_{LATCH}	Latch-up current	Per Jedec JC40.2 Standard 17	500	500	mA

Note:

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_I + \Sigma (C_L \times V_{CC}^2 \times f_O)$ where:
   f_I = input frequency in MHz, C_L = output load capacitance in pF,
   f_O = output frequency in MHz, V_{CC} = supply voltage in V,
   $\Sigma (C_L \times V_{CC}^2 \times f_O)$ = sum of outputs

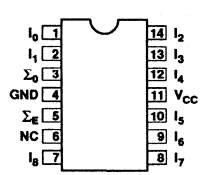
ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE
14-pin plastic DIP (300mil-wide)	-40°C to +85°C	74AC11280N 74ACT11280N
14-pin plastic SO (150mil-wide)	-40°C to +85°C	74AC11280D 74ACT11280D

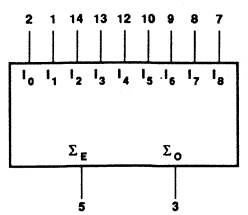
Expansion to larger word sizes is accomplished by tying the Even outputs of up to nine parallel devices to the data inputs of the final stage.

PIN CONFIGURATION

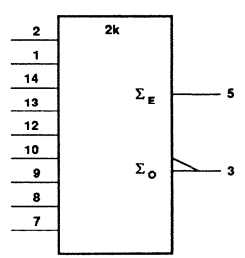
N and D Packages



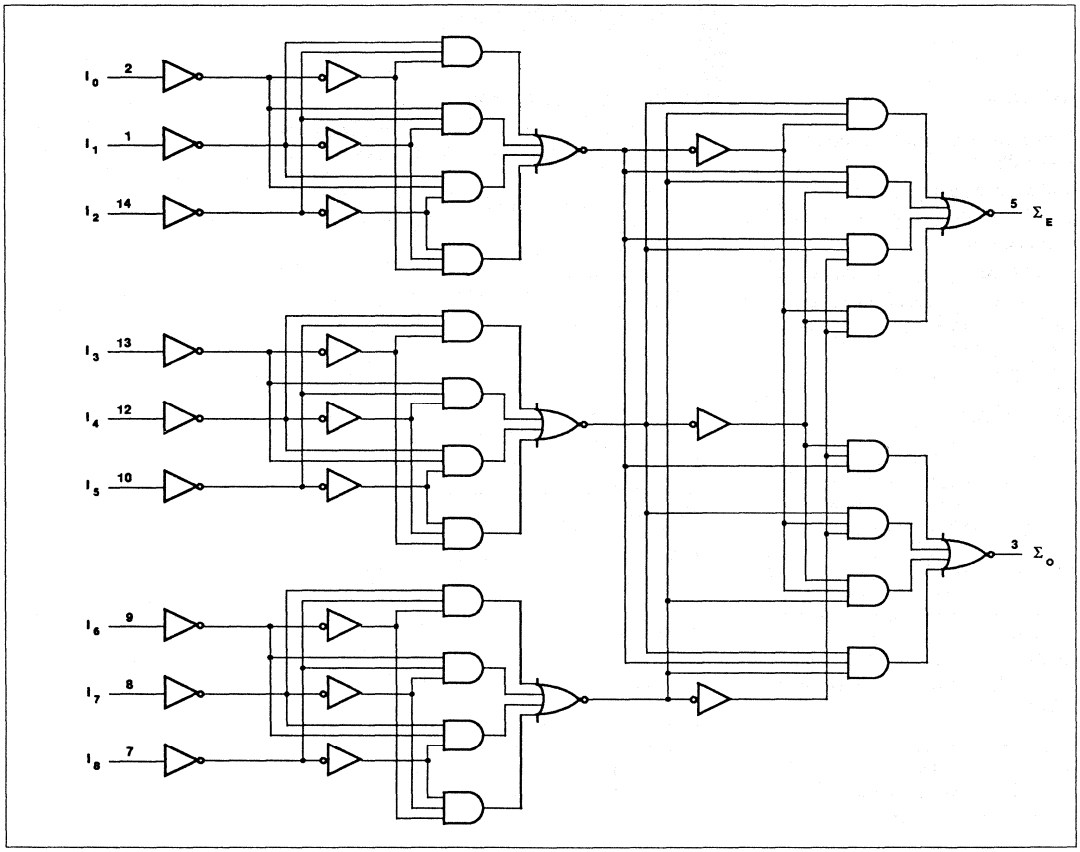
LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



LOGIC DIAGRAM



PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
2, 1, 14, 13, 12, 10, 9, 8, 7	I_0 - I_8	Data inputs
5	Σ_E	Even parity output
3	Σ_O	Odd parity output
4	GND	Ground (0V)
11	V_{CC}	Positive supply voltage

FUNCTION TABLE

INPUTS	OUTPUTS	
Number of High Data Inputs (I_0 - I_8)	Σ_E	Σ_O
Even - 0, 2, 4, 6, 8	H	L
Odd - 1, 3, 5, 7, 9	L	H

H = High voltage level
L = Low voltage level

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	74AC11280			74ACT11280			UNIT
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	DC supply voltage	3.0[1]	5.0	5.5	4.5	5.0	5.5	V
V_I	Input voltage	0		V_{CC}	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	0		V_{CC}	V
$\Delta t/\Delta v$	Input transition rise or fall rate	0		10	0		10	ns/V
T_A	Operating free-air temperature	-40		+85	-40		+85	°C

NOTE:
1. No electrical or switching characteristics are specified at V_{CC} < 3V. Operation between 2V and 3V is not recommended, but within that range, a device output will maintain a previously established logic state.

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	TEST CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 to+7.0	V
I_{IK} or V_I	DC input diode current[2]	$V_I < 0$	-20	mA
		$V_I > V_{CC}$	20	
	DC input voltage		-0.5 to V_{CC} +0.5	V
I_{OK} or V_O	DC output diode current[2]	$V_O < 0$	-50	mA
		$V_O > V_{CC}$	50	
	DC output voltage		-0.5 to V_{CC} +0.5	V
I_O	DC output source or sink current per output pin	V_O = 0 to V_{CC}	±50	mA
I_{CC} or I_{GND}	DC V_{CC} current		±100	mA
	DC ground current		±100	
T_{STG}	Storage temperature		-65 to 150	°C
P_{TOT}	Power dissipation per package Plastic DIP	Above 70°C:derate linearly by 8mW/K	500	mW
	Power dissipation per package Plastic surface mount (SO)	Above 70°C:derate linearly by 6mW/K	400	mW

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		V_{CC}	74AC11280				74ACT11280				UNIT
					T_A = +25°C		T_A = -40°C to +85°C		T_A = +25°C		T_A = -40°C to +85°C		
				V	Min	Max	Min	Max	Min	Max	Min	Max	
V_{IH}	High-level input voltage			3.0	2.10		2.10						V
				4.5	3.15		3.15		2.0		2.0		
				5.5	3.85		3.85		2.0		2.0		
V_{IL}	Low-level input voltage			3.0		0.90		0.90					V
				4.5		1.35		1.35		0.8		0.8	
				5.5		1.65		1.65		0.8		0.8	
V_{OH}	High-level output voltage	V_I = V_{IL} or V_{IH}	I_{OH} = -50μA	3.0	2.9		2.9						V
				4.5	4.4		4.4		4.4		4.4		
				5.5	5.4		5.4		5.4		5.4		
			I_{OH} = -4mA	3.0	2.58		2.48						
			I_{OH} = -24mA	4.5	3.94		3.8		3.94		3.8		
				5.5	4.94		4.8		4.94		4.8		
			I_{OH} = -75mA[1]	5.5			3.85				3.85		
V_{OL}	Low-level output voltage	V_I = V_{IL} or V_{IH}	I_{OL} = 50μA	3.0		0.1		0.1					V
				4.5		0.1		0.1		0.1		0.1	
				5.5		0.1		0.1		0.1		0.1	
			I_{OL} = 12mA	3.0		0.36		0.44					
			I_{OL} = 24mA	4.5		0.36		0.44		0.36		0.44	
				5.5		0.36		0.44		0.36		0.44	
			I_{OL} = 75mA[1]	5.5				1.65				1.65	
I_I	Input leakage current	V_I = V_{CC} or GND		5.5		±0.1		±1.0		±0.1		±1.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC} or GND, I_O = 0		5.5		8.0		80		8.0		80	μA
ΔI_{CC}	Supply current, TTL inputs High[2]	One input at 3.4V, other inputs at V_{CC} or GND		5.5						0.9		1.0	mA

NOTES:
1. Not more than one output should be tested at a time, and the duration of the test should not exceed 10ms.
2. This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0V or V_{CC}.

AC ELECTRICAL CHARACTERISTICS AT 3.3V ±0.3V

SYMBOL	PARAMETER	WAVEFORM	74AC11280					UNIT
			T_A = +25°C			T_A = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay I_n to Σ_E	1	1.5 1.5	9.8 10.5	13.5 13.9	1.5 1.5	14.9 15.4	ns
t_{PLH} t_{PHL}	Propagation delay I_n to Σ_O	1	1.5 1.5	9.9 10.6	13.8 14.4	1.5 1.5	15.1 15.6	ns

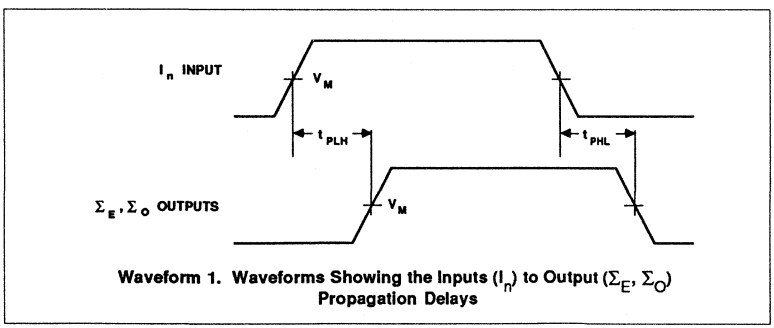
AC ELECTRICAL CHARACTERISTICS AT 5.0V ±0.5V

SYMBOL	PARAMETER	WAVEFORM	74AC11280					UNIT
			T_A = +25°C			T_A = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay I_n to Σ_E	1	1.5 1.5	5.9 6.7	9.1 9.9	1.5 1.5	10.1 10.9	ns
t_{PLH} t_{PHL}	Propagation delay I_n to Σ_O	1	1.5 1.5	6.0 6.8	9.3 10.3	1.5 1.5	10.3 11.1	ns

AC ELECTRICAL CHARACTERISTICS AT 5.0V ±0.5V

SYMBOL	PARAMETER	WAVEFORM	74ACT11280					UNIT
			T_A = +25°C			T_A = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay I_n to Σ_E	1	1.5 1.5	6.8 7.7	10.8 11.6	1.5 1.5	11.9 12.8	ns
t_{PLH} t_{PHL}	Propagation delay I_n to Σ_O	1	1.5 1.5	6.9 7.6	10.9 11.4	1.5 1.5	11.8 12.8	ns

AC WAVEFORMS

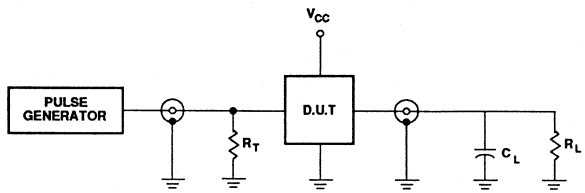


Waveform 1. Waveforms Showing the Inputs (I_n) to Output (Σ_E, Σ_O) Propagation Delays

WAVEFORM CONDITIONS

	INPUTS	OUTPUTS
AC	V_{IN} = GND to V_{CC}, V_M = 50% V_{CC}	V_{OUT} = V_{OL} to V_{OH}
ACT	V_{IN} = GND to 3.0V, V_M = 1.5V	V_M = 50% V_{CC}

TEST CIRCUIT



Test Circuit

DEFINITIONS

C_L = Load capacitance, 50pF; includes jig and probe capacitance

R_L = Load resistor, 500Ω

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators

Input pulses: PRR ≤ 10MHz

$t_r = t_f$ = 3ns

74AC/ACT11286

9-Bit Odd/Even Parity Generator/Checker with Bus Drive I/O Port

Preliminary Specification

FEATURES

- **Generates either odd or even parity for nine data lines**
- **Word length easily expanded by cascading**
- **Direct bus connection for parity generation or for checking by using the parity I/O port**
- **Glitch-free bus during power up/down**
- **Output capability: ±24mA**
- **CMOS (AC) and TTL (ACT) voltage level inputs**
- **50Ω incident wave switching**
- **Center-pin V_{CC} and ground configuration to minimize high-speed switching noise**
- **I_{CC} category: MSI**

DESCRIPTION

The 74AC/ACT11286 high-performance CMOS devices combine very high speed and high output drive comparable to the most advanced TTL families.

The 74AC/ACT11286 9-bit parity generator or checker is commonly used to detect errors in high-speed data transmission or data retrieval systems. It features a local output for parity checking and a bus-driv-

GENERAL INFORMATION

SYMBOL	PARAMETER	CONDITIONS T_A = 25°C; GND = 0V; V_{CC} = 5.0V		TYPICAL AC	TYPICAL ACT	UNIT
t_{PLH}/ t_{PHL}	Propagation delay I_n to PARITY ERROR	C_L = 50pF		6.9	8.6	ns
C_{PD}	Power dissipation capacitance[1]	f = 1MHz; C_L = 50pF	Enabled	53	56	pF
			Disabled	46	50	
C_{IN}	Input capacitance	V_I = 0V or V_{CC}		3.5	3.5	pF
$C_{I/O}$	I/O capacitance	$V_{I/O}$ = 0V or V_{CC}; Disabled		8.5	8.5	pF
I_{LATCH}	Latch-up current	Per Jedec JC40.2 Standard 17		500	500	mA

Note:

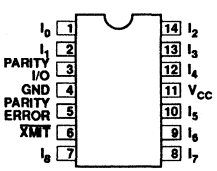
1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_I + \Sigma (C_L \times V_{CC}^2 \times f_O)$ where:
   f_I = input frequency in MHz, C_L = output load capacitance in pF,
   f_O = output frequency in MHz, V_{CC} = supply voltage in V,
   $\Sigma (C_L \times V_{CC}^2 \times f_O)$ = sum of outputs

ORDERING INFORMATION

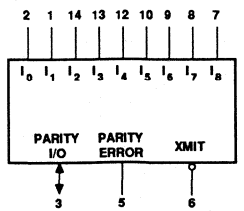
PACKAGES	TEMPERATURE RANGE	ORDER CODE
14-pin plastic DIP (300mil-wide)	-40°C to +85°C	74AC11286N 74ACT11286N
14-pin plastic SO (150mil-wide)	-40°C to +85°C	74AC11286D 74ACT11286D

PIN CONFIGURATION

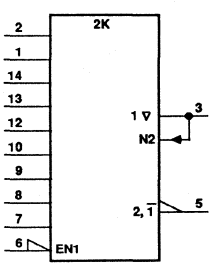
N and D Packages



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



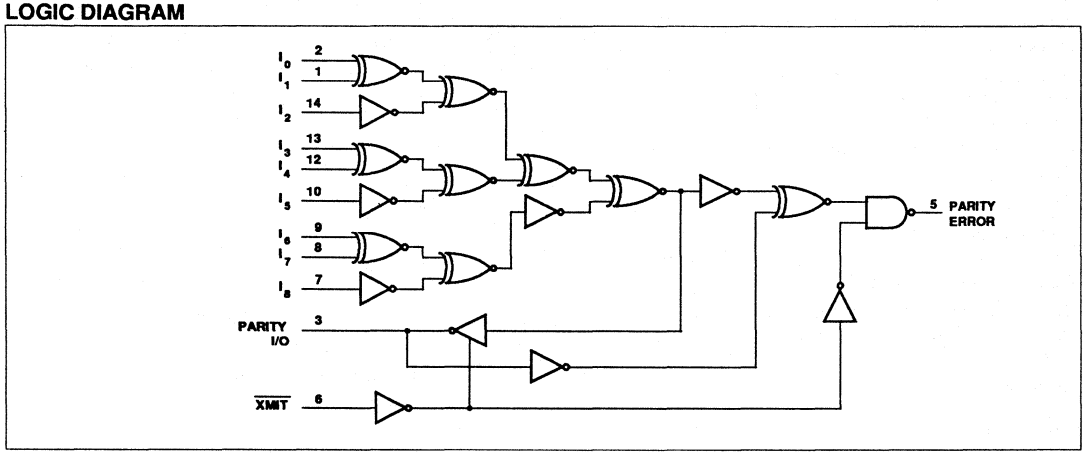
9-Bit Odd/Even Parity Generator/Checker with Bus Drive I/O Port

ing parity I/O port for parity generation/checking.

The $\overline{XMIT}$ control input is implemented specifically for cascading for expanding word length. When $\overline{XMIT}$ is held Low the parity tree is disabled and the Parity Error output remains at a High logic level regardless of the other inputs (I_0-I_8). When $\overline{XMIT}$ is High the parity tree is enabled. Parity Error indicates a parity error when either an even number of inputs are High and Parity I/O is forced to Low, or when an odd number of inputs are High and Parity I/O is forced High.

The I/O control circuitry is designed so that the I/O port will remain in the high-impedance state during power-up or power-down to prevent bus glitches.

LOGIC DIAGRAM



PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
2, 1, 14, 13, 12, 10, 9, 8, 7	I_0 - I_8	Data inputs
3	PARITY I/O	Parity I/O
6	$\overline{XMIT}$	Transmit input (active Low)
5	PARITY ERROR	Parity error output
4	GND	Ground (0V)
11	V_{CC}	Positive supply voltage

FUNCTION TABLE

Number of High Data Inputs (I_0 - I_8)	$\overline{XMIT}$	PARITY I/O	PARITY ERROR
0, 2, 4, 6, 8	l	H	H
1, 3, 5, 7, 9	l	L	H
0, 2, 4, 6, 8	h	h	H
	h	l	L
1, 3, 5, 7, 9	h	h	L
	h	l	H

l = Low voltage level input
h = High voltage level input
H = High voltage level output
L = Low voltage level output

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	74AC11286			74ACT11286			UNIT
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	DC supply voltage	3.0[1]	5.0	5.5	4.5	5.0	5.5	V
V_I	Input voltage	0		V_{CC}	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	0		V_{CC}	V
$\Delta t/\Delta v$	Input transition rise or fall rate	0		10	0		10	ns/V
T_A	Operating free-air temperature	-40		+85	-40		+85	°C

NOTE:

1. No electrical or switching characteristics are specified at V_{CC} < 3V. Operation between 2V and 3V is not recommended, but within that range, a device output will maintain a previously established logic state.

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	TEST CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 to+7.0	V
I_{IK} or V_I	DC input diode current[2]	$V_I < 0$	-20	mA
		$V_I > V_{CC}$	20	
	DC input voltage		-0.5 to V_{CC} +0.5	V
I_{OK} or V_O	DC output diode current[2]	$V_O < 0$	-50	mA
		$V_O > V_{CC}$	50	
	DC output voltage		-0.5 to V_{CC} +0.5	V
I_O	DC output source or sink current per output pin	V_O = 0 to V_{CC}	±50	mA
I_{CC} or I_{GND}	DC V_{CC} current		±100	mA
	DC ground current		±100	
T_{STG}	Storage temperature		-65 to 150	°C
P_{TOT}	Power dissipation per package Plastic DIP	Above 70°C:derate linearly by 8mW/K	500	mW
	Power dissipation per package Plastic surface mount (SO)	Above 70°C:derate linearly by 6mW/K	400	mW

NOTES:

1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		V_{CC}	74AC11286				74ACT11286				UNIT
					T_A = +25°C		T_A = -40°C to +85°C		T_A = +25°C		T_A = -40°C to +85°C		
				V	Min	Max	Min	Max	Min	Max	Min	Max	
V_{IH}	High-level input voltage			3.0	2.10		2.10						V
				4.5	3.15		3.15		2.0		2.0		
				5.5	3.85		3.85		2.0		2.0		
V_{IL}	Low-level input voltage			3.0		0.90		0.90					V
				4.5		1.35		1.35		0.8		0.8	
				5.5		1.65		1.65		0.8		0.8	
V_{OH}	High-level output voltage	V_I = V_{IL} or V_{IH}	I_{OH} = -50μA	3.0	2.9		2.9						V
				4.5	4.4		4.4		4.4		4.4		
				5.5	5.4		5.4		5.4		5.4		
			I_{OH} = -4mA	3.0	2.58		2.48						
			I_{OH} = -24mA	4.5	3.94		3.8		3.94		3.8		
				5.5	4.94		4.8		4.94		4.8		
			I_{OH} = -75mA[1]	5.5			3.85				3.85		
V_{OL}	Low-level output voltage	V_I = V_{IL} or V_{IH}	I_{OL} = 50μA	3.0		0.1		0.1					V
				4.5		0.1		0.1		0.1		0.1	
				5.5		0.1		0.1		0.1		0.1	
			I_{OL} = 12mA	3.0		0.36		0.44					
			I_{OL} = 24mA	4.5		0.36		0.44		0.36		0.44	
				5.5		0.36		0.44		0.36		0.44	
			I_{OL} = 75mA[1]	5.5				1.65				1.65	
I_I	Input leakage current	V_I = V_{CC} or GND		5.5		±0.1		±1.0		±0.1		±1.0	μA
I_{OZ}	3-State output off-state current	V_I = V_{IL} or V_{IH}, V_O = V_{CC} or GND		5.5		±0.5		±5.0		±0.5		±5.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC} or GND, I_O = 0		5.5		8.0		80		8.0		80	μA
ΔI_{CC}	Supply current, TTL inputs High[2]	One input at 3.4V, other inputs at V_{CC} or GND		5.5						0.9		1.0	mA

NOTES:
1. Not more than one output should be tested at a time, and the duration of the test should not exceed 10ms.
2. This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0V or V_{CC}.

AC ELECTRICAL CHARACTERISTICS AT 3.3V ±0.3V

SYMBOL	PARAMETER	WAVEFORM	74AC11286					UNIT
			T_A = +25°C			T_A = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay I_n to PARITY I/O	1	1.5 1.5	9.3 10.6	13.2 14.5	1.5 1.5	15.2 17.2	ns
t_{PLH} t_{PHL}	Propagation delay I_n to PARITY ERROR	1	1.5 1.5	10.1 11.0	14.4 15.1	1.5 1.5	16.3 17.1	ns
t_{PLH} t_{PHL}	Propagation delay PARITY I/O to PARITY ERROR	1	1.5 1.5	6.4 7.3	8.7 9.5	1.5 1.5	9.6 10.7	ns
t_{PZH} t_{PHZ}	Propagation delay $\overline{XMIT}$ to PARITY I/O	2	1.5 1.5	5.0 4.8	6.8 6.2	1.5 1.5	7.5 6.5	ns
t_{PZL} t_{PLZ}	Propagation delay $\overline{XMIT}$ to PARITY I/O	2	1.5 1.5	9.1 5.4	11.9 6.9	1.5 1.5	13.1 7.4	ns

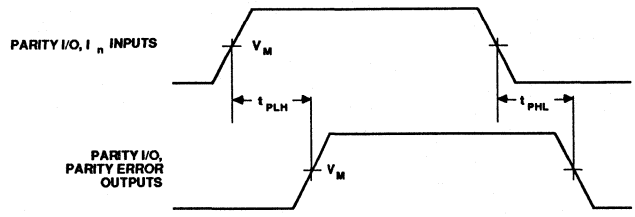
AC ELECTRICAL CHARACTERISTICS AT 5.0V ±0.5V

SYMBOL	PARAMETER	WAVEFORM	74AC11286					UNIT
			T_A = +25°C			T_A = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay I_n to PARITY I/O	1	1.5 1.5	6.0 6.9	8.8 9.8	1.5 1.5	10.0 11.1	ns
t_{PLH} t_{PHL}	Propagation delay I_n to PARITY ERROR	1	1.5 1.5	6.6 7.2	9.4 10.1	1.5 1.5	10.6 11.4	ns
t_{PLH} t_{PHL}	Propagation delay PARITY I/O to PARITY ERROR	1	1.5 1.5	4.4 5.0	6.1 6.7	1.5 1.5	6.8 7.4	ns
t_{PZH} t_{PHZ}	Propagation delay $\overline{XMIT}$ to PARITY I/O	2	1.5 1.5	3.4 4.4	5.0 5.7	1.5 1.5	5.4 6.0	ns
t_{PZL} t_{PLZ}	Propagation delay $\overline{XMIT}$ to PARITY I/O	2	1.5 1.5	5.7 4.6	7.9 5.9	1.5 1.5	9.0 6.3	ns

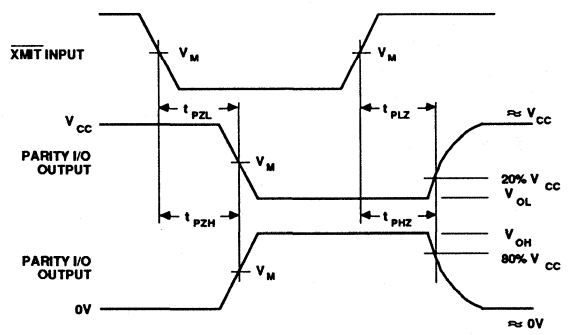
AC ELECTRICAL CHARACTERISTICS AT 5.0V ±0.5V

SYMBOL	PARAMETER	WAVEFORM	74ACT11286					UNIT
			T_A = +25°C			T_A = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay I_n to PARITY I/O	1	1.5 1.5	7.8 8.8	10.6 11.6	1.5 1.5	12.1 13.3	ns
t_{PLH} t_{PHL}	Propagation delay I_n to PARITY ERROR	1	1.5 1.5	8.3 8.8	11.1 11.9	1.5 1.5	12.7 13.4	ns
t_{PLH} t_{PHL}	Propagation delay PARITY I/O to PARITY ERROR	1	1.5 1.5	6.0 6.7	7.8 8.3	1.5 1.5	8.5 9.2	ns
t_{PZH} t_{PHZ}	Propagation delay $\overline{XMIT}$ to PARITY I/O	2	1.5 1.5	5.3 6.7	7.4 7.9	1.5 1.5	8.0 8.5	ns
t_{PZL} t_{PLZ}	Propagation delay $\overline{XMIT}$ to PARITY I/O	2	1.5 1.5	7.9 6.8	10.5 8.0	1.5 1.5	11.6 8.7	ns

AC WAVEFORMS



Waveform 1. Waveforms Showing the Inputs (I_n, PARITY I/O) to Outputs (PARITY ERROR, PARITY I/O) Propagation Delays

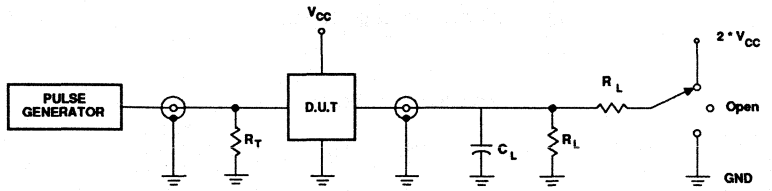


Waveform 2. Waveforms Showing the 3-State Output Enable and Disable Times

WAVEFORM CONDITIONS

	INPUTS	OUTPUTS
AC	V_{IN} = GND to V_{CC}, V_M = 50% V_{CC}	V_{OUT} = V_{OL} to V_{OH}
ACT	V_{IN} = GND to 3.0V, V_M = 1.5V	V_M = 50% V_{CC}

TEST CIRCUIT



Test Circuit

TEST	S1
t_{PLH}/t_{PHL}	Open
$t_{PLZ}t_{PZL}$	2*VCC
t_{PHZ}/t_{PZH}	GND

SWITCH POSITION

DEFINITIONS

C_L = Load capacitance, 50pF; includes jig and probe capacitance

R_L = Load resistor, 500Ω

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators

Input pulses: PRR ≤ 10MHz

$t_r = t_f$ = 3ns

74AC/ACT11299

8-Input Universal Shift/Storage Register with Asynchronous Reset and Common I/O Pins

Objective Specification

FEATURES

- **Multiplexed 3-State I/O ports for bus-oriented applications**
- **Additional Serial inputs and outputs for expansion**
- **Four operating modes: Shift Left, Shift Right, Load, and Store**
- **Output capability: ±24mA**
- **CMOS (AC) and TTL (ACT) voltage level inputs**
- **50Ω incident wave switching**
- **Center-pin V_{CC} and ground configuration to minimize high-speed switching noise**
- **I_{CC} category: MSI**

DESCRIPTION

The 74AC/ACT11299 high-performance CMOS devices combine very high speed and high output drive comparable to the most advanced TTL families.

The AC/ACT11299 is an 8-bit universal shift/storage register with 3-State outputs. Four modes of operation are possible: hold (store), shift left, shift right, and load data. The parallel load inputs and flip-flop outputs are multiplexed to reduce the total number of package pins. Additional out-

GENERAL INFORMATION

SYMBOL	PARAMETER	CONDITIONS T_A = 25°C; GND = 0V; V_{CC} = 5.0V		TYPICAL AC	TYPICAL ACT	UNIT
t_{PLH}/ t_{PHL}	Propagation delay CP to I/O_n	C_L = 50pF		7.5	9.0	ns
C_{PD}	Power dissipation capacitance per flip-flop[1]	f = 1MHz; C_L = 50pF	Enabled	232	232	pF
			Disabled	50	50	
C_{IN}	Input capacitance	V_I = 0V or V_{CC}		4.0	4.0	pF
C_O	Output capacitance	V_O = 0V or V_{CC}; Disabled		10	10	pF
C_{IO}	I/O capacitance	V_{IO} = 0V or V_{CC}; Disabled		12	12	pF
I_{LATCH}	Latch-up current	Per Jedec JC40.2 Standard 17		500	500	mA
f_{MAX}	Maximum clock frequency, CP to I/O_n	C_L = 50pF		140	65	MHz

Note:

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):

   $P_D = C_{PD} \times V_{CC}^2 \times f_I + \Sigma (C_L \times V_{CC}^2 \times f_O)$ where:

   f_I = input frequency in MHz, C_L = output load capacitance in pF,

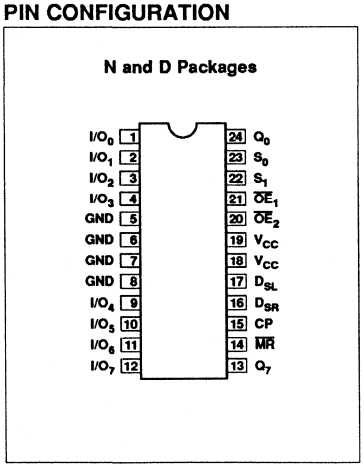
   f_O = output frequency in MHz, V_{CC} = supply voltage in V,

   $\Sigma (C_L \times V_{CC}^2 \times f_O)$ = sum of outputs

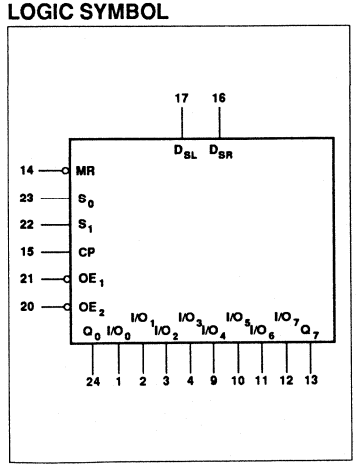
ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE
24-pin plastic DIP (300mil-wide)	-40°C to +85°C	74AC11299N 74ACT11299N
24-pin plastic SO (300mil-wide)	-40°C to +85°C	74AC11299D 74ACT11299D

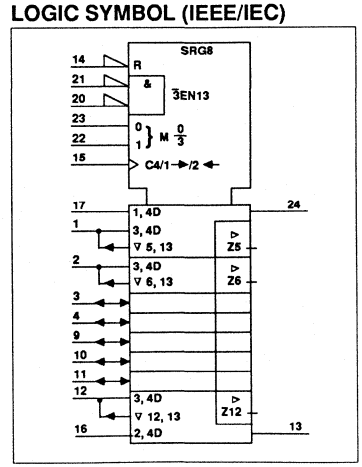
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



puts are provided for flip-flops Q_0 and Q_7 to allow easy serial cascading. A separate active-Low Master Reset is used to reset the register.

The AC/ACT11299 contains eight edge-triggered D-type flip-flops and the interstage logic necessary to perform synchronous shift left, shift right, parallel load and hold operations. The type of operation is determined by S_0 and S_1, as shown in the Mode Select Table. All flip-flop outputs are brought out through 3-State buffers to separate I/O pins that also serve as data inputs in the parallel load mode. Q_0 and Q_7 are also brought out on other pins for expansion in serial shifting of longer words.

A Low signal on $\overline{MR}$ overrides the Select and CP inputs and resets the flip-flops. All other state changes are initiated by the rising edge of the clock. Inputs can change when the clock is in either state provided only that the recommended setup and hold times, relative to the rising edge of CP, are observed.

A High signal on either $\overline{OE}_1$ or $\overline{OE}_2$ disables the 3-State buffers and puts the I/O pins in the high-impedance state. In this condition the shift, hold, load and reset operations can still occur. The 3-State buffers are also disabled by High signals on both S_0 and S_1 in preparation for a parallel load operation.

PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
15	CP	Clock input
17	D_{SL}	Serial data input for left shift
16	D_{SR}	Serial data input for right shift
23, 22	S_0, S_1	Mode select inputs
14	$\overline{MR}$	Asynchronous master reset input (active-Low)
21, 20	$\overline{OE}_1$, $\overline{OE}_2$	Output enable inputs (active-Low)
1, 2, 3, 4, 9, 10, 11, 12	I/O_0 -I/O_7	Data inputs/outputs
24, 13	Q_0, Q_7	Serial outputs
5, 6, 7, 8	GND	Ground (0V)
18, 19	V_{CC}	Positive supply voltage

MODE SELECT TABLE

INPUTS					OPERATING MODE
$\overline{OE}$	$\overline{MR}$	S_0	S_1	CP	
L	L	X	X	X	Asynchronous Reset; Q_0 - Q_7 = Low
L	H	H	H	↑	Parallel Load; $I/O_n \rightarrow Q_n$
L	H	L	H	↑	Shift Right; $D_{SR} \rightarrow Q_0$, $Q_0 \rightarrow Q_1$, etc.
L	H	H	L	↑	Shift Left; $D_{SL} \rightarrow Q_7$, $Q_7 \rightarrow Q_6$, etc.
L	H	L	L	X	Hold
H	X	X	X	X	Outputs in High-Z

H = High voltage levle
L = Low voltage levels
X = Don't Care
↑ = Low-to-High clock transition

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	74AC11299			74ACT11299			UNIT
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	DC supply voltage	3.0[1]	5.0	5.5	4.5	5.0	5.5	V
V_I	Input voltage	0		V_{CC}	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	0		V_{CC}	V
$\Delta t/\Delta v$	Input transition rise or fall rate	0		10	0		10	ns/V
T_A	Operating free-air temperature	-40		+85	-40		+85	°C

NOTE:

1. No electrical or switching characteristics are specified at V_{CC} < 3V. Operation between 2V and 3V is not recommended, but within that range, a device output will maintain a previously established logic state.

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	TEST CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 to+7.0	V
I_{IK} or V_I	DC input diode current[2]	$V_I < 0$	-20	mA
		$V_I > V_{CC}$	20	
	DC input voltage		-0.5 to V_{CC} +0.5	V
I_{OK} or V_O	DC output diode current[2]	$V_O < 0$	-50	mA
		$V_O > V_{CC}$	50	
	DC output voltage		-0.5 to V_{CC} +0.5	V
I_O	DC output source or sink current per output pin	V_O = 0 to V_{CC}	±50	mA
I_{CC} or I_{GND}	DC V_{CC} current		±250	mA
	DC ground current		±250	
T_{STG}	Storage temperature		-65 to 150	°C
P_{TOT}	Power dissipation per package Plastic DIP	Above 70°C:derate linearly by 8mW/K	500	mW
	Power dissipation per package Plastic surface mount (SO)	Above 70°C:derate linearly by 6mW/K	400	mW

NOTES:

1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		V_{CC}	74AC11299				74ACT11299				UNIT
					T_A = +25°C		T_A = -40°C to +85°C		T_A = +25°C		T_A = -40°C to +85°C		
				V	Min	Max	Min	Max	Min	Max	Min	Max	
V_{IH}	High-level input voltage			3.0	2.10		2.10						V
				4.5	3.15		3.15		2.0		2.0		
				5.5	3.85		3.85		2.0		2.0		
V_{IL}	Low-level input voltage			3.0		0.90		0.90					V
				4.5		1.35		1.35		0.8		0.8	
				5.5		1.65		1.65		0.8		0.8	
V_{OH}	High-level output voltage	V_I = V_{IL} or V_{IH}	I_{OH} = -50μA	3.0	2.9		2.9						V
				4.5	4.4		4.4		4.4		4.4		
				5.5	5.4		5.4		5.4		5.4		
			I_{OH} = -4mA	3.0	2.58		2.48						
			I_{OH} = -24mA	4.5	3.94		3.8		3.94		3.8		
				5.5	4.94		4.8		4.94		4.8		
			I_{OH} = -75mA[1]	5.5			3.85				3.85		
V_{OL}	Low-level output voltage	V_I = V_{IL} or V_{IH}	I_{OL} = 50μA	3.0		0.1		0.1					V
				4.5		0.1		0.1		0.1		0.1	
				5.5		0.1		0.1		0.1		0.1	
			I_{OL} = 12mA	3.0		0.36		0.44					
			I_{OL} = 24mA	4.5		0.36		0.44		0.36		0.44	
				5.5		0.36		0.44		0.36		0.44	
			I_{OL} = 75mA[1]	5.5				1.65				1.65	
I_I	Input leakage current	V_I = V_{CC} or GND		5.5		±0.1		±1.0		±0.1		±1.0	μA
I_{OZ}	3-State output off-state current	V_I = V_{IL} or V_{IH}, V_O = V_{CC} or GND		5.5		±0.5		±5.0		±0.5		±5.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC} or GND, I_O = 0		5.5		8.0		80		8.0		80	μA
ΔI_{CC}	Supply current, TTL inputs High[2]	One input at 3.4V, other inputs at V_{CC} or GND		5.5						0.9		1.0	mA

NOTES:
1. Not more than one output should be tested at a time, and the duration of the test should not exceed 10ms.
2. This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0V or V_{CC}.

74AC/ACT11323

8-Input Universal Shift/Storage Register with Synchronous Reset and Common I/O Pins

Objective Specification

FEATURES

- **Multiplexed 3-State I/O ports for bus-oriented applications**
- **Additional Serial inputs and outputs for expansion**
- **Four operating modes: Shift Left, Shift Right, Load, and Store**
- **Output capability: ±24mA**
- **CMOS (AC) and TTL (ACT) voltage level inputs**
- **50Ω incident wave switching**
- **Center-pin V_{CC} and ground configuration to minimize high-speed switching noise**
- **I_{CC} category: MSI**

DESCRIPTION

The 74AC/ACT11323 high-performance CMOS devices combine very high speed and high output drive comparable to the most advanced TTL families.

The AC/ACT11323 is an 8-bit universal shift/storage register with 3-State outputs. Its function is similar to the 74AC/ACT11299 with the exception of the synchronous Reset. Parallel load inputs and flip-flop outputs are multiplexed to minimize pin counts. Separate serial inputs

GENERAL INFORMATION

SYMBOL	PARAMETER	CONDITIONS T_A = 25°C; GND = 0V; V_{CC} = 5.0V		TYPICAL AC	TYPICAL ACT	UNIT
t_{PLH}/ t_{PHL}	Propagation delay CP to I/O_n	C_L = 50pF		7.5	9.0	ns
C_{PD}	Power dissipation capacitance per flip-flop[1]	f = 1MHz;	Enabled	232	232	pF
		C_L = 50pF	Disabled	50	50	
C_{IN}	Input capacitance	V_I = 0V or V_{CC}		4.0	4.0	pF
C_O	Output capacitance	V_O = 0V or V_{CC}; Disabled		10	10	pF
C_{IO}	I/O capacitance	V_{IO} = 0V or V_{CC}; Disabled		12	12	pF
I_{LATCH}	Latch-up current	Per Jedec JC40.2 Standard 17		500	500	mA
f_{MAX}	Maximum clock frequency, CP to I/O_n	C_L = 50pF		140	65	MHz

Note:

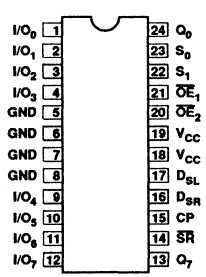
1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_I + \Sigma (C_L \times V_{CC}^2 \times f_O)$ where:
   f_I = input frequency in MHz, C_L = output load capacitance in pF,
   f_O = output frequency in MHz, V_{CC} = supply voltage in V,
   $\Sigma (C_L \times V_{CC}^2 \times f_O)$ = sum of outputs

ORDERING INFORMATION

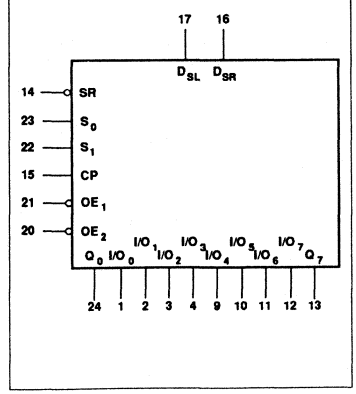
PACKAGES	TEMPERATURE RANGE	ORDER CODE
24-pin plastic DIP (300mil-wide)	-40°C to +85°C	74AC11323N 74ACT11323N
24-pin plastic SO (300mil-wide)	-40°C to +85°C	74AC11323D 74ACT11323D

PIN CONFIGURATION

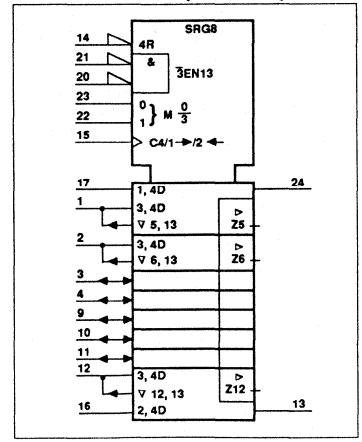
N and D Packages



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



and outputs are provided for flip-flops Q_0 and Q_7 to allow easy serial cascading. Four modes of operation are possible: hold (store), shift left, shift right, and load data.

The AC/ACT11323 contains eight edge-triggered D-type flip-flops and the inter-stage logic necessary to perform synchronous shift left, shift right, parallel load and hold operations. The type of operation is determined by S_0 and S_1, as shown in the Mode Select Table. All flip-flop outputs are brought out through 3-State buffers to separate I/O pins that also serve as data inputs in the parallel load mode. Q_0 and Q_7 are also brought out on other pins for expansion in serial shifting of longer words.

A Low signal on $\overline{SR}$ overrides the Select inputs and resets the flip-flops on the next rising edge of CP. All other state changes are initiated by the rising edge of the clock. Inputs can change when the clock is in either state provided only that the recommended setup and hold tirnes, relative to the rising edge of CP, are observed.

A High signal on either $\overline{OE}_1$ or $\overline{OE}_2$ disables the 3-State buffers and puts the I/O pins in the high-impedance state. In this condition the shift, hold, load and reset operations can still occur. The 3-State buffers are also disabled by High signals on both S_0 and S_1 in preparation for a parallel load operation.

PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
15	CP	Clock input
17	D_{SL}	Serial data input for left shift
16	D_{SR}	Serial data input for right shift
23, 22	S_0, S_1	Mode select inputs
14	$\overline{SR}$	Synchronous master reset input (active-Low)
21, 20	$\overline{OE}_1$, $\overline{OE}_2$	Output enable inputs (active-Low)
1, 2, 3, 4, 9, 10, 11, 12	I/O_0 -I/O_7	Data inputs/outputs
24, 13	Q_0, Q_7	Serial outputs
5, 6, 7, 8	GND	Ground (0V)
18, 19	V_{CC}	Positive supply voltage

MODE SELECT TABLE

INPUTS					OPERATING MODE
$\overline{SR}$	$\overline{OE}_n$	S_0	S_1	CP	
L	L	X	X	↑	Synchronous Reset; Q_0 - Q_7 = Low
H	L	H	H	↑	Parallel Load; $I/O_n \rightarrow Q_n$
H	L	L	H	↑	Shift Right; $D_{SR} \rightarrow Q_0$, $Q_0 \rightarrow Q_1$, etc.
H	L	H	L	↑	Shift Left; $D_{SL} \rightarrow Q_7$, $Q_7 \rightarrow Q_6$, etc.
H	L	L	L	X	Hold
X	H	X	X	X	Outputs Disabled

H = High voltage levle
L = Low voltage levels
X = Don't Care
↑ = Low-to-High clock transition

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	74AC11323			74ACT11323			UNIT
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	DC supply voltage	3.0[1]	5.0	5.5	4.5	5.0	5.5	V
V_I	Input voltage	0		V_{CC}	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	0		V_{CC}	V
$\Delta t/\Delta v$	Input transition rise or fall rate	0		10	0		10	ns/V
T_A	Operating free-air temperature	-40		+85	-40		+85	°C

NCTE:

1. No electrical or switching characteristics are specified at $V_{CC} < 3V$. Operation between 2V and 3V is not recommended, but within that range, a device output will maintain a previously established logic state.

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	TEST CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 to+7.0	V
I_{IK} or V_I	DC input diode current[2]	$V_I < 0$	-20	mA
		$V_I > V_{CC}$	20	
	DC input voltage		-0.5 to V_{CC} +0.5	V
I_{OK} or V_O	DC output diode current[2]	$V_O < 0$	-50	mA
		$V_O > V_{CC}$	50	
	DC output voltage		-0.5 to V_{CC} +0.5	V
I_O	DC output source or sink current per output pin	V_O = 0 to V_{CC}	±50	mA
I_{CC} or I_{GND}	DC V_{CC} current		±250	mA
	DC ground current		±250	
T_{STG}	Storage temperature		-65 to 150	°C
P_{TOT}	Power dissipation per package Plastic DIP	Above 70°C:derate linearly by 8mW/K	500	mW
	Power dissipation per package Plastic surface mount (SO)	Above 70°C:derate linearly by 6mW/K	400	mW

NOTES:

1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		V_{CC}	74AC11323				74ACT11323				UNIT
					T_A = +25°C		T_A = -40°C to +85°C		T_A = +25°C		T_A = -40°C to +85°C		
				V	Min	Max	Min	Max	Min	Max	Min	Max	
V_{IH}	High-level input voltage			3.0	2.10		2.10						V
				4.5	3.15		3.15		2.0		2.0		
				5.5	3.85		3.85		2.0		2.0		
V_{IL}	Low-level input voltage			3.0		0.90		0.90					V
				4.5		1.35		1.35		0.8		0.8	
				5.5		1.65		1.65		0.8		0.8	
V_{OH}	High-level output voltage	V_I = V_{IL} or V_{IH}	I_{OH} = -50μA	3.0	2.9		2.9						V
				4.5	4.4		4.4		4.4		4.4		
				5.5	5.4		5.4		5.4		5.4		
			I_{OH} = -4mA	3.0	2.58		2.48						
			I_{OH} = -24mA	4.5	3.94		3.8		3.94		3.8		
				5.5	4.94		4.8		4.94		4.8		
			I_{OH} = -75mA[1]	5.5			3.85				3.85		
V_{OL}	Low-level output voltage	V_I = V_{IL} or V_{IH}	I_{OL} = 50μA	3.0		0.1		0.1					V
				4.5		0.1		0.1		0.1		0.1	
				5.5		0.1		0.1		0.1		0.1	
			I_{OL} = 12mA	3.0		0.36		0.44					
			I_{OL} = 24mA	4.5		0.36		0.44		0.36		0.44	
				5.5		0.36		0.44		0.36		0.44	
			I_{OL} = 75mA[1]	5.5				1.65				1.65	
I_I	Input leakage current	V_I = V_{CC} or GND		5.5		±0.1		±1.0		±0.1		±1.0	μA
I_{OZ}	3-State output off-state current	V_I = V_{IL} or V_{IH}, V_O = V_{CC} or GND		5.5		±0.5		±5.0		±0.5		±5.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC} or GND, I_O = 0		5.5		8.0		80		8.0		80	μA
ΔI_{CC}	Supply current, TTL inputs High[2]	One input at 3.4V, other inputs at V_{CC} or GND		5.5						0.9		1.0	mA

NOTES:
1. Not more than one output should be tested at a time, and the duration of the test should not exceed 10ms.
2. This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0V or V_{CC}.

74AC/ACT11352

Dual 4-Input Multiplexer; INV

Objective Specification

FEATURES

- **Separate Output Enable inputs for each section**
- **Common Select inputs**
- **Output capability: ±24 mA**
- **CMOS (AC) and TTL (ACT) voltage level inputs**
- **50Ω incident wave switching**
- **Center-pin V_{CC} and ground configuration to minimize high-speed switching noise**
- **I_{CC} category: MSI**

DESCRIPTION

The 74AC/ACT11352 high-performance CMOS devices combine very high speed and high output drive comparable to the most advanced TTL families.

The 74AC/ACT11352 device provides two identical 4-input multiplexers with inverting outputs which select two bits from four sources selected by common select inputs (S_0, S_1). When the individual Enable ($1\overline{E}$, $2\overline{E}$) inputs of the 4-input multiplexers are High, the outputs are forced High.

The 74AC/ACT11352 devices are the logic implementation of a 2-pole, 4-position switch; the position of the switch being determined by the logic levels supplied to the two select inputs.

The '11352 is the inverting version of the '11153.

GENERAL INFORMATION

SYMBOL	PARAMETER	CONDITIONS T_A = 25°C; GND = 0V; V_{CC} = 5.0V	TYPICAL		UNIT
			AC	ACT	
t_{PLH}/ t_{PHL}	Propagation delay $1I_n$, $2I_n$ to $n\overline{Y}$	C_L = 50pF	5.0	6.0	ns
C_{PD}	Power dissipation capacitance per multiplexer[1]	f = 1MHz; C_L = 50pF	39	39	pF
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	3.5	3.5	pF
I_{LATCH}	Latch-up current	Per Jedec JC40.2 Standard 17	500	500	mA

Note:

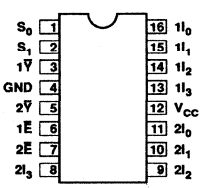
1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_I + \Sigma (C_L \times V_{CC}^2 \times f_O)$ where:
   f_I = input frequency in MHz, C_L = output load capacitance in pF,
   f_O = output frequency in MHz, V_{CC} = supply voltage in V,
   $\Sigma (C_L \times V_{CC}^2 \times f_O)$ = sum of outputs

ORDERING INFORMATION

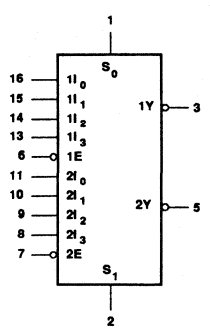
PACKAGES	TEMPERATURE RANGE	ORDER CODE
16-pin plastic DIP (300mil-wide)	-40°C to +85°C	74AC11352N 74ACT11352N
16-pin plastic SO (150mil-wide)	-40°C to +85°C	74AC11352D 74ACT11352D

PIN CONFIGURATION

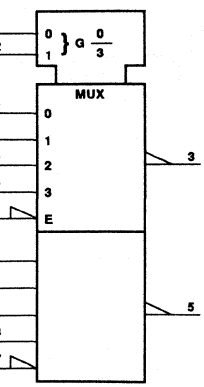
N and D Packages



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



PIN DESCRIPTION

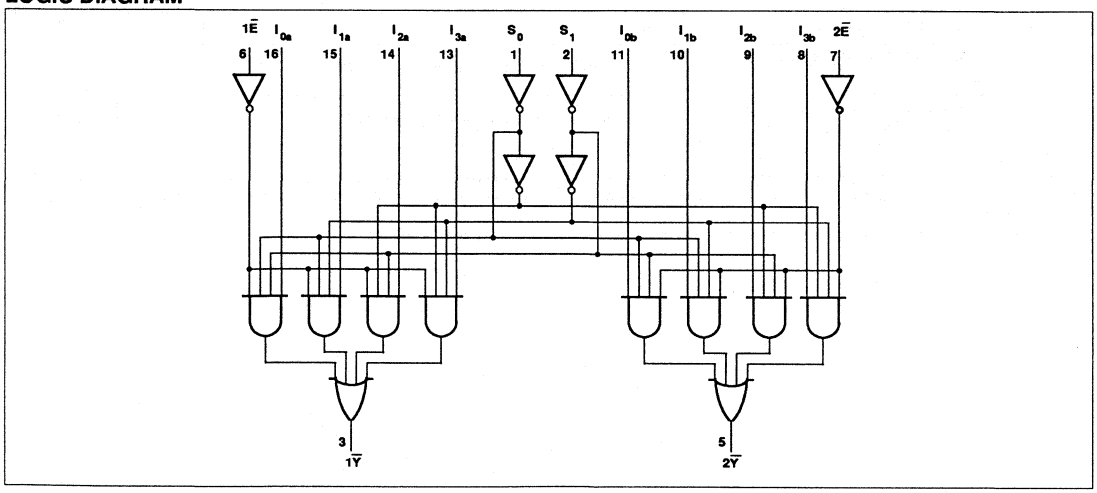
PIN NUMBER	SYMBOL	NAME AND FUNCTION
1, 2	S_0, S_1	Common select inputs
16, 15, 14, 13	$1I_0$ - $1I_3$	Port A data inputs
11, 10, 9, 8	$2I_0$ - $2I_3$	Port B data inputs
6	$1\overline{E}$	Port A enable input (active Low)
7	$2\overline{E}$	Port B enable input (active Low)
3, 5	$1\overline{Y}$, $2\overline{Y}$	Data outputs
4	GND	Ground (0V)
12	V_{CC}	Positive supply voltage

FUNCTION TABLE

INPUTS							OUTPUT
$n\overline{E}$	S_0	S_1	I_{0n}	I_{1n}	I_{2n}	I_{3n}	$n\overline{Y}$
H	X	X	X	X	X	X	H
L	L	L	L	X	X	X	H
L	L	L	H	X	X	X	L
L	H	L	X	L	X	X	H
L	H	L	X	H	X	X	L
L	L	H	X	X	L	X	H
L	L	H	X	X	H	X	L
L	H	H	X	X	X	L	H
L	H	H	X	X	X	H	L

H = High voltage level steady state
L = Low voltage level steady state
X = Don't care

LOGIC DIAGRAM



RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	74AC11352			74ACT11352			UNIT
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	DC supply voltage	3.0[1]	5.0	5.5	4.5	5.0	5.5	V
V_I	Input voltage	0		V_{CC}	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	0		V_{CC}	V
$\Delta t/\Delta v$	Input transition rise or fall rate	0		10	0		10	ns/V
T_A	Operating free-air temperature	-40		+85	-40		+85	°C

NOTE:

1. No electrical or switching characteristics are specified at V_{CC} < 3V. Operation between 2V and 3V is not recommended, but within that range, a device output will maintain a previously established logic state.

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	TEST CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 to+7.0	V
I_{IK} or V_I	DC input diode current[2]	$V_I < 0$	-20	mA
		$V_I > V_{CC}$	20	
	DC input voltage		-0.5 to V_{CC} +0.5	V
I_{OK} or V_O	DC output diode current[2]	$V_O < 0$	-50	mA
		$V_O > V_{CC}$	50	
	DC output voltage		-0.5 to V_{CC} +0.5	V
I_O	DC output source or sink current per output pin	V_O = 0 to V_{CC}	±50	mA
I_{CC} or I_{GND}	DC V_{CC} current		±100	mA
	DC ground current		±100	
T_{STG}	Storage temperature		-65 to 150	°C
P_{TOT}	Power dissipation per package Plastic DIP	Above 70°C:derate linearly by 8mW/K	500	mW
	Power dissipation per package Plastic surface mount (SO)	Above 70°C:derate linearly by 6mW/K	400	mW

NOTES:

1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		V_{CC}	74AC11352				74ACT11352				UNIT
					T_A = +25°C		T_A = -40°C to +85°C		T_A = +25°C		T_A = -40°C to +85°C		
				V	Min	Max	Min	Max	Min	Max	Min	Max	
V_{IH}	High-level input voltage			3.0	2.10		2.10						V
				4.5	3.15		3.15		2.0		2.0		
				5.5	3.85		3.85		2.0		2.0		
V_{IL}	Low-level input voltage			3.0		0.90		0.90					V
				4.5		1.35		1.35		0.8		0.8	
				5.5		1.65		1.65		0.8		0.8	
V_{OH}	High-level output voltage	V_I = V_{IL} or V_{IH}	I_{OH} = -50μA	3.0	2.9		2.9						V
				4.5	4.4		4.4		4.4		4.4		
				5.5	5.4		5.4		5.4		5.4		
			I_{OH} = -4mA	3.0	2.58		2.48						
			I_{OH} = -24mA	4.5	3.94		3.8		3.94		3.8		
				5.5	4.94		4.8		4.94		4.8		
			I_{OH} = -75mA[1]	5.5			3.85				3.85		
V_{OL}	Low-level output voltage	V_I = V_{IL} or V_{IH}	I_{OL} = 50μA	3.0		0.1		0.1					V
				4.5		0.1		0.1		0.1		0.1	
				5.5		0.1		0.1		0.1		0.1	
			I_{OL} = 12mA	3.0		0.36		0.44					
			I_{OL} = 24mA	4.5		0.36		0.44		0.36		0.44	
				5.5		0.36		0.44		0.36		0.44	
			I_{OL} = 75mA[1]	5.5				1.65				1.65	
I_I	Input leakage current	V_I = V_{CC} or GND		5.5		±0.1		±1.0		±0.1		±1.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC} or GND, I_O = 0		5.5		8.0		80		8.0		80	μA
ΔI_{CC}	Supply current, TTL inputs High[2]	One input at 3.4V, other inputs at V_{CC} or GND		5.5						0.9		1.0	mA

NOTES:
1. Not more than one output should be tested at a time, and the duration of the test should not exceed 10ms.
2. This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0V or V_{CC}

AC ELECTRICAL CHARACTERISTICS AT 3.3V ±0.3V

SYMBOL	PARAMETER	WAVEFORM	74AC11153					UNIT
			T_A = +25°C			T_A = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay I_n to $n\overline{Y}$	1	1.5 1.5			1.5 1.5		ns
t_{PLH} t_{PHL}	Propagation delay S_n to $n\overline{Y}$	1	1.5 1.5			1.5 1.5		ns
t_{PLH} t_{PHL}	Propagation delay $n\overline{E}$ to $n\overline{Y}$	2	1.5 1.5			1.5 1.5		ns

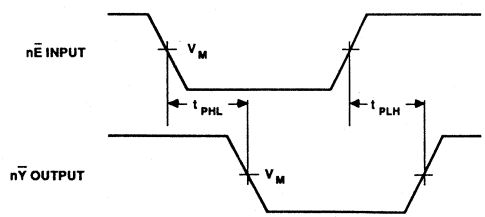
AC ELECTRICAL CHARACTERISTICS AT 5.0V ±0.5V

SYMBOL	PARAMETER	WAVEFORM	74AC11153					UNIT
			T_A = +25°C			T_A = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay I_n to $n\overline{Y}$	1	1.5 1.5			1.5 1.5		ns
t_{PLH} t_{PHL}	Propagation delay S_n to $n\overline{Y}$	1	1.5 1.5			1.5 1.5		ns
t_{PLH} t_{PHL}	Propagation delay $n\overline{E}$ to $n\overline{Y}$	2	1.5 1.5			1.5 1.5		ns

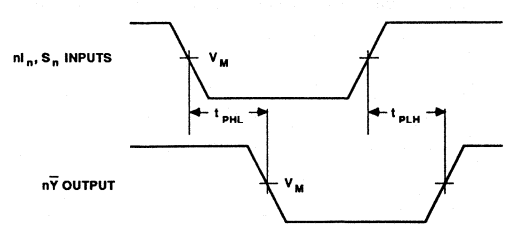
AC ELECTRICAL CHARACTERISTICS AT 5.0V ±0.5V

SYMBOL	PARAMETER	WAVEFORM	74ACT11153					UNIT
			T_A = +25°C			T_A = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay I_n to $n\overline{Y}$	1	1.5 1.5			1.5 1.5		ns
t_{PLH} t_{PHL}	Propagation delay S_n to $n\overline{Y}$	1	1.5 1.5			1.5 1.5		ns
t_{PLH} t_{PHL}	Propagation delay $n\overline{E}$ to $n\overline{Y}$	2	1.5 1.5			1.5 1.5		ns

AC WAVEFORMS



Waveform 1. Waveforms Showing the Enable Input ($n\overline{E}$) to Output ($n\overline{Y}$) Propagation Delays



Waveform 2. Waveforms Showing the Data Inputs (nI_n) and Select Input (S_n) to Output ($n\overline{Y}$) Propagation Delays

The 74AC/ACT11353 devices are the logic implementation of a 2-pole, 4-position switch; the position of the switch being determined by the logic levels supplied to the two select inputs.

The '11253 is the non-inverting version of the '11353.

PIN DESCRIPTION

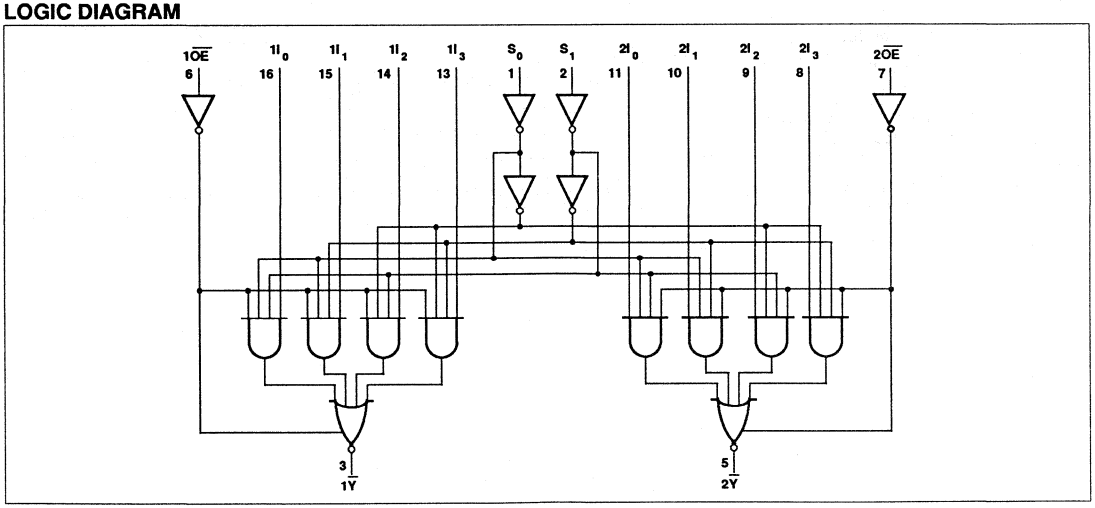
PIN NUMBER	SYMBOL	NAME AND FUNCTION
1, 2	S_0, S_1	Common select inputs
16, 15, 14, 13	$1I_0$ - $1I_3$	Port A data inputs
11, 10, 9, 8	$2I_0$ - $2I_3$	Port B data inputs
6	$1\overline{OE}$	Port A output enable input
7	$2\overline{OE}$	Port B output enable input
3, 5	$1\overline{Y}$, $2\overline{Y}$	3-State data outputs
4	GND	Ground (0V)
12	V_{CC}	Positive supply voltage

FUNCTION TABLE

INPUTS							OUTPUT
$n\overline{OE}$	S_1	S_0	nI_0	nI_1	nI_2	nI_3	$n\overline{Y}$
H	X	X	X	X	X	X	Z
L	L	L	L	X	X	X	H
L	L	L	H	X	X	X	L
L	L	H	X	L	X	X	H
L	L	H	X	H	X	X	L
L	H	L	X	X	L	X	H
L	H	L	X	X	H	X	L
L	H	H	X	X	X	L	H
L	H	H	X	X	X	H	L

H = High voltage level steady state
L = Low voltage level steady state
X = Don't care
Z = High-impedance "OFF" state

LOGIC DIAGRAM



RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	74AC11353			74ACT11353			UNIT
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	DC supply voltage	3.0[1]	5.0	5.5	4.5	5.0	5.5	V
V_I	Input voltage	0		V_{CC}	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	0		V_{CC}	V
$\Delta t/\Delta v$	Input transition rise or fall rate	0		10	0		10	ns/V
T_A	Operating free-air temperature	-40		+85	-40		+85	°C

NOTE:

1. No electrical or switching characteristics are specified at V_{CC} < 3V. Operation between 2V and 3V is not recommended, but within that range, a device output will maintain a previously established logic state.

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	TEST CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 to+7.0	V
I_{IK} or V_I	DC input diode current[2]	$V_I < 0$	-20	mA
		$V_I > V_{CC}$	20	
	DC input voltage		-0.5 to V_{CC} +0.5	V
I_{OK} or V_O	DC output diode current[2]	$V_O < 0$	-50	mA
		$V_O > V_{CC}$	50	
	DC output voltage		-0.5 to V_{CC} +0.5	V
I_O	DC output source or sink current per output pin	V_O = 0 to V_{CC}	±50	mA
I_{CC} or I_{GND}	DC V_{CC} current		±100	mA
	DC ground current		±100	
T_{STG}	Storage temperature		-65 to 150	°C
P_{TOT}	Power dissipation per package Plastic DIP	Above 70°C:derate linearly by 8mW/K	500	mW
	Power dissipation per package Plastic surface mount (SO)	Above 70°C:derate linearly by 6mW/K	400	mW

NOTES:

1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		V_{CC}	74AC11353				74ACT11353				UNIT
					T_A = +25°C		T_A = -40°C to +85°C		T_A = +25°C		T_A = -40°C to +85°C		
				V	Min	Max	Min	Max	Min	Max	Min	Max	
V_{IH}	High-level input voltage			3.0	2.10		2.10						V
				4.5	3.15		3.15		2.0		2.0		
				5.5	3.85		3.85		2.0		2.0		
V_{IL}	Low-level input voltage			3.0		0.90		0.90					V
				4.5		1.35		1.35		0.8		0.8	
				5.5		1.65		1.65		0.8		0.8	
V_{OH}	High-level output voltage	V_I = V_{IL} or V_{IH}	I_{OH} = -50μA	3.0	2.9		2.9						V
				4.5	4.4		4.4		4.4		4.4		
				5.5	5.4		5.4		5.4		5.4		
			I_{OH} = -4mA	3.0	2.58		2.48						
			I_{OH} = -24mA	4.5	3.94		3.8		3.94		3.8		
				5.5	4.94		4.8		4.94		4.8		
			I_{OH} = -75mA[1]	5.5			3.85				3.85		
V_{OL}	Low-level output voltage	V_I = V_{IL} or V_{IH}	I_{OL} = 50μA	3.0		0.1		0.1					V
				4.5		0.1		0.1		0.1		0.1	
				5.5		0.1		0.1		0.1		0.1	
			I_{OL} = 12mA	3.0		0.36		0.44					
			I_{OL} = 24mA	4.5		0.36		0.44		0.36		0.44	
				5.5		0.36		0.44		0.36		0.44	
			I_{OL} = 75mA[1]	5.5				1.65				1.65	
I_I	Input leakage current	V_I = V_{CC} or GND		5.5		±0.1		±1.0		±0.1		±1.0	μA
I_{OZ}	3-State output off-state current	V_I = V_{IL} or V_{IH}; V_O = V_{CC} or GND		5.5		±0.5		±5.0		±0.5		±5.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC} or GND, I_O = 0		5.5		8.0		80		8.0		80	μA
ΔI_{CC}	Supply current, TTL inputs High[2]	One input at 3.4V, other inputs at V_{CC} or GND		5.5						0.9		1.0	mA

NOTES:
1. Not more than one output should be tested at a time, and the duration of the test should not exceed 10ms.
2. This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0V or V_{CC}.

AC ELECTRICAL CHARACTERISTICS AT 3.3V ±0.3V

SYMBOL	PARAMETER	WAVEFORM	74AC11353					UNIT
			T_A = +25°C			T_A = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay nI_n to $n\overline{Y}$	1	1.5 1.5	6.5 6.6	8.6 8.7	1.5 1.5	9.6 9.7	ns
t_{PLH} t_{PHL}	Propagation delay S_n to $n\overline{Y}$	1	1.5 1.5	7.0 7.2	9.6 9.8	1.5 1.5	10.7 10.9	ns
t_{PZH} t_{PZL}	Output enable time to High and Low Level	2	1.5 1.5	4.4 5.4	6.0 7.2	1.5 1.5	6.6 7.9	ns
t_{PHZ} t_{PLZ}	Output disable time from High and Low Level	2	1.5 1.5	4.8 4.9	6.2 6.3	1.5 1.5	6.5 6.6	ns

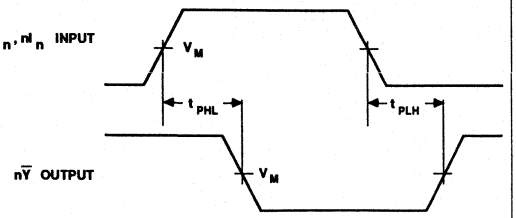
AC ELECTRICAL CHARACTERISTICS AT 5.0V ±0.5V

SYMBOL	PARAMETER	WAVEFORM	74AC11353					UNIT
			T_A = +25°C			T_A = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay nI_n to $n\overline{Y}$	1	1.5 1.5	4.0 4.2	5.9 6.1	1.5 1.5	6.6 6.8	ns
t_{PLH} t_{PHL}	Propagation delay S_n to $n\overline{Y}$	1	1.5 1.5	4.5 4.6	6.6 6.9	1.5 1.5	7.4 7.6	ns
t_{PZH} t_{PZL}	Output enable time to High and Low Level	2	1.5 1.5	2.9 3.4	4.4 5.1	1.5 1.5	4.8 5.6	ns
t_{PHZ} t_{PLZ}	Output disable time from High and Low Level	2	1.5 1.5	4.4 4.1	5.8 5.5	1.5 1.5	6.1 5.8	ns

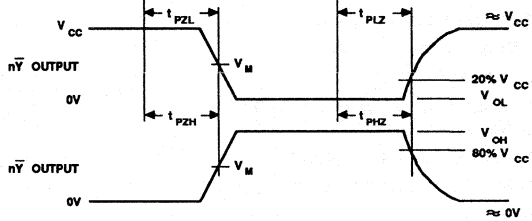
AC ELECTRICAL CHARACTERISTICS AT 5.0V ±0.5V

SYMBOL	PARAMETER	WAVEFORM	74ACT11353					UNIT
			T_A = +25°C			T_A = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay nI_n to $n\overline{Y}$	1	1.5 1.5	6.3 5.3	9.8 7.2	1.5 1.5	11.0 8.0	ns
t_{PLH} t_{PHL}	Propagation delay S_n to $n\overline{Y}$	1	1.5 1.5	6.6 5.9	11.1 8.3	1.5 1.5	12.7 9.4	ns
t_{PZH} t_{PZL}	Output enable time to High and Low Level	2	1.5 1.5	4.3 4.2	6.8 6.7	1.5 1.5	7.4 7.4	ns
t_{PHZ} t_{PLZ}	Output disable time from High and Low Level	2	1.5 1.5	6.1 5.4	7.8 6.9	1.5 1.5	8.2 7.3	ns

AC WAVEFORMS



Waveform 1. Waveforms Showing the Input (nI_n, S_n) to Output ($n\overline{Y}$) Propagation Delays

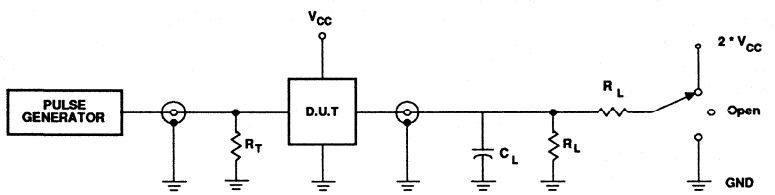


Waveform 2. Waveforms Showing the 3-State Output Enable and Disable Times

WAVEFORM CONDITIONS

	INPUTS	OUTPUTS
AC	V_{IN} = GND to V_{CC}, V_M = 50% V_{CC}	V_{OUT} = V_{OL} to V_{OH}
ACT	V_{IN} = GND to 3.0V, V_M = 1.5V	V_M = 50% V_{CC}

TEST CIRCUIT



Test Circuit

TEST	S1
t_{PLH}/t_{PHL}	Open
$t_{PLZ}t_{PZL}$	2*VCC
t_{PHZ}/t_{PZH}	GND

SWITCH POSITION

DEFINITIONS

C_L = Load capacitance, 50pF; includes jig and probe capacitance

R_L = Load resistor, 500Ω

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators

Input pulses: PRR ≤ 10MHz

$t_r = t_f$ = 3ns

74AC/ACT11373

Octal D-Type Transparent Latch; 3-State

Product Specification

FEATURES

- **8-bit transparent latch**
- **3-State output buffers**
- **Common 3-State Output Enable**
- **Independent register and 3-State buffer operation**
- **Output capability: ±24 mA**
- **CMOS (AC) and TTL (ACT) voltage level inputs**
- **50Ω incident wave switching**
- **Center-pin V_{CC} and ground configuration to minimize high-speed switching noise**
- **I_{CC} category: MSI**

DESCRIPTION

The 74AC/ACT11373 high-performance CMOS devices combine very high speed and high output drive comparable to the most advanced TTL families.

The 74AC/ACT11373 device is an octal transparent latch coupled to eight 3-State output buffers. The two sections of the device are controlled independently by Latch Enable (LE) and Output Enable ($\overline{OE}$) control gates.

The data on the D inputs are transferred to the latch outputs when the Latch Enable (LE) input is High. The latch remains

GENERAL INFORMATION

SYMBOL	PARAMETER	CONDITIONS T_A = 25°C; GND = 0V; V_{CC} = 5.0V		TYPICAL AC	TYPICAL ACT	UNIT
t_{PLH}/t_{PHL}	Propagation delay D_n to Q_n	C_L = 50pF		5.8	7.0	ns
C_{PD}	Power dissipation capacitance per latch[1]	f = 1MHz; C_L = 50pF	Enabled	47	65	pF
			Disabled	36	54	
C_{IN}	Input capacitance	V_I = 0V or V_{CC}		4.0	4.0	pF
C_{OUT}	Output capacitance	V_I = 0V or V_{CC}; Disabled		10	10	pF
I_{LATCH}	Latch-up current	Per Jedec JC40.2 Standard 17		500	500	mA

Note:

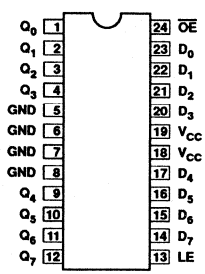
1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_I + \Sigma (C_L \times V_{CC}^2 \times f_O)$ where:
   f_I = input frequency in MHz, C_L = output load capacitance in pF,
   f_O = output frequency in MHz, V_{CC} = supply voltage in V,
   $\Sigma (C_L \times V_{CC}^2 \times f_O)$ = sum of outputs

ORDERING INFORMATION

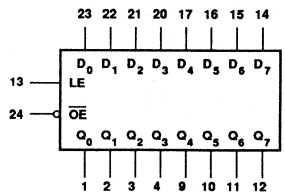
PACKAGES	TEMPERATURE RANGE	ORDER CODE
24-pin plastic DIP (300mil-wide)	-40°C to +85°C	74AC11373N 74ACT11373N
24-pin plastic SO (300mil-wide)	-40°C to +85°C	74AC11373D 74ACT11373D

PIN CONFIGURATION

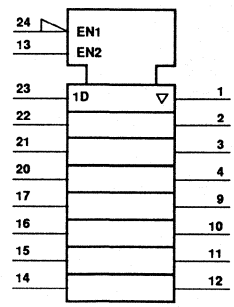
N and D Packages



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



transparent to the data inputs while LE is High, and stores the data that is present one setup time before the High-to-Low enable transition.

The 3-State output buffers are designed to drive heavily loaded 3-State buses, MOS memories, or MOS microprocessors. The active-Low Output Enable ($\overline{OE}$) controls all eight 3-State buffers independent of the latch operation.

When $\overline{OE}$ is Low, the latched or transparent data appears at the outputs. When $\overline{OE}$ is High, the outputs are in the High-impedance "OFF" state, which means they will neither drive nor load the bus.

PIN DESCRIPTION

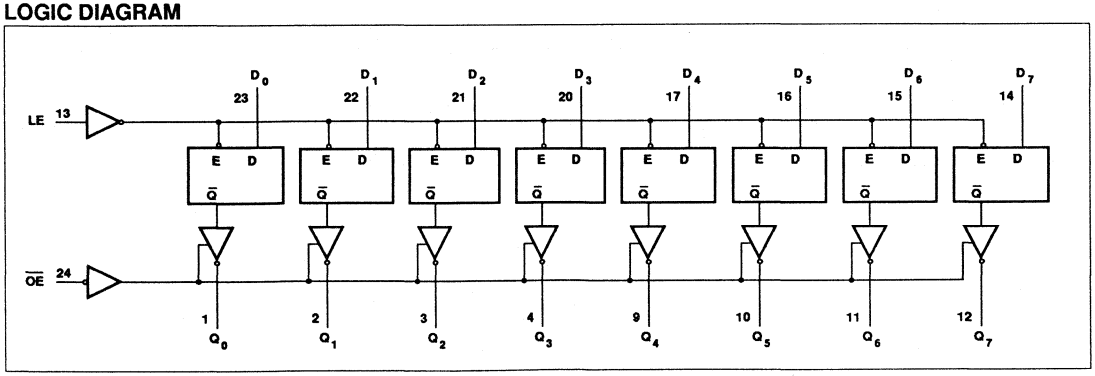
PIN NUMBER	SYMBOL	NAME AND FUNCTION
24	$\overline{OE}$	Output enable
23, 22, 21, 20, 17, 16, 15, 14	D_0 - D_7	Data inputs
1, 2, 3, 4, 9, 10, 11, 12	Q_0 - Q_7	Data outputs
13	LE	Latch enable
5, 6, 7, 8	GND	Ground (0V)
18, 19	V_{CC}	Positive supply voltage

FUNCTION TABLE

OPERATING MODES	INPUTS			INTERNAL REGISTER	OUTPUTS
	$\overline{OE}$	LE	D_n		Q_n
Enable and read register	L L	H H	L H	L H	L H
Latch and read register	L L	↓ ↓	l h	L H	L H
Hold	L	L	X	NC	NC
Disable outputs	H	X	X	X	Z

H = High voltage level steady state
h = High voltage level one set-up time prior to the High-to-Low E transition
L = Low voltage level steady state
l = Low voltage level one set-up time prior to the High-to-Low E transition
X = Don't care
NC = No change
Z = High-impedance "OFF" state
↓ = High-to-Low transition

LOGIC DIAGRAM



RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		74AC11373			74ACT11373			UNIT
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	DC supply voltage		3.0[1]	5.0	5.5	4.5	5.0	5.5	V
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
$\Delta t/\Delta v$	Input transition rise or fall rate	Data, LE	0		10	0		10	ns/V
		Output enable	0		5	0		10	
T_A	Operating free-air temperature		-40		+85	-40		+85	°C

NOTE:

1. No electrical or switching characteristics are specified at $V_{CC} < 3V$. Operation between 2V and 3V is not recommended, but within that range, a device output will maintain a previously established logic state.

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	TEST CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 to+7.0	V
I_{IK} or V_I	DC input diode current[2]	$V_I < 0$	-20	mA
		$V_I > V_{CC}$	20	
	DC input voltage		-0.5 to V_{CC} +0.5	V
I_{OK} or V_O	DC output diode current[2]	$V_O < 0$	-50	mA
		$V_O > V_{CC}$	50	
	DC output voltage		-0.5 to V_{CC} +0.5	V
I_O	DC output source or sink current per output pin	V_O = 0 to V_{CC}	±50	mA
I_{CC} or I_{GND}	DC V_{CC} current		±200	mA
	DC ground current		±200	
T_{STG}	Storage temperature		-65 to 150	°C
P_{TOT}	Power dissipation per package Plastic DIP	Above 70°C:derate linearly by 8mW/K	500	mW
	Power dissipation per package Plastic surface mount (SO)	Above 70°C:derate linearly by 6mW/K	400	mW

NOTES:

1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		V_{CC}	74AC11373				74ACT11373				UNIT
					T_A = +25°C		T_A = -40°C to +85°C		T_A = +25°C		T_A = -40°C to +85°C		
				V	Min	Max	Min	Max	Min	Max	Min	Max	
V_{IH}	High-level input voltage			3.0	2.10		2.10						V
				4.5	3.15		3.15		2.0		2.0		
				5.5	3.85		3.85		2.0		2.0		
V_{IL}	Low-level input voltage			3.0		0.90		0.90					V
				4.5		1.35		1.35		0.8		0.8	
				5.5		1.65		1.65		0.8		0.8	
V_{OH}	High-level output voltage	V_I = V_{IL} or V_{IH}	I_{OH} = -50μA	3.0	2.9		2.9						V
				4.5	4.4		4.4		4.4		4.4		
				5.5	5.4		5.4		5.4		5.4		
			I_{OH} = -4mA	3.0	2.58		2.48						
			I_{OH} = -24mA	4.5	3.94		3.8		3.94		3.8		
				5.5	4.94		4.8		4.94		4.8		
			I_{OH} = -75mA[1]	5.5			3.85				3.85		
V_{OL}	Low-level output voltage	V_I = V_{IL} or V_{IH}	I_{OL} = 50μA	3.0		0.1		0.1					V
				4.5		0.1		0.1		0.1		0.1	
				5.5		0.1		0.1		0.1		0.1	
			I_{OL} = 12mA	3.0		0.36		0.44					
			I_{OL} = 24mA	4.5		0.36		0.44		0.36		0.44	
				5.5		0.36		0.44		0.36		0.44	
			I_{OL} = 75mA[1]	5.5				1.65				1.65	
I_I	Input leakage current	V_I = V_{CC} or GND		5.5		±0.1		±1.0		±0.1		±1.0	μA
I_{OZ}	3-State output off-state current	V_I = V_{IL} or V_{IH}, V_O = V_{CC} or GND		5.5		±0.5		±5.0		±0.5		±5.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC} or GND, I_O = 0		5.5		8.0		80		8.0		80	μA
ΔI_{CC}	Supply current, TTL inputs High[2]	One input at 3.4V, other inputs at V_{CC} or GND		5.5						0.9		1.0	mA

NOTES:
1. Not more than one output should be tested at a time, and the duration of the test should not exceed 10ms.
2. This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0V or V_{CC}.

AC ELECTRICAL CHARACTERISTICS AT 3.3V ±0.3V

SYMBOL	PARAMETER	WAVEFORM	74AC11373					UNIT
			T_A = +25°C			T_A = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay D_n to Q_n	1	1.5 1.5	9.0 8.0	13.1 10.6	1.5 1.5	14.8 11.7	ns
t_{PLH} t_{PHL}	Propagation delay LE to Q_n	4	1.5 1.5	10.0 9.5	14.5 12.8	1.5 1.5	16.3 14.2	ns
t_{PZH} t_{PZL}	Output enable time to High and Low level	2	1.5 1.5	9.0 8.5	13.1 11.6	1.5 1.5	14.7 13.1	ns
t_{PHZ} t_{PLZ}	Output disable time from High and Low level	2	1.5 1.5	9.5 7.5	12.0 10.2	1.5 1.5	12.7 10.8	ns
t_W	LE Pulse Width High or Low	4	5.5			5.5		ns
t_S	Setup time D_n to LE↓	3	4.0			4.0		ns
t_H	Hold time D_n to LE↓	3	2.0			2.0		ns

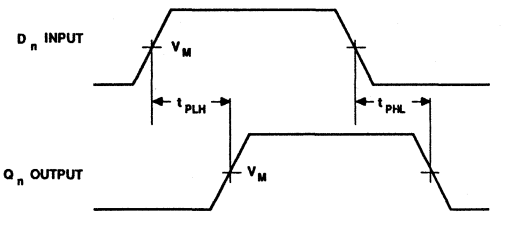
AC ELECTRICAL CHARACTERISTICS AT 5.0V ±0.5V

SYMBOL	PARAMETER	WAVEFORM	74AC11373					UNIT
			T_A = +25°C			T_A = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay D_n to Q_n	1	1.5 1.5	6.0 5.5	8.9 7.6	1.5 1.5	10.3 8.4	ns
t_{PLH} t_{PHL}	Propagation delay LE to Q_n	4	1.5 1.5	6.5 6.5	10.0 9.1	1.5 1.5	11.3 10.2	ns
t_{PZH} t_{PZL}	Output enable time to High and Low level	2	1.5 1.5	6.5 6.0	9.5 8.6	1.5 1.5	10.8 9.7	ns
t_{PHZ} t_{PLZ}	Output disable time from High and Low level	2	1.5 1.5	8.5 6.0	10.6 8.2	1.5 1.5	11.1 8.7	ns
t_W	LE Pulse Width High or Low	4	4.0			4.0		ns
t_S	Setup time D_n to LE↓	3	3.5			3.5		ns
t_H	Hold time D_n to LE↓	3	2.0			2.0		ns

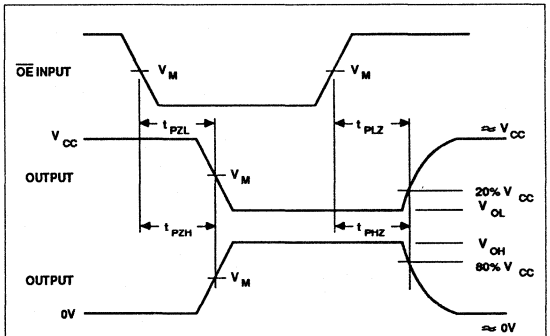
AC ELECTRICAL CHARACTERISTICS AT 5.0V ±0.5V

SYMBOL	PARAMETER	WAVEFORM	74ACT11373					UNIT
			T_A = +25°C			T_A = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay D_n to Q_n	1	1.5 1.5	7.5 6.5	10.3 9.3	1.5 1.5	11.8 10.0	ns
t_{PLH} t_{PHL}	Propagation delay LE to Q_n	4	1.5 1.5	8.5 8.5	11.3 10.9	1.5 1.5	13.0 12.2	ns
t_{PZH} t_{PZL}	Output enable time to High and Low level	2	1.5 1.5	7.0 7.5	10.7 10.9	1.5 1.5	12.5 12.0	ns
t_{PHZ} t_{PLZ}	Output disable time from High and Low level	2	1.5 1.5	10.0 7.5	12.1 9.5	1.5 1.5	12.5 10.1	ns
t_W	LE Pulse Width High or Low	4	5.0			5.0		ns
t_S	Setup time D_n to LE↓	3	3.5			3.5		ns
t_H	Hold time D_n to LE↓	3	3.5			3.5		ns

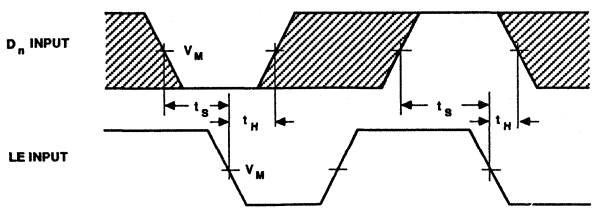
AC WAVEFORMS



Waveform 1. Waveforms Showing the Input (D_n) to Output (Q_n) Propagation Delays

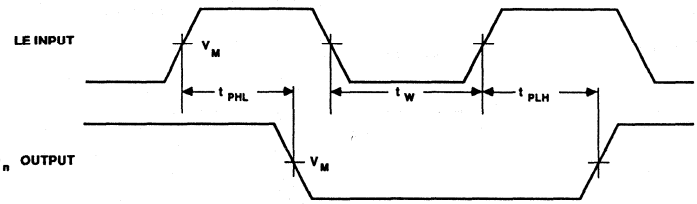


Waveform 2. Waveforms Showing the 3-State Output Enable and Disable Times



Waveform 3. Waveforms Showing the Data Setup and Hold Times for D_n Input to LE Input

AC WAVEFORMS (Continued)

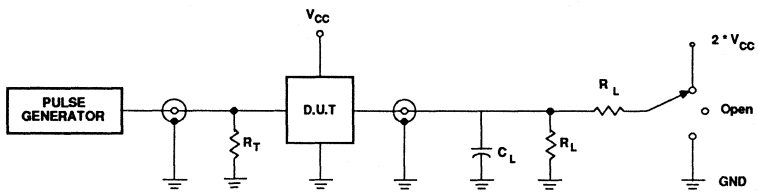


Waveform 4. Waveforms Showing the Latch Enable Input (LE) Pulse Width and the Latch Enable Input to Output (Q_n) Propagation Delays

WAVEFORM CONDITIONS

	INPUTS	OUTPUTS
AC	V_{IN} = GND to V_{CC}, V_M = 50% V_{CC}	$V_{OUT} = V_{OL}$ to V_{OH}
ACT	V_{IN} = GND to 3.0V, V_M = 1.5V	V_M = 50% V_{CC}

TEST CIRCUIT



Test Circuit

TEST	S1
t_{PLH}/t_{PHL}	Open
$t_{PLZ}t_{PZL}$	2*VCC
t_{PHZ}/t_{PZH}	GND

SWITCH POSITION

DEFINITIONS

C_L = Load capacitance, 50pF; includes jig and probe capacitance

R_L = Load resistor, 500Ω

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators

Input pulses: PRR ≤ 10MHz

$t_r = t_f$ = 3ns

74AC/ACT11374

Octal D-Type Flip-Flop; Positive-Edge Trigger; 3–State

Product Specification

FEATURES

- **3-State output buffers**
- **Common 3-State Output Enable**
- **Independent register and 3-State buffer operation**
- **Output capability: ±24 mA**
- **CMOS (AC) and TTL (ACT) voltage level inputs**
- **50Ω incident wave switching**
- **Center-pin V_{CC} and ground configuration to minimize high-speed switching noise**
- **I_{CC} category: MSI**

DESCRIPTION

The 74AC/ACT11374 high-performance CMOS devices combine very high speed and high output drive comparable to the most advanced TTL families.

The 74AC/ACT11374 device is an 8-bit, edge-triggered register coupled to eight 3-State output buffers. The two sections of the device are controlled independently by Clock (CP) and Output Enable ($\overline{OE}$) control gates. The register is fully edge-triggered. Once the set-up requirements are met, when the Clock Pulse (CP) rises the state of each D input is transferred to the corresponding flip-flop's Q output.

GENERAL INFORMATION

SYMBOL	PARAMETER	CONDITIONS T_A = 25°C; GND = 0V; V_{CC} = 5.0V		TYPICAL AC	TYPICAL ACT	UNIT
t_{PLH}/ t_{PHL}	Propagation delay CP to Q_n	C_L = 50pF		6.0	8.5	ns
C_{PD}	Power dissipation capacitance per flip-flop[1]	f = 1MHz; C_L = 50pF	Enabled	75	107	pF
			Disabled	66	96	
C_{IN}	Input capacitance	V_I = 0V or V_{CC}		4.0	4.0	pF
C_{OUT}	Output capacitance	V_I = 0V or V_{CC}; Disabled		10	10	pF
I_{LATCH}	Latch-up current	Per Jedec JC40.2 Standard 17		500	500	mA
f_{MAX}	Maximum clock frequency	C_L = 50pF; V_{CC} = 5.5V		110	70	MHz

Note:

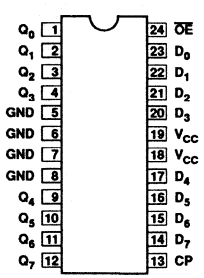
1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_I + \Sigma (C_L \times V_{CC}^2 \times f_O)$ where:
   f_I = input frequency in MHz, C_L = output load capacitance in pF,
   f_O = output frequency in MHz, V_{CC} = supply voltage in V,
   $\Sigma (C_L \times V_{CC}^2 \times f_O)$ = sum of outputs

ORDERING INFORMATION

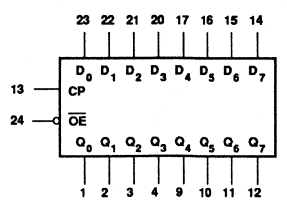
PACKAGES	TEMPERATURE RANGE	ORDER CODE
24-pin plastic DIP (300mil-wide)	-40°C to +85°C	74AC11374N 74ACT11374N
24-pin plastic SO (300mil-wide)	-40°C to +85°C	74AC11374D 74ACT11374D

PIN CONFIGURATION

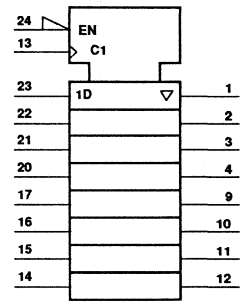
N and D Packages



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



The 3-State output buffers are designed to drive heavily loaded 3-State buses, MOS memories, or MOS microprocessors. The active-Low Output Enable ($\overline{OE}$) controls all eight 3-State buffers independent of the clock operation.

When $\overline{OE}$ is Low, the stored data appears at the outputs. When $\overline{OE}$ is High, the outputs are in the High-impedance "OFF" state, which means they will neither drive nor load the bus.

PIN DESCRIPTION

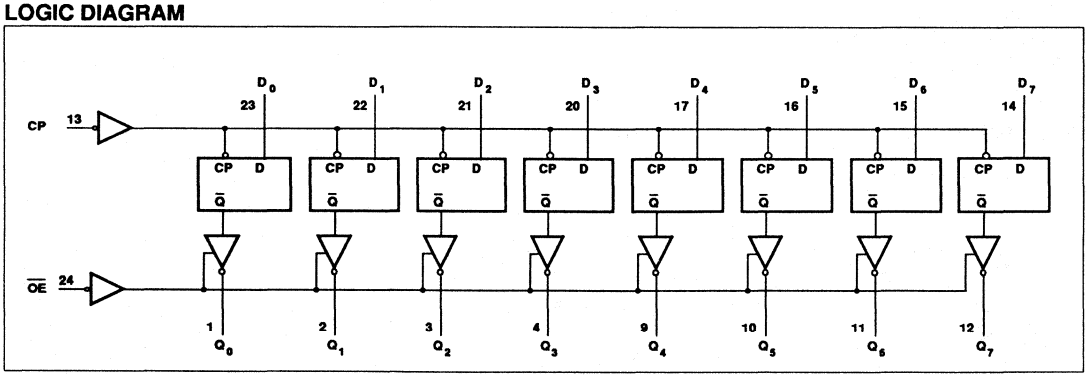
PIN NUMBER	SYMBOL	NAME AND FUNCTION
24	$\overline{OE}$	Output enable
23, 22, 21, 20, 17, 16, 15, 14	D_0 - D_7	Data inputs
1, 2, 3, 4, 9, 10, 11, 12	Q_0 - Q_7	Data outputs
13	CP	Clock input
5, 6, 7, 8	GND	Ground (0V)
18, 19	V_{CC}	Positive supply voltage

FUNCTION TABLE

OPERATING MODES	INPUTS			INTERNAL REGISTER	OUTPUTS
	$\overline{OE}$	CP	D_n		Q_n
Load and read register	L	↑	l	L	L
	L	↑	h	H	H
Disable outputs	H	X	X	X	Z

H = High voltage level steady state
h = High voltage level one set-up time prior to the Low-to-High clock transition
L = Low voltage level steady state
l = Low voltage level one set-up time prior to the Low-to-High clock transition
X = Don't care
Z = High-impedance "OFF" state
↑ = Low-to-High transition

LOGIC DIAGRAM



RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		74AC11374			74ACT11374			UNIT
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	DC supply voltage		3.0[1]	5.0	5.5	4.5	5.0	5.5	V
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
$\Delta t/\Delta v$	Input transition rise or fall rate	Data	0		10	0		10	ns/V
		Output enable	0		5	0		10	
T_A	Operating free-air temperature		-40		+85	-40		+85	°C

NOTE:

1. No electrical or switching characteristics are specified at $V_{CC} < 3V$. Operation between 2V and 3V is not recommended, but within that range, a device output will maintain a previously established logic state.

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	TEST CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 to+7.0	V
I_{IK} or V_I	DC input diode current[2]	$V_I < 0$	-20	mA
		$V_I > V_{CC}$	20	
	DC input voltage		-0.5 to V_{CC} +0.5	V
I_{OK} or V_O	DC output diode current[2]	$V_O < 0$	-50	mA
		$V_O > V_{CC}$	50	
	DC output voltage		-0.5 to V_{CC} +0.5	V
I_O	DC output source or sink current per output pin	V_O = 0 to V_{CC}	±50	mA
I_{CC} or I_{GND}	DC V_{CC} current		±200	mA
	DC ground current		±200	
T_{STG}	Storage temperature		-65 to 150	°C
P_{TOT}	Power dissipation per package Plastic DIP	Above 70°C:derate linearly by 8mW/K	500	mW
	Power dissipation per package Plastic surface mount (SO)	Above 70°C:derate linearly by 6mW/K	400	mW

NOTES:

1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		V_{CC}	74AC11374				74ACT11374				UNIT
					T_A = +25°C		T_A = -40°C to +85°C		T_A = +25°C		T_A = -40°C to +85°C		
				V	Min	Max	Min	Max	Min	Max	Min	Max	
V_{IH}	High-level input voltage			3.0	2.10		2.10						V
				4.5	3.15		3.15		2.0		2.0		
				5.5	3.85		3.85		2.0		2.0		
V_{IL}	Low-level input voltage			3.0		0.90		0.90					V
				4.5		1.35		1.35		0.8		0.8	
				5.5		1.65		1.65		0.8		0.8	
V_{OH}	High-level output voltage	V_I = V_{IL} or V_{IH}	I_{OH} = -50μA	3.0	2.9		2.9						V
				4.5	4.4		4.4		4.4		4.4		
				5.5	5.4		5.4		5.4		5.4		
			I_{OH} = -4mA	3.0	2.58		2.48						
			I_{OH} = -24mA	4.5	3.94		3.8		3.94		3.8		
				5.5	4.94		4.8		4.94		4.8		
			I_{OH} = -75mA[1]	5.5			3.85				3.85		
V_{OL}	Low-level output voltage	V_I = V_{IL} or V_{IH}	I_{OL} = 50μA	3.0		0.1		0.1					V
				4.5		0.1		0.1		0.1		0.1	
				5.5		0.1		0.1		0.1		0.1	
			I_{OL} = 12mA	3.0		0.36		0.44					
			I_{OL} = 24mA	4.5		0.36		0.44		0.36		0.44	
				5.5		0.36		0.44		0.36		0.44	
			I_{OL} = 75mA[1]	5.5				1.65				1.65	
I_I	Input leakage current	V_I = V_{CC} or GND		5.5		±0.1		±1.0		±0.1		±1.0	μA
I_{OZ}	3-State output off-state current	V_I = V_{IL} or V_{IH}, V_O = V_{CC} or GND		5.5		±0.5		±5.0		±0.5		±5.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC} or GND, I_O = 0		5.5		8.0		80		8.0		80	μA
ΔI_{CC}	Supply current, TTL inputs High[2]	One input at 3.4V, other inputs at V_{CC} or GND		5.5						0.9		1.0	mA

NOTES:
1. Not more than one output should be tested at a time, and the duration of the test should not exceed 10ms.
2. This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0V or V_{CC}.

AC ELECTRICAL CHARACTERISTICS AT 3.3V ±0.3V

SYMBOL	PARAMETER	WAVEFORM	74AC11374					UNIT
			T_A = +25°C			T_A = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	1	75	90		75		MHz
t_{PLH} t_{PHL}	Propagation delay CP to Q_n	1	1.5 1.5	9.5 9.0	12.5 12.6	1.5 1.5	14.2 14.0	ns
t_{PZH} t_{PZL}	Output enable time to High and Low level	2	1.5 1.5	8.0 8.0	10.9 11.1	1.5 1.5	12.3 12.3	ns
t_{PHZ} t_{PLZ}	Output disable time from High and Low level	2	1.5 1.5	10.0 8.0	12.1 10.7	1.5 1.5	12.5 11.6	ns
t_W	Clock pulse width High or Low	1	6.5			6.5		ns
t_S	Setup time D_n to CP	3	2.5			2.5		ns
t_H	Hold time D_n to CP	3	4.5			4.5		ns

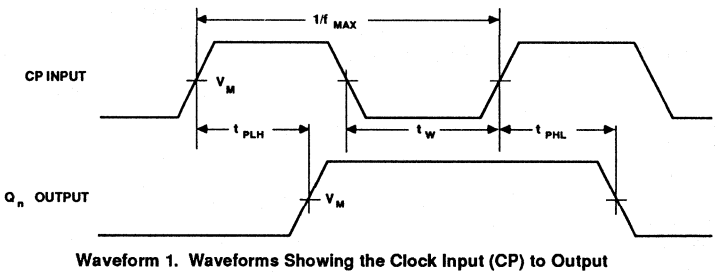
AC ELECTRICAL CHARACTERISTICS AT 5.0V ±0.5V

SYMBOL	PARAMETER	WAVEFORM	74AC11374					UNIT
			T_A = +25°C			T_A = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	1	95	110		95		MHz
t_{PLH} t_{PHL}	Propagation delay CP to Q_n	1	1.5 1.5	6.5 5.5	9.0 9.1	1.5 1.5	10.2 10.1	ns
t_{PZH} t_{PZL}	Output enable time to High and Low level	2	1.5 1.5	5.5 5.5	8.0 8.4	1.5 1.5	9.1 9.4	ns
t_{PHZ} t_{PLZ}	Output disable time from High and Low level	2	1.5 1.5	9.0 6.0	11.0 8.6	1.5 1.5	11.2 9.2	ns
t_W	Clock pulse width High or Low	1	5.0			5.0		ns
t_S	Setup time D_n to CP	3	2.5			2.5		ns
t_H	Hold time D_n to CP	3	3.5			3.5		ns

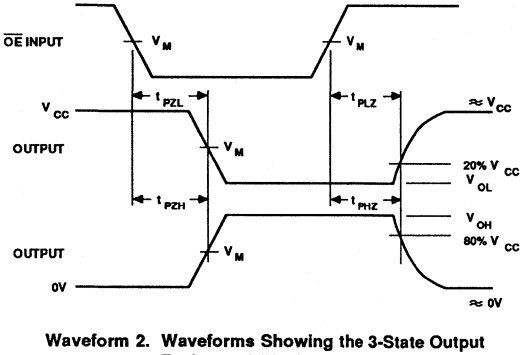
AC ELECTRICAL CHARACTERISTICS AT 5.0V ±0.5V

SYMBOL	PARAMETER	WAVEFORM	74ACT11374					UNIT
			T_A = +25°C			T_A = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	1	55	70		55		MHz
t_{PLH} t_{PHL}	Propagation delay CP to Q_n	1	1.5 1.5	8.5 8.5	10.7 11.3	1.5 1.5	12.4 13.0	ns
t_{PZH} t_{PZL}	Output enable time to High and Low level	2	1.5 1.5	7.5 7.5	11.0 11.0	1.5 1.5	12.3 12.3	ns
t_{PHZ} t_{PLZ}	Output disable time from High and Low level	2	1.5 1.5	11.0 8.0	12.7 10.0	1.5 1.5	13.2 10.8	ns
t_W	Clock pulse width High or Low	1	9.0			9.0		ns
t_S	Setup time D_n to CP	3	3.0			3.0		ns
t_H	Hold time D_n to CP	3	5.5			5.5		ns

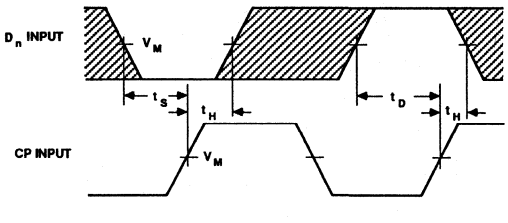
AC WAVEFORMS



Waveform 1. Waveforms Showing the Clock Input (CP) to Output (Q_n) Propagation Delays and Clock Input (CP) Pulse Width



Waveform 2. Waveforms Showing the 3-State Output Enable and Disable Times

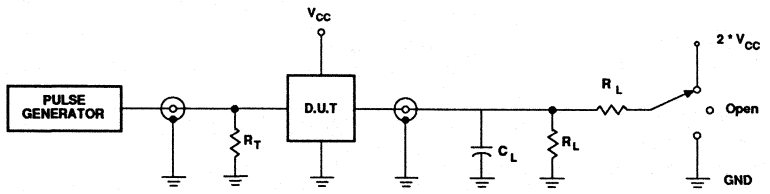


Waveform 3. Waveforms Showing the Data Set-up and Hold Times for D_n Input to CP Input

WAVEFORM CONDITIONS

	INPUTS	OUTPUTS
AC	V_{IN} = GND to V_{CC}, V_M = 50% V_{CC}	V_{OUT} = V_{OL} to V_{OH}
ACT	V_{IN} = GND to 3.0V, V_M = 1.5V	V_M = 50% V_{CC}

TEST CIRCUIT



Test Circuit

TEST	S1
t_{PLH}/t_{PHL}	Open
$t_{PLZ}t_{PZL}$	2*VCC
t_{PHZ}/t_{PZH}	GND

SWITCH POSITION

DEFINITIONS

C_L = Load capacitance, 50pF; includes jig and probe capacitance

R_L = Load resistor, 500Ω

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators

Input pulses: PRR ≤ 10MHz

$t_r = t_f$ = 3ns

74AC/ACT11377

Octal D-Type Flip-Flop with Enable

Objective Specification

FEATURES

- **Eight edge-triggered D-type flip-flops**
- **Buffered common clock**
- **Buffered clock enable**
- **Output capability: ±24 mA**
- **CMOS (AC) and TTL (ACT) voltage level inputs**
- **50Ω incident wave switching**
- **Center-pin V_{CC} and ground configuration to minimize high-speed switching noise**
- **I_{CC} category: MSI**

DESCRIPTION

The 74AC/ACT11377 high-performance CMOS devices combine very high speed and high output drive comparable to the most advanced TTL families.

The 74AC/ACT11377 provides eight positive edge-triggered D-type flip-flops with individual Data inputs and Q outputs. The common buffered Clock (CP) input loads all flip-flops simultaneously when the Enable ($\overline{E}$) is Low.

The $\overline{E}$ input must be stable one setup time prior to the Low-to-High clock transition for predictable operation.

GENERAL INFORMATION

SYMBOL	PARAMETER	CONDITIONS T_A = 25°C; GND = 0V; V_{CC} = 5.0V	TYPICAL		UNIT
			AC	ACT	
t_{PLH}/t_{PHL}	Propagation delay CP to Q_n	C_L = 50pF	5.6	6.4	ns
C_{PD}	Power dissipation capacitance per flip-flop[1]	f = 1MHz; C_L = 50pF	316	316	pF
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	4.0	4.0	pF
I_{LATCH}	Latch-up current	Per Jedec JC40.2 Standard 17	500	500	mA
f_{MAX}	Maximum clock frequency	C_L = 50pF	110	110	MHz

Note:

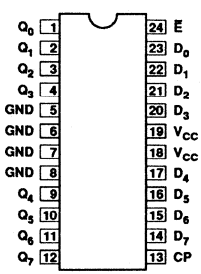
1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_I + \Sigma (C_L \times V_{CC}^2 \times f_O)$ where:
   f_I = input frequency in MHz, C_L = output load capacitance in pF,
   f_O = output frequency in MHz, V_{CC} = supply voltage in V,
   $\Sigma (C_L \times V_{CC}^2 \times f_O)$ = sum of outputs

ORDERING INFORMATION

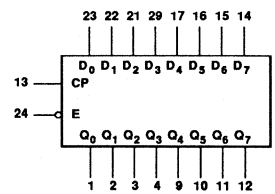
PACKAGES	TEMPERATURE RANGE	ORDER CODE
24-pin plastic DIP (300mil-wide)	-40°C to +85°C	74AC11377N 74ACT11377N
24-pin plastic SO (300mil-wide)	-40°C to +85°C	74AC11377D 74ACT11377D

PIN CONFIGURATION

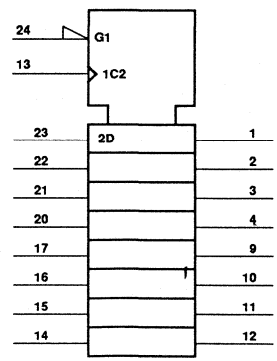
N and D Packages



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



PIN DESCRIPTION

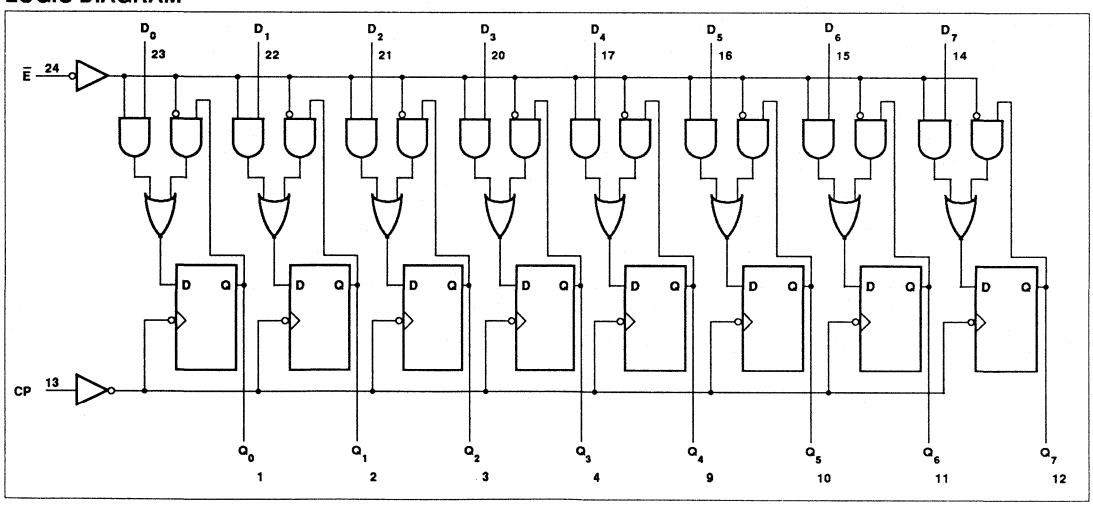
PIN NUMBER	SYMBOL	NAME AND FUNCTION
24	$\overline{E}$	Enable input (active-Low)
13	CP	Clock pulse input
23, 22, 21, 20, 17, 16, 15, 14	D_0 - D_7	Data inputs
1, 2, 3, 4, 9, 10, 11, 12	Q_0 - Q_7	Data outputs
5, 6, 7, 8	GND	Ground (0V)
18, 19	V_{CC}	Positive supply voltage

MODE SELECT—FUNCTION TABLE

OPERATING MODE	INPUTS			OUTPUTS
	CP	$\overline{E}$	D_n	Q_n
Load "1"	↑	l	h	H
Load "0"	↑	l	l	L
Hold (do nothing)	↑	h	X	no change
	X	H	X	no change

H = High voltage level steady state
h = High voltage level one setup time prior to the Low-to-High clock transition
L = Low voltage level steady state
l = Low voltage level one setup time prior to the Low-to-High clock transition
X = Don't care
↑ =Low-to-High clock transition

LOGIC DIAGRAM



RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	74AC11377			74ACT11377			UNIT
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	DC supply voltage	3.0[1]	5.0	5.5	4.5	5.0	5.5	V
V_I	Input voltage	0		V_{CC}	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	0		V_{CC}	V
$\Delta t/\Delta v$	Input transition rise or fall rate	0		10	0		10	ns/V
T_A	Operating free-air temperature	-40		+85	-40		+85	°C

NOTE:
1. No electrical or switching characteristics are specified at $V_{CC} < 3V$. Operation between 2V and 3V is not recommended, but within that range, a device output will maintain a previously established logic state.

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	TEST CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 to+7.0	V
I_{IK} or V_I	DC input diode current[2]	$V_I < 0$	-20	mA
		$V_I > V_{CC}$	20	
	DC input voltage		-0.5 to V_{CC} +0.5	V
I_{OK} or V_O	DC output diode current[2]	$V_O < 0$	-50	mA
		$V_O > V_{CC}$	50	
	DC output voltage		-0.5 to V_{CC} +0.5	V
I_O	DC output source or sink current per output pin	V_O = 0 to V_{CC}	±50	mA
I_{CC} or I_{GND}	DC V_{CC} current		±200	mA
	DC ground current		±200	
T_{STG}	Storage temperature		-65 to 150	°C
P_{TOT}	Power dissipation per package Plastic DIP	Above 70°C:derate linearly by 8mW/K	500	mW
	Power dissipation per package Plastic surface mount (SO)	Above 70°C:derate linearly by 6mW/K	400	mW

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		V_{CC}	74AC11377				74ACT11377				UNIT
					T_A = +25°C		T_A = -40°C to +85°C		T_A = +25°C		T_A = -40°C to +85°C		
				V	Min	Max	Min	Max	Min	Max	Min	Max	
V_{IH}	High-level input voltage			3.0	2.10		2.10						V
				4.5	3.15		3.15		2.0		2.0		
				5.5	3.85		3.85		2.0		2.0		
V_{IL}	Low-level input voltage			3.0		0.90		0.90					V
				4.5		1.35		1.35		0.8		0.8	
				5.5		1.65		1.65		0.8		0.8	
V_{OH}	High-level output voltage	V_I = V_{IL} or V_{IH}	I_{OH} = -50μA	3.0	2.9		2.9						V
				4.5	4.4		4.4		4.4		4.4		
				5.5	5.4		5.4		5.4		5.4		
			I_{OH} = -4mA	3.0	2.58		2.48						
			I_{OH} = -24mA	4.5	3.94		3.8		3.94		3.8		
				5.5	4.94		4.8		4.94		4.8		
			I_{OH} = -75mA[1]	5.5			3.85				3.85		
V_{OL}	Low-level output voltage	V_I = V_{IL} or V_{IH}	I_{OL} = 50μA	3.0		0.1		0.1					V
				4.5		0.1		0.1		0.1		0.1	
				5.5		0.1		0.1		0.1		0.1	
			I_{OL} = 12mA	3.0		0.36		0.44					
			I_{OL} = 24mA	4.5		0.36		0.44		0.36		0.44	
				5.5		0.36		0.44		0.36		0.44	
			I_{OL} = 75mA[1]	5.5				1.65				1.65	
I_I	Input leakage current	V_I = V_{CC} or GND		5.5		±0.1		±1.0		±0.1		±1.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC} or GND, I_O = 0		5.5		8.0		80		8.0		80	μA
ΔI_{CC}	Supply current, TTL inputs High[2]	One input at 3.4V, other inputs at V_{CC} or GND		5.5						0.9		1.0	mA

NOTES:
1. Not more than one output should be tested at a time, and the duration of the test should not exceed 10ms.
2. This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0V or V_{CC}.

74AC/ACT11378

Hex D-Type Flip-Flop w/ Enable; Positive-Edge Trigger

Objective Specification

FEATURES

- **Output capability: ±24 mA**
- **Positive edge-triggered clock**
- **Common asynchronous Enable ($\overline{E}$) input**
- **Center-pin V_{CC} and ground configuration to minimize high-speed switching noise**
- **I_{CC} category: MSI**

DESCRIPTION

The 74AC/ACT11378 high-performance CMOS devices combine very high speed and high output drive comparable to the most advanced TTL families.

The 74AC/ACT11378 provides six edge-triggered D-type flip-flops with individual Data inputs (D_0 - D_5) and Q outputs (Q_0 - Q_5). The flip-flops load the data on the rising edge of the common clock (CP) providing that the common Enable ($\overline{E}$) is held Low. When the Enable is High, the flip-flops hold their previous state.

GENERAL INFORMATION

SYMBOL	PARAMETER	CONDITIONS T_A = 25°C; GND = 0V V_{CC} = 5.0V	TYPICAL		UNIT
			AC	ACT	
t_{PLH}/ t_{PHL}	Propagation delay CP to Q_n	C_L = 50pF	4.3	5.2	ns
C_{PD}	Power dissipation capacitance per flip-flop[1]	f = 1MHz; C_L = 50pF	30	31	pF
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	4.0	4.0	pF
I_{LATCH}	Latch-up current	Per Jedec JC40.2 Standard 17	500	500	mA
f_{MAX}	Maximum clock frequency	C_L = 50 pF	165	160	MHz

Note:

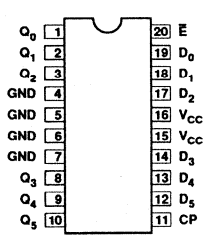
1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_I + \Sigma (C_L \times V_{CC}^2 \times f_O)$ where:
   f_I = input frequency in MHz, C_L = output load capacitance in pF,
   f_O = output frequency in MHz, V_{CC} = supply voltage in V,
   $\Sigma (C_L \times V_{CC}^2 \times f_O)$ = sum of outputs

ORDERING INFORMATION

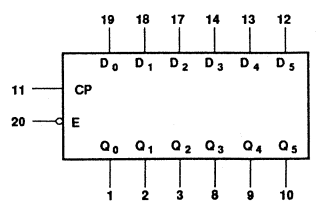
PACKAGES	TEMPERATURE RANGE	ORDER CODE
20-pin plastic DIP (300mil-wide)	-40°C to +85°C	74AC11378N 74ACT11378N
20-pin plastic SO (300mil-wide)	-40°C to +85°C	74AC11378D 74ACT11378D

PIN CONFIGURATION

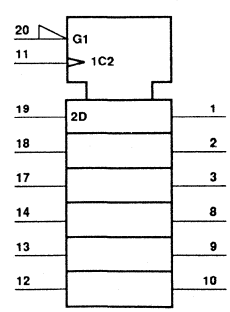
N and D Packages



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



Hex D-Type Flip-Flop w/Enable; Positive-Edge Trigger

74AC/ACT11378

PIN DESCRIPTION

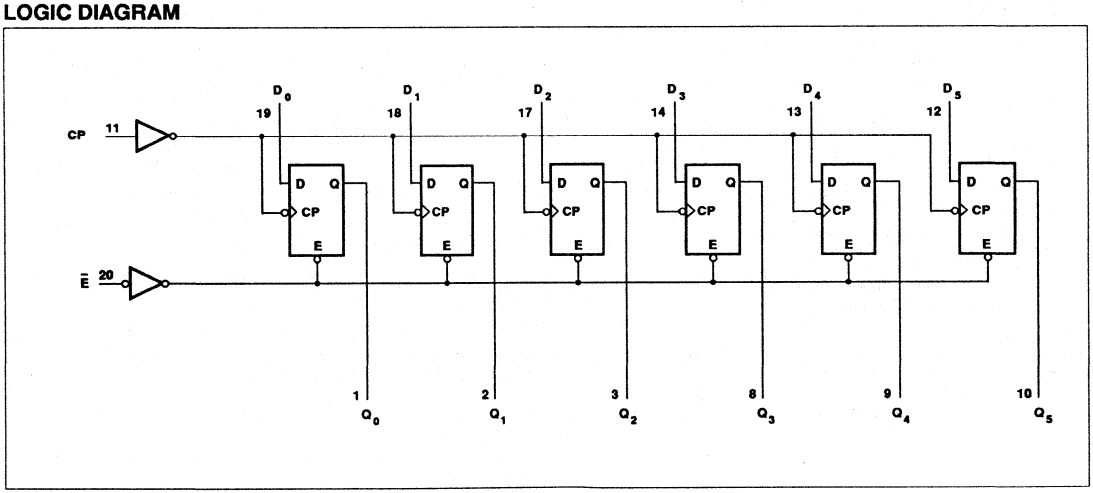
PIN NUMBER	SYMBOL	NAME AND FUNCTION
19, 18, 17, 14, 13, 12	D_0 - D_5	Data inputs
1, 2, 3, 8, 9, 10	Q_0 - Q_5	Data outputs
20	$\overline{E}$	Data enable input (active Low)
11	CP	Clock input
4, 5, 6, 7	GND	Ground (0V)
15, 16	V_{CC}	Positive supply voltage

FUNCTION TABLE

OPERATING MODE	INPUTS			OUTPUTS
	$\overline{E}$	CP	D_n	Q_n
Disabled input (hold)	H	↑	X	NC
Load "1" (set)	L	↑	h	H
Load "0" (reset)	L	↑	l	L

H = High voltage level steady state
h = High voltage level one set-up time prior to the Low-to-High clock transition
L = Low voltage level steady state
l = Low voltage level one set-up time prior to the Low-to-High clock transition
X = Don't care
NC = No Change
↑ = Low-to-High clock transition

LOGIC DIAGRAM



RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	74AC11378			74ACT11378			UNIT
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	DC supply voltage	3.0[1]	5.0	5.5	4.5	5.0	5.5	V
V_I	Input voltage	0		V_{CC}	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	0		V_{CC}	V
$\Delta t/\Delta v$	Input transition rise or fall rate	0		10	0		10	ns/V
T_A	Operating free-air temperature	-40		+85	-40		+85	°C

NOTE:
1. No electrical or switching characteristics are specified at $V_{CC} < 3V$. Operation between 2V and 3V is not recommended, but within that range, a device output will maintain a previously established logic state.

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	TEST CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 to+7.0	V
I_{IK} or V_I	DC input diode current[2]	$V_I < 0$	-20	mA
		$V_I > V_{CC}$	20	
	DC input voltage		-0.5 to V_{CC} +0.5	V
I_{OK} or V_O	DC output diode current[2]	$V_O < 0$	-50	mA
		$V_O > V_{CC}$	50	
	DC output voltage		-0.5 to V_{CC} +0.5	V
I_O	DC output source or sink current per output pin	V_O = 0 to V_{CC}	±50	mA
I_{CC} or I_{GND}	DC V_{CC} current		±150	mA
	DC ground current		±150	
T_{STG}	Storage temperature		-65 to 150	°C
P_{TOT}	Power dissipation per package Plastic DIP	Above 70°C:derate linearly by 8mW/K	500	mW
	Power dissipation per package Plastic surface mount (SO)	Above 70°C:derate linearly by 6mW/K	400	mW

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		V_{CC}	74AC11378				74ACT11378				UNIT
					T_A = +25°C		T_A = -40°C to +85°C		T_A = +25°C		T_A = -40°C to +85°C		
				V	Min	Max	Min	Max	Min	Max	Min	Max	
V_{IH}	High-level input voltage			3.0	2.10		2.10						V
				4.5	3.15		3.15		2.0		2.0		
				5.5	3.85		3.85		2.0		2.0		
V_{IL}	Low-level input voltage			3.0		0.90		0.90					V
				4.5		1.35		1.35		0.8		0.8	
				5.5		1.65		1.65		0.8		0.8	
V_{OH}	High-level output voltage	V_I = V_{IL} or V_{IH}	I_{OH} = -50μA	3.0	2.9		2.9						V
				4.5	4.4		4.4		4.4		4.4		
				5.5	5.4		5.4		5.4		5.4		
			I_{OH} = -4mA	3.0	2.58		2.48						
			I_{OH} = -24mA	4.5	3.94		3.8		3.94		3.8		
				5.5	4.94		4.8		4.94		4.8		
			I_{OH} = -75mA[1]	5.5			3.85				3.85		
V_{OL}	Low-level output voltage	V_I = V_{IL} or V_{IH}	I_{OL} = 50μA	3.0		0.1		0.1					V
				4.5		0.1		0.1		0.1		0.1	
				5.5		0.1		0.1		0.1		0.1	
			I_{OL} = 12mA	3.0		0.36		0.44					
			I_{OL} = 24mA	4.5		0.36		0.44		0.36		0.44	
				5.5		0.36		0.44		0.36		0.44	
			I_{OL} = 75mA[1]	5.5				1.65				1.65	
I_I	Input leakage current	V_I = V_{CC} or GND		5.5		±0.1		±1.0		±0.1		±1.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC} or GND, I_O = 0		5.5		8.0		80		8.0		80	μA
ΔI_{CC}	Supply current, TTL inputs High[2]	One input at 3.4V, other inputs at V_{CC} or GND		5.5						0.9		1.0	mA

NOTES:
1. Not more than one output should be tested at a time, and the duration of the test should not exceed 10ms.
2. This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0V or V_{CC}.

74AC/ACT11379

Quad D-Type Flip-Flop w/ Data Enable

Preliminary Specification

FEATURES

- **Output capability: ±24 mA**
- **Edge-triggered D-type inputs**
- **Positive edge-triggered clock**
- **Common asynchronous Enable ($\overline{E}$) input**
- **Center-pin V_{CC} and ground configuration to minimize high-speed switching noise**
- **I_{CC} category: MSI**

DESCRIPTION

The 74AC/ACT11379 high-performance CMOS devices combine very high speed and high output drive comparable to the most advanced TTL families.

The 74AC/ACT11379 provides four edge-triggered D-type flip-flops with individual Data inputs (D_0 - D_3) and Q and $\overline{Q}$ outputs. The flip-flops load the data on the rising edge of the common clock (CP) providing that the common Enable ($\overline{E}$) is held Low. When the Enable is High, the flip-flops hold their previous state.

GENERAL INFORMATION

SYMBOL	PARAMETER	CONDITIONS T_A = 25°C; GND = 0V; V_{CC} = 5.0V	TYPICAL		UNIT
			AC	ACT	
t_{PLH}/ t_{PHL}	Propagation delay CP to Q_n or $\overline{Q}_n$	C_L = 50pF	4.8	5.3	ns
C_{PD}	Power dissipation capacitance per flip-flop[1]	f = 1MHz; C_L = 50pF	38	38	pF
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	4.0	4.0	pF
I_{LATCH}	Latch-up current	Per Jedec JC40.2 Standard 17	500	500	mA
f_{MAX}	Maximum clock frequency	C_L = 50pF	165	165	MHz

Note:

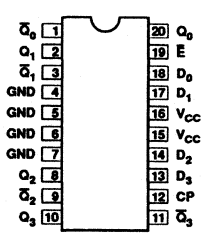
1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_I + \Sigma (C_L \times V_{CC}^2 \times f_O)$ where:
   f_I = input frequency in MHz, C_L = output load capacitance in pF,
   f_O = output frequency in MHz, V_{CC} = supply voltage in V,
   $\Sigma (C_L \times V_{CC}^2 \times f_O)$ = sum of outputs

ORDERING INFORMATION

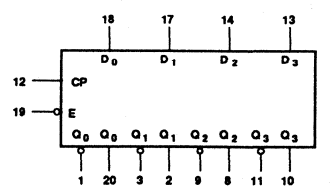
PACKAGES	TEMPERATURE RANGE	ORDER CODE
20-pin plastic DIP (300mil-wide)	-40°C to +85°C	74AC11379N 74ACT11379N
20-pin plastic SO (300mil-wide)	-40°C to +85°C	74AC11379D 74ACT11379D

PIN CONFIGURATION

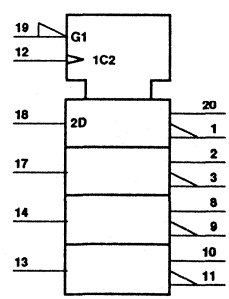
N and D Packages



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



PIN DESCRIPTION

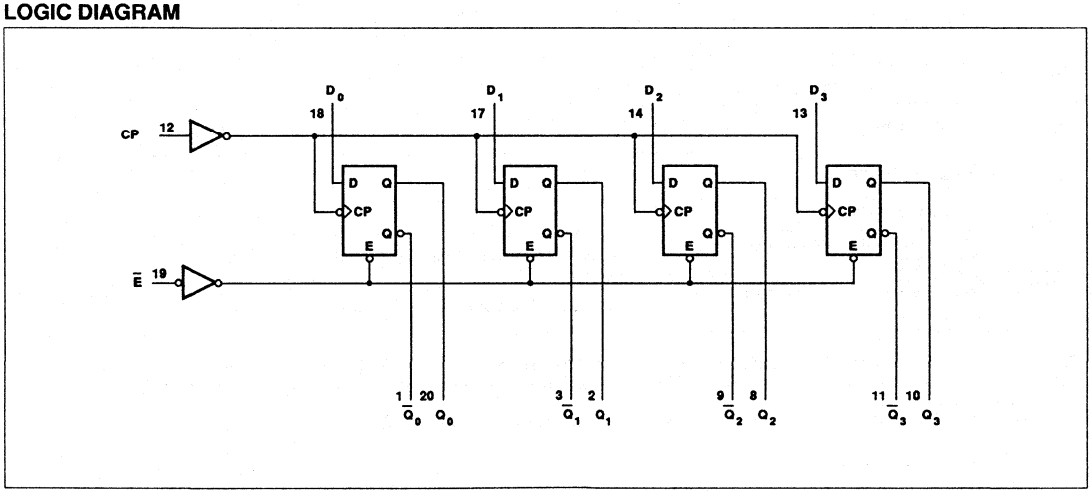
PIN NUMBER	SYMBOL	NAME AND FUNCTION
18, 17, 14, 13	D_0 - D_3	Data inputs
20, 2, 8, 10	Q_0 - Q_3	Data outputs
1, 3, 9, 11	$\overline{Q}_0$ - $\overline{Q}_3$	Data outputs (complements of Q_n outputs)
19	$\overline{E}$	Data enable input (active Low)
12	CP	Clock input
4, 5, 6, 7	GND	Ground (0V)
15, 16	V_{CC}	Positive supply voltage

FUNCTION TABLE

OPERATING MODE	INPUTS			OUTPUTS	
	$\overline{E}$	CP	D_n	Q_n	$\overline{Q}_n$
Disabled input (hold)	H	↑	X	NC	NC
Load "1" (set)	L	↑	h	H	L
Load "0" (reset)	L	↑	l	L	H

H = High voltage level steady state
h = High voltage level one set-up time prior to the Low-to-High clock transition
L = Low voltage level steady state
l = Low voltage level one set-up time prior to the Low-to-High clock transition
X = Don't care
NC = No Change
↑ = Low-to-High clock transition

LOGIC DIAGRAM



RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	74AC11379			74ACT11379			UNIT
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	DC supply voltage	3.0[1]	5.0	5.5	4.5	5.0	5.5	V
V_I	Input voltage	0		V_{CC}	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	0		V_{CC}	V
$\Delta t/\Delta v$	Input transition rise or fall rate	0		10	0		10	ns/V
T_A	Operating free-air temperature	-40		+85	-40		+85	°C

NOTE:
1. No electrical or switching characteristics are specified at V_{CC} < 3V. Operation between 2V and 3V is not recommended, but within that range, a device output will maintain a previously established logic state.

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	TEST CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 to+7.0	V
I_{IK} or V_I	DC input diode current[2]	$V_I < 0$	-20	mA
		$V_I > V_{CC}$	20	
	DC input voltage		-0.5 to V_{CC} +0.5	V
I_{OK} or V_O	DC output diode current[2]	$V_O < 0$	-50	mA
		$V_O > V_{CC}$	50	
	DC output voltage		-0.5 to V_{CC} +0.5	V
I_O	DC output source or sink current per output pin	V_O = 0 to V_{CC}	±50	mA
I_{CC} or I_{GND}	DC V_{CC} current		±200	mA
	DC ground current		±200	
T_{STG}	Storage temperature		-65 to 150	°C
P_{TOT}	Power dissipation per package Plastic DIP	Above 70°C:derate linearly by 8mW/K	500	mW
	Power dissipation per package Plastic surface mount (SO)	Above 70°C:derate linearly by 6mW/K	400	mW

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		V_{CC}	74AC11379				74ACT11379				UNIT
					T_A = +25°C		T_A = -40°C to +85°C		T_A = +25°C		T_A = -40°C to +85°C		
				V	Min	Max	Min	Max	Min	Max	Min	Max	
V_{IH}	High-level input voltage			3.0	2.10		2.10						V
				4.5	3.15		3.15		2.0		2.0		
				5.5	3.85		3.85		2.0		2.0		
V_{IL}	Low-level input voltage			3.0		0.90		0.90					V
				4.5		1.35		1.35		0.8		0.8	
				5.5		1.65		1.65		0.8		0.8	
V_{OH}	High-level output voltage	V_I = V_{IL} or V_{IH}	I_{OH} = -50μA	3.0	2.9		2.9						V
				4.5	4.4		4.4		4.4		4.4		
				5.5	5.4		5.4		5.4		5.4		
			I_{OH} = -4mA	3.0	2.58		2.48						
			I_{OH} = -24mA	4.5	3.94		3.8		3.94		3.8		
				5.5	4.94		4.8		4.94		4.8		
			I_{OH} = -75mA[1]	5.5			3.85				3.85		
V_{OL}	Low-level output voltage	V_I = V_{IL} or V_{IH}	I_{OL} = 50μA	3.0		0.1		0.1					V
				4.5		0.1		0.1		0.1		0.1	
				5.5		0.1		0.1		0.1		0.1	
			I_{OL} = 12mA	3.0		0.36		0.44					
			I_{OL} = 24mA	4.5		0.36		0.44		0.36		0.44	
				5.5		0.36		0.44		0.36		0.44	
			I_{OL} = 75mA[1]	5.5				1.65				1.65	
I_I	Input leakage current	V_I = V_{CC} or GND		5.5		±0.1		±1.0		±0.1		±1.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC} or GND, I_O = 0		5.5		8.0		80		8.0		80	μA
ΔI_{CC}	Supply current, TTL inputs High[2]	One input at 3.4V, other inputs at V_{CC} or GND		5.5						0.9		1.0	mA

NOTES:
1. Not more than one output should be tested at a time, and the duration of the test should not exceed 10ms.
2. This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0V or V_{CC}.

AC ELECTRICAL CHARACTERISTICS AT 3.3V ±0.3V

SYMBOL	PARAMETER	WAVEFORM	74AC11379					UNIT
			T_A = +25°C			T_A = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	1	130	155		130		MHz
t_{PLH} t_{PHL}	Propagation delay CP to Q_n, $\overline{Q}_n$	1	1.5 1.5	5.0 8.3	7.1 10.4	1.5 1.5	7.7 11.2	ns
t_S	Setup time, High or Low D_n to CP	1	7.0			7.0		ns
t_H	Hold time, High or Low CP to D_n	1	0.0			0.0		ns
t_S	Setup time, High or Low $\overline{E}$ to CP	1	4.5			4.5		ns
t_H	Hold time, High or Low CP to $\overline{E}$	1	0.0			0.0		ns
t_W	Clock pulse width High or Low	1	4.0			4.0		ns

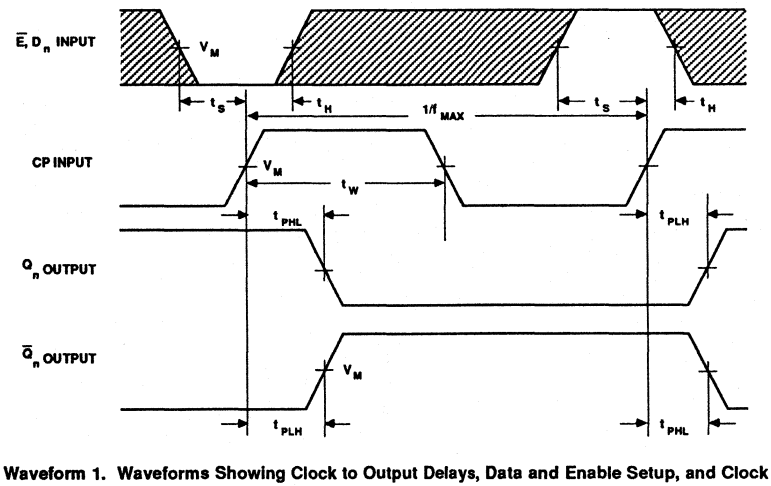
AC ELECTRICAL CHARACTERISTICS AT 5.0V ±0.5V

SYMBOL	PARAMETER	WAVEFORM	74AC11379					UNIT
			T_A = +25°C			T_A = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	1	140	165		140		MHz
t_{PLH} t_{PHL}	Propagation delay CP to Q_n, $\overline{Q}_n$	1	1.5 1.5	3.8 5.9	5.3 7.6	1.5 1.5	5.8 8.4	ns
t_S	Setup time, High or Low D_n to CP	1	5.0			5.0		ns
t_H	Hold time, High or Low CP to D_n	1	0.0			0.0		ns
t_S	Setup time, High or Low $\overline{E}$ to CP	1	3.0			3.0		ns
t_H	Hold time, High or Low CP to $\overline{E}$	1	0.5			0.5		ns
t_W	Clock pulse width High or Low	1	3.5			3.5		ns

AC ELECTRICAL CHARACTERISTICS AT 5.0V ±0.5V

SYMBOL	PARAMETER	WAVEFORM	74ACT11379					UNIT
			T_A = +25°C			T_A = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	1	140	165		140		MHz
t_{PLH} t_{PHL}	Propagation delay CP to Q_n, $\overline{Q}_n$	1	1.5 1.5	4.3 6.4	5.6 7.9	1.5 1.5	6.1 8.7	ns
t_S	Setup time, High or Low D_n to CP	1	4.5			4.5		ns
t_H	Hold time, High or Low CP to D_n	1	0.5			0.5		ns
t_S	Setup time, High or Low $\overline{E}$ to CP	1	3.0			3.0		ns
t_H	Hold time, High or Low CP to $\overline{E}$	1	1.0			1.0		ns
t_W	Clock pulse width High or Low	1	3.5			3.5		ns

AC WAVEFORMS

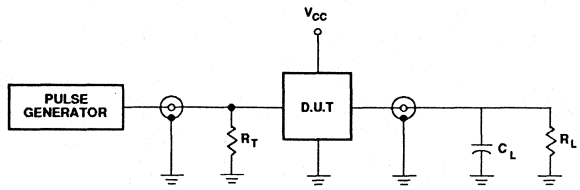


Waveform 1. Waveforms Showing Clock to Output Delays, Data and Enable Setup, and Clock Pulse Width

WAVEFORM CONDITIONS

	INPUTS	OUTPUTS
AC	V_{IN} = GND to V_{CC}, V_M = 50% V_{CC}	V_{OUT} = V_{OL} to V_{OH}
ACT	V_{IN} = GND to 3.0V, V_M = 1.5V	V_M = 50% V_{CC}

TEST CIRCUIT



Test Circuit

DEFINITIONS

C_L = Load capacitance, 50pF; includes jig and probe capacitance

R_L = Load resistor, 500Ω

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators

Input pulses: PRR ≤ 10MHz

$t_r = t_f$ = 3ns

74AC/ACT11470

Octal Transceiver/Register with Dual Enable; 3-State

Objective Specification

FEATURES

- **Combines '245 and '374 type functions in one chip**
- **8-bit octal transceiver with D-type flip-flops**
- **3-State buffers**
- **Output capability: ±24 mA**
- **CMOS (AC) and TTL (ACT) voltage level inputs**
- **50Ω incident wave switching**
- **Center-pin V_{CC} and ground configuration to minimize high-speed switching noise**
- **I_{CC} category: MSI**

DESCRIPTION

The 74AC/ACT11470 high-performance CMOS devices combine very high speed and high output drive comparable to the most advanced TTL families.

The 74AC/ACT11470 Octal Transceiver/Register contains two sets of D-type flip-flops for temporary storage of data flowing in either direction. Dual Enable ($\overline{E}_{AB}$, $\overline{E}_{BA}$) and Output Enable ($\overline{OE}_{AB}$, $\overline{OE}_{BA}$) inputs are provided for each register to permit independent control of inputting and outputting in either direction of data flow.

GENERAL INFORMATION

SYMBOL	PARAMETER	CONDITIONS T_A = 25°C; GND = 0V; V_{CC} = 5.0V		TYPICAL AC	TYPICAL ACT	UNIT
t_{PLH}/t_{PHL}	Propagation delay CP_{XX} to A_n or B_n	C_L = 50pF		5.2	6.7	ns
C_{PD}	Power dissipation capacitance per register[1]	f = 1MHz;	Enabled	155	160	pF
		C_L = 50pF	Disabled	35	40	
C_{IN}	Input capacitance	V_I = 0V or V_{CC}		4.5	4.5	pF
$C_{I/O}$	I/O capacitance	$V_{I/O}$ = 0V or V_{CC}; Disabled		12.0	12.0	pF
I_{LATCH}	Latch-up current	Per Jedec JC40.2 Standard 17		500	500	mA
f_{MAX}	Maximum clock frequency	C_L = 50pF		125	125	MHz

Note:

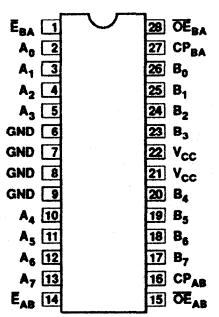
1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_O)$ where:
   f_i = input frequency in MHz, C_L = output load capacitance in pF,
   f_O = output frequency in MHz, V_{CC} = supply voltage in V,
   $\Sigma (C_L \times V_{CC}^2 \times f_O)$ = sum of outputs

ORDERING INFORMATION

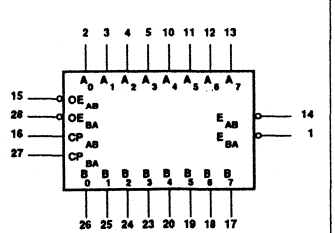
PACKAGES	TEMPERATURE RANGE	ORDER CODE
28-pin plastic DIP (300mil-wide)	-40°C to +85°C	74AC11470N 74ACT11470N
28-pin plastic SO (300mil-wide)	-40°C to +85°C	74AC11470D 74ACT11470D

PIN CONFIGURATION

N and D Packages



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)

In progress

PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
16	CP_{AB}	A-to-B clock input (active Low)
27	CP_{BA}	B-to-A clock input (active Low)
15	$\overline{OE}_{AB}$	A-to-B output enable input (active Low)
28	$\overline{OE}_{BA}$	B-to-A output enable input (active Low)
14	$\overline{E}_{AB}$	A-to-B enable input (active Low)
1	$\overline{E}_{BA}$	B-to-A enable input (active Low)
2, 3, 4, 5, 10, 11, 12, 13	$A_0 - A_7$	Data inputs/outputs (A side)
26, 25, 24, 23, 20, 19, 18, 17	$B_0 - B_7$	Data inputs/outputs (B side)
6, 7, 8, 9	GND	Ground (0V)
21, 22	V_{CC}	Positive supply voltage

FUNCTION TABLE

INPUTS				OUTPUTS	STATUS
$\overline{OE}_{XX}$	$\overline{E}_{XX}$	CP_{XX}	Data		
H	X	X	X	Z	Outputs disabled
X	H	X	X	Z	Outputs and clock disabled
L	L	↑	l h	L H	Load register
X	↑	L	l h	Z	Load register and disable outputs

H = High voltage level
h = High state present one setup time before the Low-to-High transition
L = Low voltage level
= Low state present one setup time before the Low-to-High transition
↑ = Low-to-High transition
X = Don't care
Z = High-impedance state

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	74AC11470			74ACT11470			UNIT
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	DC supply voltage	3.0[1]	5.0	5.5	4.5	5.0	5.5	V
V_I	Input voltage	0		V_{CC}	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	0		V_{CC}	V
$\Delta t/\Delta v$	Input transition rise or fall rate	0		10	0		10	ns/V
T_A	Operating free-air temperature	-40		+85	-40		+85	°C

NOTE:
1. No electrical or switching characteristics are specified at V_{CC} < 3V. Operation between 2V and 3V is not recommended, but within that range, a device output will maintain a previously established logic state.

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	TEST CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 to+7.0	V
I_{IK} or V_I	DC input diode current[2]	$V_I < 0$	-20	mA
		$V_I > V_{CC}$	20	
	DC input voltage		-0.5 to V_{CC} +0.5	V
I_{OK} or V_O	DC output diode current[2]	$V_O < 0$	-50	mA
		$V_O > V_{CC}$	50	
	DC output voltage		-0.5 to V_{CC} +0.5	V
I_O	DC output source or sink current per output pin	V_O = 0 to V_{CC}	±50	mA
I_{CC} or I_{GND}	DC V_{CC} current		±200	mA
	DC ground current		±200	
T_{STG}	Storage temperature		-65 to 150	°C
P_{TOT}	Power dissipation per package Plastic DIP	Above 70°C:derate linearly by 8mW/K	500	mW
	Power dissipation per package Plastic surface mount (SO)	Above 70°C:derate linearly by 6mW/K	400	mW

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		V_{CC}	74AC11470				74ACT11470				UNIT
					T_A = +25°C		T_A = -40°C to +85°C		T_A = +25°C		T_A = -40°C to +85°C		
				V	Min	Max	Min	Max	Min	Max	Min	Max	
V_{IH}	High-level input voltage			3.0	2.10		2.10						V
				4.5	3.15		3.15		2.0		2.0		
				5.5	3.85		3.85		2.0		2.0		
V_{IL}	Low-level input voltage			3.0		0.90		0.90					V
				4.5		1.35		1.35		0.8		0.8	
				5.5		1.65		1.65		0.8		0.8	
V_{OH}	High-level output voltage	V_I = V_{IL} or V_{IH}	I_{OH} = -50μA	3.0	2.9		2.9						V
				4.5	4.4		4.4		4.4		4.4		
				5.5	5.4		5.4		5.4		5.4		
			I_{OH} = -4mA	3.0	2.58		2.48						
			I_{OH} = -24mA	4.5	3.94		3.8		3.94		3.8		
				5.5	4.94		4.8		4.94		4.8		
			I_{OH} = -75mA[1]	5.5			3.85				3.85		
V_{OL}	Low-level output voltage	V_I = V_{IL} or V_{IH}	I_{OL} = 50μA	3.0		0.1		0.1					V
				4.5		0.1		0.1		0.1		0.1	
				5.5		0.1		0.1		0.1		0.1	
			I_{OL} = 12mA	3.0		0.36		0.44					
			I_{OL} = 24mA	4.5		0.36		0.44		0.36		0.44	
				5.5		0.36		0.44		0.36		0.44	
			I_{OL} = 75mA[1]	5.5				1.65				1.65	
I_I	Input leakage current	V_I = V_{CC} or GND		5.5		±0.1		±1.0		±0.1		±1.0	μA
I_{OZ}	3-State output off-state current	V_I = V_{IL} or V_{IH}, V_O = V_{CC} or GND		5.5		±0.5		±5.0		±0.5		±5.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC} or GND, I_O = 0		5.5		8.0		80		8.0		80	μA
ΔI_{CC}	Supply current, TTL inputs High[2]	One input at 3.4V, other inputs at V_{CC} or GND		5.5						0.9		1.0	mA

NOTES:
1. Not more than one output should be tested at a time, and the duration of the test should not exceed 10ms.
2. This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0V or V_{CC}.

74AC/ACT11471

Octal Transceiver/Register with Dual Enable; 3-State; INV

Objective Specification

FEATURES

- **Combines '245 and '374 type functions in one chip**
- **8-bit octal transceiver with D-type flip-flops**
- **3-State buffers**
- **Output capability: ±24 mA**
- **CMOS (AC) and TTL (ACT) voltage level inputs**
- **50Ω incident wave switching**
- **Center-pin V_{CC} and ground configuration to minimize high-speed switching noise**
- **I_{CC} category: MSI**

DESCRIPTION

The 74AC/ACT11471 high-performance CMOS devices combine very high speed and high output drive comparable to the most advanced TTL families.

The 74AC/ACT11471 Octal Transceiver/Register contains two sets of D-type flip-flops for temporary storage of data flowing in either direction. Dual Enable ($\overline{E}_{AB}$, $\overline{E}_{BA}$) and Output Enable ($\overline{OE}_{AB}$, $\overline{OE}_{BA}$) inputs are provided for each register to permit independent control of inputting and outputting in either direction of data flow.

GENERAL INFORMATION

SYMBOL	PARAMETER	CONDITIONS T_A = 25°C; GND = 0V; V_{CC} = 5.0V		TYPICAL AC	TYPICAL ACT	UNIT
t_{PLH}/t_{PHL}	Propagation delay CP_{XX} to $\overline{A}_n$ or $\overline{B}_n$	C_L = 50pF		5.2	6.7	ns
C_{PD}	Power dissipation capacitance per register[1]	f = 1MHz; C_L = 50pF	Enabled	155	160	pF
			Disabled	35	40	
C_{IN}	Input capacitance	V_I = 0V or V_{CC}		4.5	4.5	pF
$C_{I/O}$	I/O capacitance	$V_{I/O}$ = 0V or V_{CC}; Disabled		12.0	12.0	pF
I_{LATCH}	Latch-up current	Per Jedec JC40.2 Standard 17		500	500	mA
f_{MAX}	Maximum clock frequency	C_L = 50pF		125	125	MHz

Note:

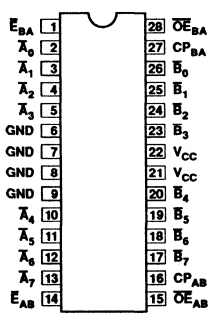
1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_I + \Sigma (C_L \times V_{CC}^2 \times f_O)$ where:
   f_I = input frequency in MHz, C_L = output load capacitance in pF,
   f_O = output frequency in MHz, V_{CC} = supply voltage in V,
   $\Sigma (C_L \times V_{CC}^2 \times f_O)$ = sum of outputs

ORDERING INFORMATION

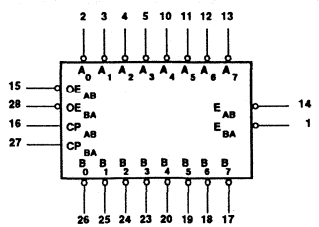
PACKAGES	TEMPERATURE RANGE	ORDER CODE
28-pin plastic DIP (300mil-wide)	-40°C to +85°C	74AC11471N 74ACT11471N
28-pin plastic SO (300mil-wide)	-40°C to +85°C	74AC11471D 74ACT11471D

PIN CONFIGURATION

N and D Packages



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)

In progress

PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
16	CP_{AB}	A-to-B clock input (active Low)
27	CP_{BA}	B-to-A clock input (active Low)
15	$\overline{OE}_{AB}$	A-to-B output enable input (active Low)
28	$\overline{OE}_{BA}$	B-to-A output enable input (active Low)
14	$\overline{E}_{AB}$	A-to-B enable input (active Low)
1	$\overline{E}_{BA}$	B-to-A enable input (active Low)
2, 3, 4, 5, 10, 11, 12, 13	$\overline{A}_0$ - $\overline{A}_7$	Data inputs/outputs (A side)
26, 25, 24, 23, 20, 19, 18, 17	$\overline{B}_0$ - $\overline{B}_7$	Data inputs/outputs (B side)
6, 7, 8, 9	GND	Ground (0V)
21, 22	V_{CC}	Positive supply voltage

FUNCTION TABLE

INPUTS				OUTPUTS	STATUS
$\overline{OE}_{XX}$	$\overline{E}_{XX}$	CP_{XX}	Data		
H	X	X	X	Z	Outputs disabled
X	H	X	X	Z	Outputs and clock disabled
L	L	↑	l h	H L	Load register
X	↑	L	l h	Z	Load register and disable outputs

H = High voltage level
h = High state present one setup time before the Low-to-High transition
L = Low voltage level
l = Low state present one setup time before the Low-to-High transition
↑ = Low-to-High transition
X = Don't care
Z = High-impedance state

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	74AC11471			74ACT11471			UNIT
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	DC supply voltage	3.0[1]	5.0	5.5	4.5	5.0	5.5	V
V_I	Input voltage	0		V_{CC}	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	0		V_{CC}	V
$\Delta t/\Delta v$	Input transition rise or fall rate	0		10	0		10	ns/V
T_A	Operating free-air temperature	-40		+85	-40		+85	°C

NOTE:
1. No electrical or switching characteristics are specified at V_{CC} < 3V. Operation between 2V and 3V is not recommended, but within that range, a device output will maintain a previously established logic state.

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	TEST CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 to+7.0	V
I_{IK} or V_I	DC input diode current[2]	$V_I < 0$	-20	mA
		$V_I > V_{CC}$	20	
	DC input voltage		-0.5 to V_{CC} +0.5	V
I_{OK} or V_O	DC output diode current[2]	$V_O < 0$	-50	mA
		$V_O > V_{CC}$	50	
	DC output voltage		-0.5 to V_{CC} +0.5	V
I_O	DC output source or sink current per output pin	V_O = 0 to V_{CC}	±50	mA
I_{CC} or I_{GND}	DC V_{CC} current		±200	mA
	DC ground current		±200	
T_{STG}	Storage temperature		-65 to 150	°C
P_{TOT}	Power dissipation per package Plastic DIP	Above 70°C:derate linearly by 8mW/K	500	mW
	Power dissipation per package Plastic surface mount (SO)	Above 70°C:derate linearly by 6mW/K	400	mW

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		V_{CC}	74AC11471				74ACT11471				UNIT
					T_A = +25°C		T_A = -40°C to +85°C		T_A = +25°C		T_A = -40°C to +85°C		
				V	Min	Max	Min	Max	Min	Max	Min	Max	
V_{IH}	High-level input voltage			3.0	2.10		2.10						V
				4.5	3.15		3.15		2.0		2.0		
				5.5	3.85		3.85		2.0		2.0		
V_{IL}	Low-level input voltage			3.0		0.90		0.90					V
				4.5		1.35		1.35		0.8		0.8	
				5.5		1.65		1.65		0.8		0.8	
V_{OH}	High-level output voltage	V_I = V_{IL} or V_{IH}	I_{OH} = -50μA	3.0	2.9		2.9						V
				4.5	4.4		4.4		4.4		4.4		
				5.5	5.4		5.4		5.4		5.4		
			I_{OH} = -4mA	3.0	2.58		2.48						
			I_{OH} = -24mA	4.5	3.94		3.8		3.94		3.8		
				5.5	4.94		4.8		4.94		4.8		
			I_{OH} = -75mA[1]	5.5			3.85				3.85		
V_{OL}	Low-level output voltage	V_I = V_{IL} or V_{IH}	I_{OL} = 50μA	3.0		0.1		0.1					V
				4.5		0.1		0.1		0.1		0.1	
				5.5		0.1		0.1		0.1		0.1	
			I_{OL} = 12mA	3.0		0.36		0.44					
			I_{OL} = 24mA	4.5		0.36		0.44		0.36		0.44	
				5.5		0.36		0.44		0.36		0.44	
			I_{OL} = 75mA[1]	5.5				1.65				1.65	
I_I	Input leakage current	V_I = V_{CC} or GND		5.5		±0.1		±1.0		±0.1		±1.0	μA
I_{OZ}	3-State output off-state current	V_I = V_{IL} or V_{IH}, V_O = V_{CC} or GND		5.5		±0.5		±5.0		±0.5		±5.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC} or GND, I_O = 0		5.5		8.0		80		8.0		80	μA
ΔI_{CC}	Supply current, TTL inputs High[2]	One input at 3.4V, other inputs at V_{CC} or GND		5.5						0.9		1.0	mA

NOTES:
1. Not more than one output should be tested at a time, and the duration of the test should not exceed 10ms.
2. This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0V or V_{CC}.

74AC/ACT11472

9-Wide Transceiver with Dual Enable; 3-State

Objective Specification

FEATURES

- **3-State buffers**
- **Output capability: ±24 mA**
- **CMOS (AC) and TTL (ACT) voltage level inputs**
- **50Ω incident wave switching**
- **Center-pin V_{CC} and ground configuration to minimize high-speed switching noise**
- **I_{CC} category: MSI**

DESCRIPTION

The 74AC/ACT11472 high-performance CMOS devices combine very high speed and high output drive comparable to the most advanced TTL families.

The 74AC/ACT11472 device contains two sets of latches for temporary storage of data flowing in either direction. Dual Latch Enable ($\overline{LE}_{AB}$, $\overline{LE}_{BA}$) and Output Enable ($\overline{OE}_{AB}$, $\overline{OE}_{BA}$) inputs are provided for each set of latches to permit independent control of inputting and outputting in either direction of data flow.

GENERAL INFORMATION

SYMBOL	PARAMETER	CONDITIONS T_A = 25°C; GND = 0V; V_{CC} = 5.0V		TYPICAL AC	TYPICAL ACT	UNIT
t_{PLH}/t_{PHL}	Propagation delay $\overline{LE}_{XX}$ to A_n or B_n	C_L = 50pF		5.2	6.7	ns
C_{PD}	Power dissipation capacitance per register[1]	f = 1MHz;	Enabled	200	200	pF
		C_L = 50pF	Disabled	50	50	pF
C_{IN}	Input capacitance	V_I = 0V or V_{CC}		4.5	4.5	pF
$C_{I/O}$	I/O capacitance	$V_{I/O}$ = 0V or V_{CC}; Disabled		12	12	pF
I_{LATCH}	Latch-up current	Per Jedec JC40.2 Standard 17		500	500	mA

Note:

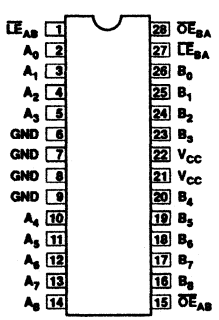
1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_I + \Sigma (C_L \times V_{CC}^2 \times f_O)$ where:
   f_I = input frequency in MHz, C_L = output load capacitance in pF,
   f_O = output frequency in MHz, V_{CC} = supply voltage in V,
   $\Sigma (C_L \times V_{CC}^2 \times f_O)$ = sum of outputs

ORDERING INFORMATION

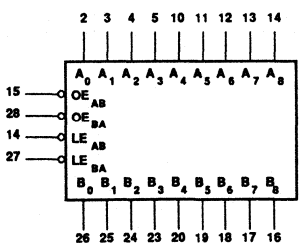
PACKAGES	TEMPERATURE RANGE	ORDER CODE
28-pin plastic DIP (300mil-wide)	-40°C to +85°C	74AC11472N 74ACT11472N
28-pin plastic SO (300mil-wide)	-40°C to +85°C	74AC11472D 74ACT11472D

PIN CONFIGURATION

N and D Packages



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)

In progress

PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
1	$\overline{LE}_{AB}$	A-to-B latch enable (active Low)
27	$\overline{LE}_{BA}$	B-to-A latch enable (active Low)
15	$\overline{OE}_{AB}$	A-to-B output enable input (active Low)
28	$\overline{OE}_{BA}$	B-to-A output enable input (active Low)
2, 3, 4, 5, 10, 11, 12, 13, 14	A_0 - A_8	Data inputs/outputs (A side)
26, 25, 24, 23, 20, 19, 18, 17, 16	B_0 - B_8	Data inputs/outputs (B side)
6, 7, 8, 9	GND	Ground (0V)
21, 22	V_{CC}	Positive supply voltage

FUNCTION TABLE

INPUTS			OUTPUTS	STATUS
$\overline{OE}_{XX}$	$\overline{LE}_{XX}$	Data		
H	X	X	Z	Latch register and disable outputs
L	L	l h	L H	Enable and read register
L	H	X X	L H	Latch and read register

H = High voltage level
h = High state present one setup time before the Low-to-High transition
L = Low voltage level
= Low state present one setup time before the Low-to-High transition
X = Don't care
Z = High-impedance state

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	74AC11472			74ACT11472			UNIT
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	DC supply voltage	3.0[1]	5.0	5.5	4.5	5.0	5.5	V
V_I	Input voltage	0		V_{CC}	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	0		V_{CC}	V
$\Delta t/\Delta v$	Input transition rise or fall rate	0		10	0		10	ns/V
T_A	Operating free-air temperature	-40		+85	-40		+85	°C

NOTE:
1. No electrical or switching characteristics are specified at V_{CC} < 3V. Operation between 2V and 3V is not recommended, but within that range, a device output will maintain a previously established logic state.

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	TEST CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 to+7.0	V
I_{IK} or V_I	DC input diode current[2]	$V_I < 0$	-20	mA
		$V_I > V_{CC}$	20	
	DC input voltage		-0.5 to V_{CC} +0.5	V
I_{OK} or V_O	DC output diode current[2]	$V_O < 0$	-50	mA
		$V_O > V_{CC}$	50	
	DC output voltage		-0.5 to V_{CC} +0.5	V
I_O	DC output source or sink current per output pin	V_O = 0 to V_{CC}	±50	mA
I_{CC} or I_{GND}	DC V_{CC} current		±225	mA
	DC ground current		±225	
T_{STG}	Storage temperature		-65 to 150	°C
P_{TOT}	Power dissipation per package Plastic DIP	Above 70°C:derate linearly by 8mW/K	500	mW
	Power dissipation per package Plastic surface mount (SO)	Above 70°C:derate linearly by 6mW/K	400	mW

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		V_{CC}	74AC11472				74ACT11472				UNIT
					T_A = +25°C		T_A = -40°C to +85°C		T_A = +25°C		T_A = -40°C to +85°C		
				V	Min	Max	Min	Max	Min	Max	Min	Max	
V_{IH}	High-level input voltage			3.0	2.10		2.10						V
				4.5	3.15		3.15		2.0		2.0		
				5.5	3.85		3.85		2.0		2.0		
V_{IL}	Low-level input voltage			3.0		0.90		0.90					V
				4.5		1.35		1.35		0.8		0.8	
				5.5		1.65		1.65		0.8		0.8	
V_{OH}	High-level output voltage	V_I = V_{IL} or V_{IH}	I_{OH} = -50μA	3.0	2.9		2.9						V
				4.5	4.4		4.4		4.4		4.4		
				5.5	5.4		5.4		5.4		5.4		
			I_{OH} = -4mA	3.0	2.58		2.48						
			I_{OH} = -24mA	4.5	3.94		3.8		3.94		3.8		
				5.5	4.94		4.8		4.94		4.8		
			I_{OH} = -75mA[1]	5.5			3.85				3.85		
V_{OL}	Low-level output voltage	V_I = V_{IL} or V_{IH}	I_{OL} = 50μA	3.0		0.1		0.1					V
				4.5		0.1		0.1		0.1		0.1	
				5.5		0.1		0.1		0.1		0.1	
			I_{OL} = 12mA	3.0		0.36		0.44					
			I_{OL} = 24mA	4.5		0.36		0.44		0.36		0.44	
				5.5		0.36		0.44		0.36		0.44	
			I_{OL} = 75mA[1]	5.5				1.65				1.65	
I_I	Input leakage current	V_I = V_{CC} or GND		5.5		±0.1		±1.0		±0.1		±1.0	μA
I_{OZ}	3-State output off-state current	V_I = V_{IL} or V_{IH}, V_O = V_{CC} or GND		5.5		±0.5		±5.0		±0.5		±5.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC} or GND, I_O = 0		5.5		8.0		80		8.0		80	μA
ΔI_{CC}	Supply current, TTL inputs High[2]	One input at 3.4V, other inputs at V_{CC} or GND		5.5						0.9		1.0	mA

NOTES:
1. Not more than one output should be tested at a time, and the duration of the test should not exceed 10ms.
2. This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0V or V_{CC}.

74AC/ACT11473

9-Wide Transceiver with Dual Enable; 3-State; INV

Objective Specification

FEATURES

- **3-State buffers**
- **Output capability: ±24 mA**
- **CMOS (AC) and TTL (ACT) voltage level inputs**
- **50Ω incident wave switching**
- **Center-pin V_{CC} and ground configuration to minimize high-speed switching noise**
- **I_{CC} category: MSI**

DESCRIPTION

The 74AC/ACT11473 high-performance CMOS devices combine very high speed and high output drive comparable to the most advanced TTL families.

The 74AC/ACT11473 device contains two sets of latches for temporary storage of data flowing in either direction. Dual Latch Enable ($\overline{LE}_{AB}$, $\overline{LE}_{BA}$) and Output Enable ($\overline{OE}_{AB}$, $\overline{OE}_{BA}$) inputs are provided for each set of latches to permit independent control of inputting and outputting in either direction of data flow.

GENERAL INFORMATION

SYMBOL	PARAMETER	CONDITIONS T_A = 25°C; GND = 0V; V_{CC} = 5.0V		TYPICAL AC	TYPICAL ACT	UNIT
t_{PLH}/ t_{PHL}	Propagation delay $\overline{LE}_{XX}$ to $\overline{A}_n$ or $\overline{B}_n$	C_L = 50pF		5.2	6.7	ns
C_{PD}	Power dissipation capacitance per register[1]	f = 1MHz; C_L = 50pF	Enabled	200	200	pF
			Disabled	50	50	
C_{IN}	Input capacitance	V_I = 0V or V_{CC}		4.5	4.5	pF
$C_{I/O}$	I/O capacitance	$V_{I/O}$ = 0V or V_{CC}; Disabled		12	12	pF
I_{LATCH}	Latch-up current	Per Jedec JC40.2 Standard 17		500	500	mA

Note:

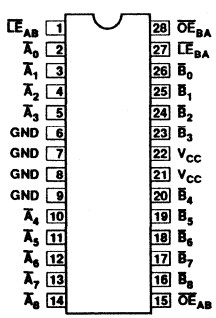
1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_I + \Sigma (C_L \times V_{CC}^2 \times f_O)$ where:
   f_I = input frequency in MHz, C_L = output load capacitance in pF,
   f_O = output frequency in MHz, V_{CC} = supply voltage in V,
   $\Sigma (C_L \times V_{CC}^2 \times f_O)$ = sum of outputs

ORDERING INFORMATION

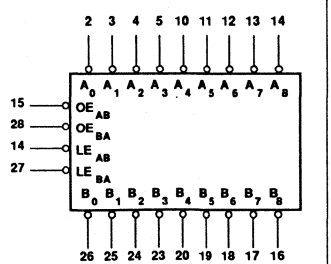
PACKAGES	TEMPERATURE RANGE	ORDER CODE
28-pin plastic DIP (300mil-wide)	-40°C to +85°C	74AC11473N 74ACT11473N
28-pin plastic SO (300mil-wide)	-40°C to +85°C	74AC11473D 74ACT11473D

PIN CONFIGURATION

N and D Packages



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)

In progress

PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
1	$\overline{LE}_{AB}$	A-to-B latch enable (active Low)
27	$\overline{LE}_{BA}$	B-to-A latch enable (active Low)
15	$\overline{OE}_{AB}$	A-to-B output enable input (active Low)
28	$\overline{OE}_{BA}$	B-to-A output enable input (active Low)
2, 3, 4, 5, 10, 11, 12, 13, 14	$\overline{A}_0$ - $\overline{A}_8$	Data inputs/outputs (A side)
26, 25, 24, 23, 20, 19, 18, 17, 16	$\overline{B}_0$ - $\overline{B}_8$	Data inputs/outputs (B side)
6, 7, 8, 9	GND	Ground (0V)
21, 22	V_{CC}	Positive supply voltage

FUNCTION TABLE

INPUTS			OUTPUTS	STATUS
$\overline{OE}_{XX}$	$\overline{LE}_{XX}$	Data		
H	X	X	Z	Latch register and disable outputs
L	L	l h	H L	Enable and read register
L	H	X X	H L	Latch and read register

H = High voltage level
h = High state present one setup time before the Low-to-High transition
L = Low voltage level
= Low state present one setup time before the Low-to-High transition
X = Don't care
Z = High-impedance state

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	74AC11473			74ACT11473			UNIT
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	DC supply voltage	3.0[1]	5.0	5.5	4.5	5.0	5.5	V
V_I	Input voltage	0		V_{CC}	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	0		V_{CC}	V
$\Delta t/\Delta v$	Input transition rise or fall rate	0		10	0		10	ns/V
T_A	Operating free-air temperature	-40		+85	-40		+85	°C

NOTE:

1. No electrical or switching characteristics are specified at V_{CC} < 3V. Operation between 2V and 3V is not recommended, but within that range, a device output will maintain a previously established logic state.

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	TEST CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 to+7.0	V
I_{IK} or V_I	DC input diode current[2]	$V_I < 0$	-20	mA
		$V_I > V_{CC}$	20	
	DC input voltage		-0.5 to V_{CC} +0.5	V
I_{OK} or V_O	DC output diode current[2]	$V_O < 0$	-50	mA
		$V_O > V_{CC}$	50	
	DC output voltage		-0.5 to V_{CC} +0.5	V
I_O	DC output source or sink current per output pin	V_O = 0 to V_{CC}	±50	mA
I_{CC} or I_{GND}	DC V_{CC} current		±225	mA
	DC ground current		±225	
T_{STG}	Storage temperature		-65 to 150	°C
P_{TOT}	Power dissipation per package Plastic DIP	Above 70°C:derate linearly by 8mW/K	500	mW
	Power dissipation per package Plastic surface mount (SO)	Above 70°C:derate linearly by 6mW/K	400	mW

NOTES:

1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		V_{CC}	74AC11473				74ACT11473				UNIT
					T_A = +25°C		T_A = -40°C to +85°C		T_A = +25°C		T_A = -40°C to +85°C		
				V	Min	Max	Min	Max	Min	Max	Min	Max	
V_{IH}	High-level input voltage			3.0	2.10		2.10						V
				4.5	3.15		3.15		2.0		2.0		
				5.5	3.85		3.85		2.0		2.0		
V_{IL}	Low-level input voltage			3.0		0.90		0.90					V
				4.5		1.35		1.35		0.8		0.8	
				5.5		1.65		1.65		0.8		0.8	
V_{OH}	High-level output voltage	V_I = V_{IL} or V_{IH}	I_{OH} = -50μA	3.0	2.9		2.9						V
				4.5	4.4		4.4		4.4		4.4		
				5.5	5.4		5.4		5.4		5.4		
			I_{OH} = -4mA	3.0	2.58		2.48						
			I_{OH} = -24mA	4.5	3.94		3.8		3.94		3.8		
				5.5	4.94		4.8		4.94		4.8		
			I_{OH} = -75mA[1]	5.5			3.85				3.85		
V_{OL}	Low-level output voltage	V_I = V_{IL} or V_{IH}	I_{OL} = 50μA	3.0		0.1		0.1					V
				4.5		0.1		0.1		0.1		0.1	
				5.5		0.1		0.1		0.1		0.1	
			I_{OL} = 12mA	3.0		0.36		0.44					
			I_{OL} = 24mA	4.5		0.36		0.44		0.36		0.44	
				5.5		0.36		0.44		0.36		0.44	
			I_{OL} = 75mA[1]	5.5				1.65				1.65	
I_I	Input leakage current	V_I = V_{CC} or GND		5.5		±0.1		±1.0		±0.1		±1.0	μA
I_{OZ}	3-State output off-state current	V_I = V_{IL} or V_{IH}, V_O = V_{CC} or GND		5.5		±0.5		±5.0		±0.5		±5.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC} or GND, I_O = 0		5.5		8.0		80		8.0		80	μA
ΔI_{CC}	Supply current, TTL inputs High[2]	One input at 3.4V, other inputs at V_{CC} or GND		5.5						0.9		1.0	mA

NOTES:
1. Not more than one output should be tested at a time, and the duration of the test should not exceed 10ms.
2. This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0V or V_{CC}.

74AC/ACT11474

9-Wide Transceiver/Register with Dual Enable; 3-State

Objective Specification

FEATURES

- **Combines '245 and '374 type functions in one chip**
- **9-wide transceiver with D-type flip-flops**
- **3-State buffers**
- **Output capability: ±24 mA**
- **CMOS (AC) and TTL (ACT) voltage level inputs**
- **50Ω incident wave switching**
- **Center-pin V_{CC} and ground configuration to minimize high-speed switching noise**
- **I_{CC} category: MSI**

DESCRIPTION

The 74AC/ACT11474 high-performance CMOS devices combine very high speed and high output drive comparable to the most advanced TTL families.

The 74AC/ACT11474 device contains two sets of D-type flip-flops for temporary storage of data flowing in either direction. Dual clock (CP_{AB}, CP_{BA}) and Output Enable ($\overline{OE}_{AB}$, $\overline{OE}_{BA}$) inputs are provided for each register to permit independent control of inputting and outputting in either direction of data flow.

GENERAL INFORMATION

SYMBOL	PARAMETER	CONDITIONS T_A = 25°C; GND = 0V; V_{CC} = 5.0V		TYPICAL AC	TYPICAL ACT	UNIT
t_{PLH}/t_{PHL}	Propagation delay CP_{XX} to A_n or B_n	C_L = 50pF		5.3	7.1	ns
C_{PD}	Power dissipation capacitance per register[1]	f = 1MHz; C_L = 50pF	Enabled	200	200	pF
			Disabled	50	50	
C_{IN}	Input capacitance	V_I = 0V or V_{CC}		4.5	4.5	pF
$C_{I/O}$	I/O capacitance	$V_{I/O}$ = 0V or V_{CC}; Disabled		12	12	pF
I_{LATCH}	Latch-up current	Per Jedec JC40.2 Standard 17		500	500	mA
f_{MAX}	Maximum clock frequency	C_L = 50pF		125	125	MHz

Note:

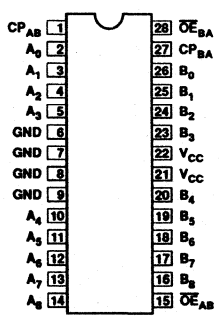
1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_I + \Sigma (C_L \times V_{CC}^2 \times f_O)$ where:
   f_I = input frequency in MHz, C_L = output load capacitance in pF,
   f_O = output frequency in MHz, V_{CC} = supply voltage in V,
   $\Sigma (C_L \times V_{CC}^2 \times f_O)$ = sum of outputs

ORDERING INFORMATION

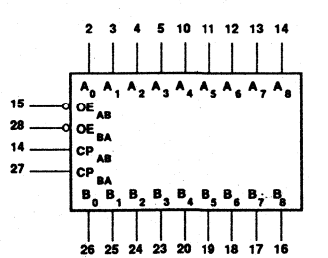
PACKAGES	TEMPERATURE RANGE	ORDER CODE
28-pin plastic DIP (300mil-wide)	-40°C to +85°C	74AC11474N 74ACT11474N
28-pin plastic SO (300mil-wide)	-40°C to +85°C	74AC11474D 74ACT11474D

PIN CONFIGURATION

N and D Packages



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)

In progress

PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
1	CP_{AB}	A-to-B clock
27	CP_{BA}	B-to-A clock
15	$\overline{OE}_{AB}$	A-to-B output enable input (active Low)
28	$\overline{OE}_{BA}$	B-to-A output enable input (active Low)
2, 3, 4, 5, 10, 11, 12, 13, 14	$A_0 - A_8$	Data inputs/outputs (A side)
26, 25, 24, 23, 20, 19, 18, 17, 16	$B_0 - B_8$	Data inputs/outputs (B side)
6, 7, 8, 9	GND	Ground (0V)
21, 22	V_{CC}	Positive supply voltage

FUNCTION TABLE

INPUTS			OUTPUTS	STATUS
$\overline{OE}_{XX}$	CP_{XX}	Data		
H	X	X	Z	Latch register and disable outputs
L	↑	l h	L H	Enable and read register

H = High voltage level
h = High state present one setup time before the Low-to-High transition
L = Low voltage level
= Low state present one setup time before the Low-to-High transition
↑ = Low-to-High clock transition
X = Don't care
Z = High-impedance state

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	74AC11474			74ACT11474			UNIT
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	DC supply voltage	3.0[1]	5.0	5.5	4.5	5.0	5.5	V
V_I	Input voltage	0		V_{CC}	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	0		V_{CC}	V
$\Delta t/\Delta v$	Input transition rise or fall rate	0		10	0		10	ns/V
T_A	Operating free-air temperature	-40		+85	-40		+85	°C

NOTE:

1. No electrical or switching characteristics are specified at V_{CC} < 3V. Operation between 2V and 3V is not recommended, but within that range, a device output will maintain a previously established logic state.

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	TEST CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 to+7.0	V
I_{IK} or V_I	DC input diode current[2]	$V_I < 0$	-20	mA
		$V_I > V_{CC}$	20	
	DC input voltage		-0.5 to V_{CC} +0.5	V
I_{OK} or V_O	DC output diode current[2]	$V_O < 0$	-50	mA
		$V_O > V_{CC}$	50	
	DC output voltage		-0.5 to V_{CC} +0.5	V
I_O	DC output source or sink current per output pin	V_O = 0 to V_{CC}	±50	mA
I_{CC} or I_{GND}	DC V_{CC} current		±225	mA
	DC ground current		±225	
T_{STG}	Storage temperature		-65 to 150	°C
P_{TOT}	Power dissipation per package Plastic DIP	Above 70°C:derate linearly by 8mW/K	500	mW
	Power dissipation per package Plastic surface mount (SO)	Above 70°C:derate linearly by 6mW/K	400	mW

NOTES:

1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		V_{CC}	74AC11474				74ACT11474				UNIT
					T_A = +25°C		T_A = -40°C to +85°C		T_A = +25°C		T_A = -40°C to +85°C		
				V	Min	Max	Min	Max	Min	Max	Min	Max	
V_{IH}	High-level input voltage			3.0	2.10		2.10						V
				4.5	3.15		3.15		2.0		2.0		
				5.5	3.85		3.85		2.0		2.0		
V_{IL}	Low-level input voltage			3.0		0.90		0.90					V
				4.5		1.35		1.35		0.8		0.8	
				5.5		1.65		1.65		0.8		0.8	
V_{OH}	High-level output voltage	V_I = V_{IL} or V_{IH}	I_{OH} = -50μA	3.0	2.9		2.9						V
				4.5	4.4		4.4		4.4		4.4		
				5.5	5.4		5.4		5.4		5.4		
			I_{OH} = -4mA	3.0	2.58		2.48						
			I_{OH} = -24mA	4.5	3.94		3.8		3.94		3.8		
				5.5	4.94		4.8		4.94		4.8		
			I_{OH} = -75mA[1]	5.5			3.85				3.85		
V_{OL}	Low-level output voltage	V_I = V_{IL} or V_{IH}	I_{OL} = 50μA	3.0		0.1		0.1					V
				4.5		0.1		0.1		0.1		0.1	
				5.5		0.1		0.1		0.1		0.1	
			I_{OL} = 12mA	3.0		0.36		0.44					
			I_{OL} = 24mA	4.5		0.36		0.44		0.36		0.44	
				5.5		0.36		0.44		0.36		0.44	
			I_{OL} = 75mA[1]	5.5				1.65				1.65	
I_I	Input leakage current	V_I = V_{CC} or GND		5.5		±0.1		±1.0		±0.1		±1.0	μA
I_{OZ}	3-State output off-state current	V_I = V_{IL} or V_{IH}, V_O = V_{CC} or GND		5.5		±0.5		±5.0		±0.5		±5.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC} or GND, I_O = 0		5.5		8.0		80		8.0		80	μA
ΔI_{CC}	Supply current, TTL inputs High[2]	One input at 3.4V, other inputs at V_{CC} or GND		5.5						0.9		1.0	mA

NOTES:
1. Not more than one output should be tested at a time, and the duration of the test should not exceed 10ms.
2. This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0V or V_{CC}.

74AC/ACT11475

9-Wide Transceiver/Register with Dual Enable; 3-State; INV

Objective Specification

FEATURES

- **Combines '245 and '374 type functions in one chip**
- **9-wide transceiver with D-type flip-flops**
- **3-State buffers**
- **Output capability: ±24 mA**
- **CMOS (AC) and TTL (ACT) voltage level inputs**
- **50Ω incident wave switching**
- **Center-pin V_{CC} and ground configuration to minimize high-speed switching noise**
- **I_{CC} category: MSI**

DESCRIPTION

The 74AC/ACT11475 high-performance CMOS devices combine very high speed and high output drive comparable to the most advanced TTL families.

The 74AC/ACT11475 device contains two sets of D-type flip-flops for temporary storage of data flowing in either direction. Dual clock (CP_{AB}, CP_{BA}) and Output Enable ($\overline{OE}_{AB}$, $\overline{OE}_{BA}$) inputs are provided for each register to permit independent control of inputting and outputting in either direction of data flow.

GENERAL INFORMATION

SYMBOL	PARAMETER	CONDITIONS T_A = 25°C; GND = 0V; V_{CC} = 5.0V		TYPICAL AC	TYPICAL ACT	UNIT
t_{PLH}/t_{PHL}	Propagation delay CP_{XX} to $\overline{A}_n$ or $\overline{B}_n$	C_L = 50pF		5.3	7.1	ns
C_{PD}	Power dissipation capacitance per register[1]	f = 1MHz; C_L = 50pF	Enabled	200	200	pF
			Disabled	50	50	
C_{IN}	Input capacitance	V_I = 0V or V_{CC}		4.5	4.5	pF
$C_{I/O}$	I/O capacitance	$V_{I/O}$ = 0V or V_{CC}; Disabled		12	12	pF
I_{LATCH}	Latch-up current	Per Jedec JC40.2 Standard 17		500	500	mA
f_{MAX}	Maximum clock frequency	C_L = 50pF		125	125	MHz

Note:

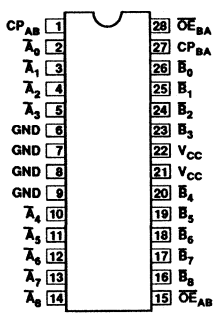
1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_I + \Sigma (C_L \times V_{CC}^2 \times f_O)$ where:
   f_I = input frequency in MHz, C_L = output load capacitance in pF,
   f_O = output frequency in MHz, V_{CC} = supply voltage in V,
   $\Sigma (C_L \times V_{CC}^2 \times f_O)$ = sum of outputs

ORDERING INFORMATION

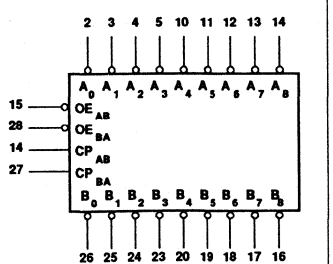
PACKAGES	TEMPERATURE RANGE	ORDER CODE
28-pin plastic DIP (300mil-wide)	-40°C to +85°C	74AC11475N 74ACT11475N
28-pin plastic SO (300mil-wide)	-40°C to +85°C	74AC11475D 74ACT11475D

PIN CONFIGURATION

N and D Packages



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)

In progress

9-Wide Transceiver/Register with Dual Enable; 3-State; INV

74AC/ACT11475

PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
1	CP_{AB}	A-to-B clock
27	CP_{BA}	B-to-A clock
15	$\overline{OE}_{AB}$	A-to-B output enable input (active Low)
28	$\overline{OE}_{BA}$	B-to-A output enable input (active Low)
2, 3, 4, 5, 10, 11, 12, 13, 14	$\overline{A}_0$ - $\overline{A}_8$	Data inputs/outputs (A side)
26, 25, 24, 23, 20, 19, 18, 17, 16	$\overline{B}_0$ - $\overline{B}_8$	Data inputs/outputs (B side)
6, 7, 8, 9	GND	Ground (0V)
21, 22	V_{CC}	Positive supply voltage

FUNCTION TABLE

INPUTS			OUTPUTS	STATUS
$\overline{OE}_{XX}$	CP_{XX}	Data		
H	X	X	Z	Latch register and disable outputs
L	↑	l h	H L	Enable and read register

H = High voltage level
h = High state present one setup time before the Low-to-High transition
L = Low voltage level
= Low state present one setup time before the Low-to-High transition
↑ = Low-to-High clock transition
X = Don't care
Z = High-impedance state

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	74AC11475			74ACT11475			UNIT
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	DC supply voltage	3.0[1]	5.0	5.5	4.5	5.0	5.5	V
V_I	Input voltage	0		V_{CC}	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	0		V_{CC}	V
$\Delta t/\Delta v$	Input transition rise or fall rate	0		10	0		10	ns/V
T_A	Operating free-air temperature	-40		+85	-40		+85	°C

NOTE:

1. No electrical or switching characteristics are specified at V_{CC} < 3V. Operation between 2V and 3V is not recommended, but within that range, a device output will maintain a previously established logic state.

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	TEST CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 to+7.0	V
I_{IK} or V_I	DC input diode current[2]	$V_I < 0$	-20	mA
		$V_I > V_{CC}$	20	
	DC input voltage		-0.5 to V_{CC} +0.5	V
I_{OK} or V_O	DC output diode current[2]	$V_O < 0$	-50	mA
		$V_O > V_{CC}$	50	
	DC output voltage		-0.5 to V_{CC} +0.5	V
I_O	DC output source or sink current per output pin	V_O = 0 to V_{CC}	±50	mA
I_{CC} or I_{GND}	DC V_{CC} current		±225	mA
	DC ground current		±225	
T_{STG}	Storage temperature		-65 to 150	°C
P_{TOT}	Power dissipation per package Plastic DIP	Above 70°C:derate linearly by 8mW/K	500	mW
	Power dissipation per package Plastic surface mount (SO)	Above 70°C:derate linearly by 6mW/K	400	mW

NOTES:

1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		V_{CC}	74AC11475				74ACT11475				UNIT
					T_A = +25°C		T_A = -40°C to +85°C		T_A = +25°C		T_A = -40°C to +85°C		
				V	Min	Max	Min	Max	Min	Max	Min	Max	
V_{IH}	High-level input voltage			3.0	2.10		2.10						V
				4.5	3.15		3.15		2.0		2.0		
				5.5	3.85		3.85		2.0		2.0		
V_{IL}	Low-level input voltage			3.0		0.90		0.90					V
				4.5		1.35		1.35		0.8		0.8	
				5.5		1.65		1.65		0.8		0.8	
V_{OH}	High-level output voltage	V_I = V_{IL} or V_{IH}	I_{OH} = -50μA	3.0	2.9		2.9						V
				4.5	4.4		4.4		4.4		4.4		
				5.5	5.4		5.4		5.4		5.4		
			I_{OH} = -4mA	3.0	2.58		2.48						
			I_{OH} = -24mA	4.5	3.94		3.8		3.94		3.8		
				5.5	4.94		4.8		4.94		4.8		
			I_{OH} = -75mA[1]	5.5			3.85				3.85		
V_{OL}	Low-level output voltage	V_I = V_{IL} or V_{IH}	I_{OL} = 50μA	3.0		0.1		0.1					V
				4.5		0.1		0.1		0.1		0.1	
				5.5		0.1		0.1		0.1		0.1	
			I_{OL} = 12mA	3.0		0.36		0.44					
			I_{OL} = 24mA	4.5		0.36		0.44		0.36		0.44	
				5.5		0.36		0.44		0.36		0.44	
			I_{OL} = 75mA[1]	5.5				1.65				1.65	
I_I	Input leakage current	V_I = V_{CC} or GND		5.5		±0.1		±1.0		±0.1		±1.0	μA
I_{OZ}	3-State output off-state current	V_I = V_{IL} or V_{IH}, V_O = V_{CC} or GND		5.5		±0.5		±5.0		±0.5		±5.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC} or GND, I_O = 0		5.5		8.0		80		8.0		80	μA
ΔI_{CC}	Supply current, TTL inputs High[2]	One input at 3.4V, other inputs at V_{CC} or GND		5.5						0.9		1.0	mA

NOTES:
1. Not more than one output should be tested at a time, and the duration of the test should not exceed 10ms.
2. This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0V or V_{CC}.

74AC/ACT11520

8-Bit Identity Comparator with Input Pull-Up

Product Specification

FEATURES

- **Compares two 8-bit words**
- **Output capability: ±24 mA**
- **CMOS (AC) and TTL (ACT) voltage level inputs**
- **50Ω incident wave switching**
- **Center-pin V_{CC} and ground configuration to minimize high-speed switching noise**
- **I_{CC} category: MSI**

DESCRIPTION

The 74AC/ACT11520 high-performance CMOS devices combine very high speed and high output drive comparable to the most advanced TTL families.

The 74AC/ACT11520 identity comparators perform comparisons on two 8-bit binary or BCD words and provides a Low output when the two words match bit for bit.

The 74AC/ACT11520 identity comparators also feature 20-k ohm pull-up termination resistors on the Q inputs for analog or switch data and a provision for $\overline{P=Q}$ totem-pole outputs.

GENERAL INFORMATION

SYMBOL	PARAMETER	CONDITIONS T_A = 25°C; GND = 0V; V_{CC} = 5.0V	TYPICAL		UNIT
			AC	ACT	
t_{PLH}/t_{PHL}	Propagation delay P_n or Q_n to $\overline{P=Q}$	C_L = 50pF	7.6	8.3	ns
C_{PD}	Power dissipation capacitance[1]	f = 1MHz; C_L = 50pF	42	40	pF
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	3.5	3.5	pF
I_{LATCH}	Latch-up current	Per Jedec JC40.2 Standard 17	500	500	mA

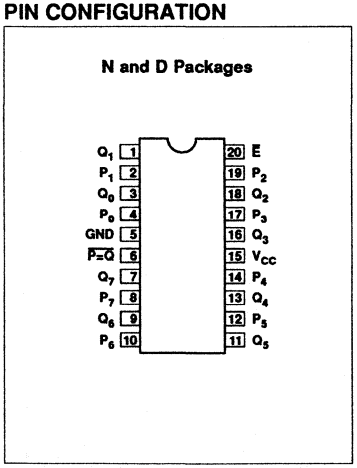
Note:

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_I + \Sigma (C_L \times V_{CC}^2 \times f_O)$ where:
   f_I = input frequency in MHz, C_L = output load capacitance in pF,
   f_O = output frequency in MHz, V_{CC} = supply voltage in V,
   $\Sigma (C_L \times V_{CC}^2 \times f_O)$ = sum of outputs

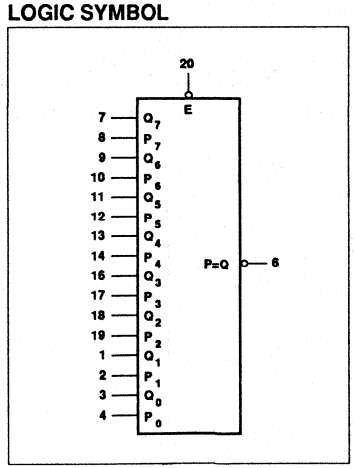
ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE
20-pin plastic DIP (300mil-wide)	-40°C to +85°C	74AC11520N 74ACT11520N
20-pin plastic SO (300mil-wide)	-40°C to +85°C	74AC11520D 74ACT11520D

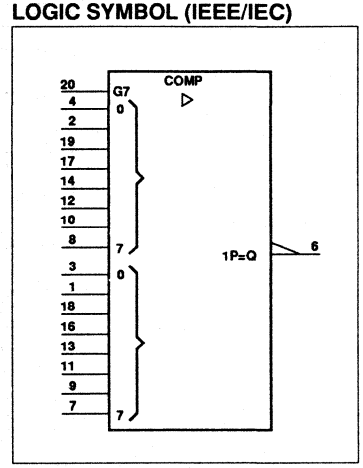
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



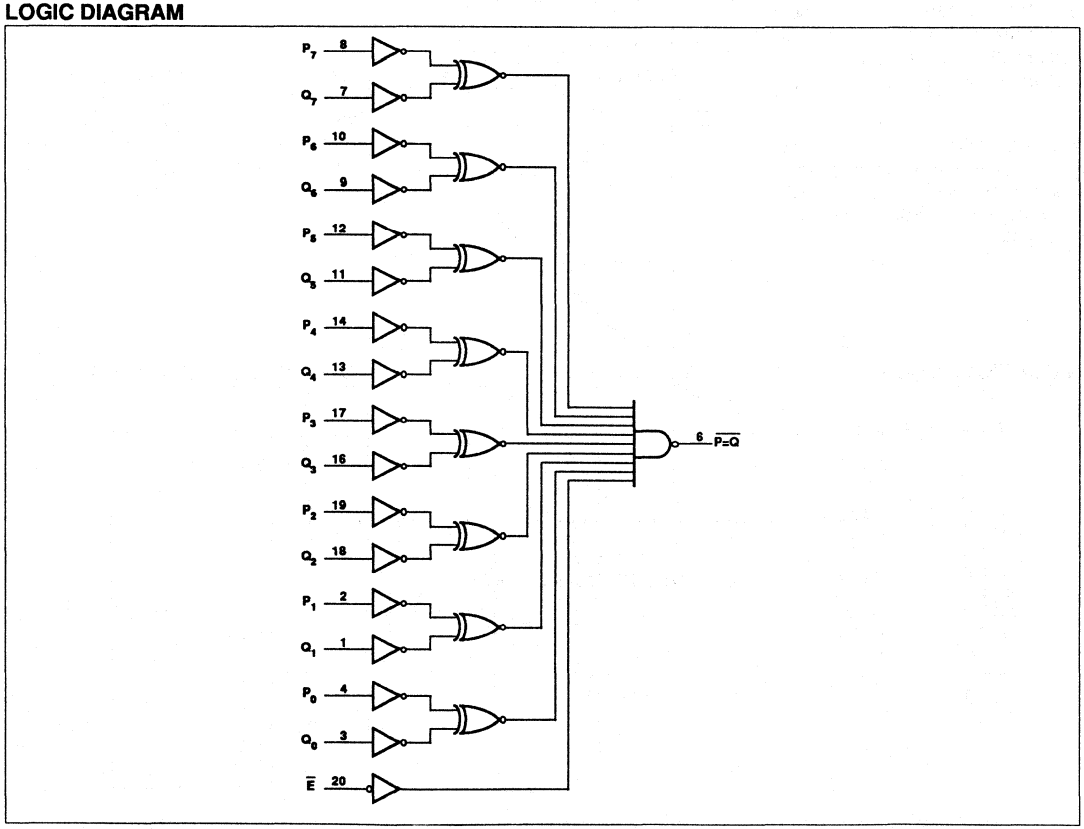
PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
4, 2, 19, 17 14, 12, 10, 8	P_0 to P_7	Data inputs
3, 1, 18, 16 13, 11, 9, 7	Q_0 to Q_7	Data inputs
20	$\overline{E}$	Enable input (active Low)
6	$\overline{P=Q}$	Output
5	GND	Ground (0V)
15	V_{CC}	Positive supply voltage

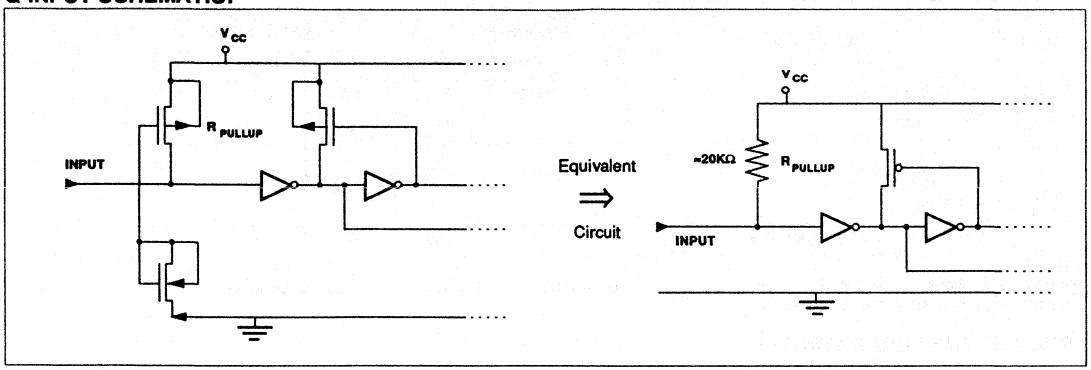
FUNCTION TABLE

INPUTS		OUTPUT
DATA P, Q	ENABLE $\overline{E}$	$\overline{P=Q}$
P = Q	L	L
P > Q	L	H
P < Q	L	H
X	H	H

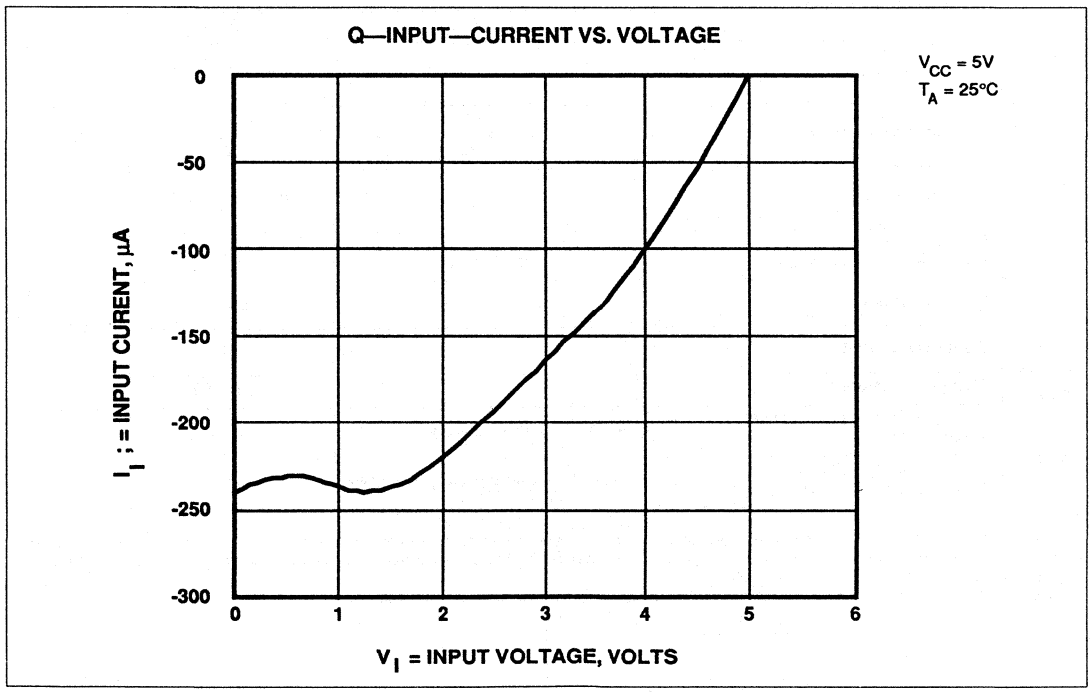
LOGIC DIAGRAM



Q-INPUT SCHEMATIC:



TYPICAL Q-INPUT CHARACTERISTICS



RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	74AC11520			74ACT11520			UNIT
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	DC supply voltage	3.0[1]	5.0	5.5	4.5	5.0	5.5	V
V_I	Input voltage	0		V_{CC}	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	0		V_{CC}	V
$\Delta t/\Delta v$	Input transition rise or fall rate	0		10	0		10	ns/V
T_A	Operating free-air temperature	-40		+85	-40		+85	°C

NOTE:
1. No electrical or switching characteristics are specified at $V_{CC} < 3V$. Operation between 2V and 3V is not recommended, but within that range, a device output will maintain a previously established logic state.

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	TEST CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 to+7.0	V
I_{IK} or V_I	DC input diode current[2]	$V_I < 0$	-20	mA
		$V_I > V_{CC}$	20	
	DC input voltage		-0.5 to V_{CC} +0.5	V
I_{OK} or V_O	DC output diode current[2]	$V_O < 0$	-50	mA
		$V_O > V_{CC}$	50	
	DC output voltage		-0.5 to V_{CC} +0.5	V
I_O	DC output source or sink current per output pin	V_O = 0 to V_{CC}	±50	mA
I_{CC} or I_{GND}	DC V_{CC} current		±100	mA
	DC ground current		±100	
T_{STG}	Storage temperature		-65 to 150	°C
P_{TOT}	Power dissipation per package Plastic DIP	Above 70°C:derate linearly by 8mW/K	500	mW
	Power dissipation per package Plastic surface mount (SO)	Above 70°C:derate linearly by 6mW/K	400	mW

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		V_{CC}	74AC11520				74ACT11520				UNIT
					T_A = +25°C		T_A = -40°C to +85°C		T_A = +25°C		T_A = -40°C to +85°C		
				V	Min	Max	Min	Max	Min	Max	Min	Max	
V_{IH}	High-level input voltage			3.0	2.10		2.10						V
				4.5	3.15		3.15		2.0		2.0		
				5.5	3.85		3.85		2.0		2.0		
V_{IL}	Low-level input voltage			3.0		0.90		0.90					V
				4.5		1.35		1.35		0.8		0.8	
				5.5		1.65		1.65		0.8		0.8	
V_{OH}	High-level output voltage	V_I = V_{IL} or V_{IH}	I_{OH} = -50μA	3.0	2.9		2.9						V
				4.5	4.4		4.4		4.4		4.4		
				5.5	5.4		5.4		5.4		5.4		
			I_{OH} = -4mA	3.0	2.58		2.48						
			I_{OH} = -24mA	4.5	3.94		3.8		3.94		3.8		
				5.5	4.94		4.8		4.94		4.8		
			I_{OH} = -75mA[1]	5.5			3.85				3.85		
V_{OL}	Low-level output voltage	V_I = V_{IL} or V_{IH}	I_{OL} = 50μA	3.0		0.1		0.1					V
				4.5		0.1		0.1		0.1		0.1	
				5.5		0.1		0.1		0.1		0.1	
			I_{OL} = 12mA	3.0		0.36		0.44					
			I_{OL} = 24mA	4.5		0.36		0.44		0.36		0.44	
				5.5		0.36		0.44		0.36		0.44	
			I_{OL} = 75mA[1]	5.5				1.65				1.65	
I_I	Input leakage current†	P and $\overline{E}$ inputs only V_I = V_{CC} or GND		5.5		±0.1		±1.0		±0.1		±1.0	μA
I_{CC}	Quiescent supply current†	Q inputs open; P and $\overline{E}$ inputs, V_I = V_{CC} or GND		5.5		8.0		80		8.0		80	μA
ΔI_{CC}	Supply current, TTL inputs High[2]	Q inputs open; P and $\overline{E}$ inputs, one input at 3.4V and other inputs at V_{CC} or GND		5.5						0.9		1.0	mA

NOTES:
1. Not more than one output should be tested at a time, and the duration of the test should not exceed 10ms.
2. This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0V or V_{CC}.

† Refer to the following DC ELECTRICAL CHARACTERISTICS ADDENDUM table.

DC ELECTRICAL CHARACTERISTICS ADDENDUM

SYMBOL	PARAMETER	TEST CONDITIONS	V_{CC}	74AC11520				74ACT11520				UNIT
				T_A = +25°C		T_A = -40°C to +85°C		T_A = +25°C		T_A = -40°C to +85°C		
			V	Typ	Max	Min	Max	Typ	Max	Min	Max	
I_{IH}	Input current	Q inputs only, V_I = V_{CC}	5.5		10		10		10		10	μA
I_{IL}	Input current	Q inputs only, V_I = GND	5.5	-0.3	-0.6		-1.0	-0.3	-0.6		-1.0	mA
I_{CC}	Quiescent supply current	Q inputs, V_I = GND; P and $\overline{E}$ inputs, V_I = V_{CC} or GND	5.5	2.3	4.8		8.0	2.3	4.8		8.0	mA

AC ELECTRICAL CHARACTERISTICS AT 3.3V ±0.3V

SYMBOL	PARAMETER	WAVEFORM	74AC11520					UNIT
			T_A = +25°C			T_A = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay P_n, Q_n to $\overline{P=Q}$	1	1.5 1.5	12.0 10.4	16.5 14.4	1.5 1.5	18.6 16.3	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{E}$ to $\overline{P=Q}$	1	1.5 1.5	6.9 6.3	9.0 8.6	1.5 1.5	10.0 9.5	ns

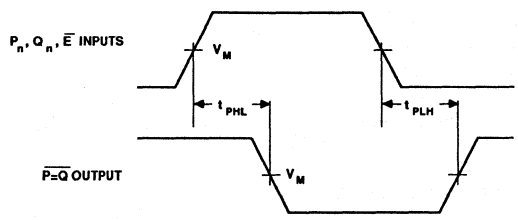
AC ELECTRICAL CHARACTERISTICS AT 5.0V ±0.5V

SYMBOL	PARAMETER	WAVEFORM	74AC11520					UNIT
			T_A = +25°C			T_A = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay P_n, Q_n to $\overline{P=Q}$	1	1.5 1.5	8.1 7.1	11.1 10.1	1.5 1.5	12.6 11.3	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{E}$ to $\overline{P=Q}$	1	1.5 1.5	4.9 4.8	6.6 7.1	1.5 1.5	7.4 7.8	ns

AC ELECTRICAL CHARACTERISTICS AT 5.0V ±0.5V

SYMBOL	PARAMETER	WAVEFORM	74ACT11520					UNIT
			T_A = +25°C			T_A = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay P_n, Q_n to $\overline{P=Q}$	1	1.5 1.5	8.6 8.0	12.7 12.4	1.5 1.5	14.3 13.9	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{E}$ to $\overline{P=Q}$	1	1.5 1.5	6.4 5.8	8.5 9.0	1.5 1.5	9.5 9.8	ns

AC WAVEFORMS

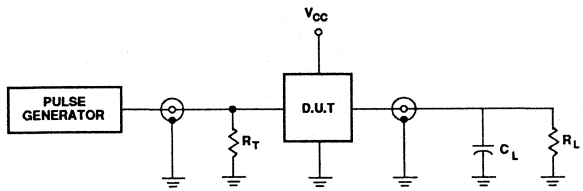


Waveform 1. Waveforms Showing the Inputs (P_n, Q_n, $\overline{E}$) to Output ($\overline{P=Q}$) Propagation Delays

WAVEFORM CONDITIONS

	INPUTS	OUTPUTS
AC	V_{IN} = GND to V_{CC}, V_M = 50% V_{CC}	$V_{OUT} = V_{OL}$ to V_{OH}
ACT	V_{IN} = GND to 3.0V, V_M = 1.5V	V_M = 50% V_{CC}

TEST CIRCUIT



Test Circuit

DEFINITIONS

C_L = Load capacitance, 50pF; includes jig and probe capacitance

R_L = Load resistor, 500Ω

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators

Input pulses: PRR ≤ 10MHz

$t_r = t_f$ = 3ns

74AC/ACT11521

8-Bit Identity Comparator

Product Specification

FEATURES

- **Compares two 8-bit words**
- **Output capability: ±24 mA**
- **Inputs are TTL-voltage compatible**
- **CMOS (AC) and TTL (ACT) voltage level inputs**
- **50Ω incident wave switching**
- **Center-pin V_{CC} and ground configuration to minimize high-speed switching noise**
- **I_{CC} category: MSI**

DESCRIPTION

The 74AC/ACT11521 high-performance CMOS devices combine very high speed and high output drive comparable to the most advanced TTL families.

The 74AC/ACT11521 identity comparators perform comparisons on two 8-bit binary or BCD words and provides a Low output when the two words match bit for bit.

The 74AC/ACT11521 identity comparators also feature a provision for $\overline{P=Q}$ totem-pole outputs.

GENERAL INFORMATION

SYMBOL	PARAMETER	CONDITIONS T_A = 25°C; GND = 0V; V_{CC} = 5.0V	TYPICAL		UNIT
			AC	ACT	
t_{PLH}/t_{PHL}	Propagation delay P_n or Q_n to $\overline{P=Q}$	C_L = 50pF	7.8	8.5	ns
C_{PD}	Power dissipation capacitance[1]	f = 1MHz; C_L = 50pF	42	40	pF
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	3.5	3.5	pF
I_{LATCH}	Latch-up current	Per Jedec JC40.2 Standard 17	500	500	mA

Note:

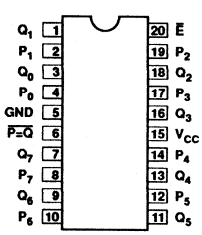
1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_I + \Sigma (C_L \times V_{CC}^2 \times f_O)$ where:
   f_I = input frequency in MHz, C_L = output load capacitance in pF,
   f_O = output frequency in MHz, V_{CC} = supply voltage in V,
   $\Sigma (C_L \times V_{CC}^2 \times f_O)$ = sum of outputs

ORDERING INFORMATION

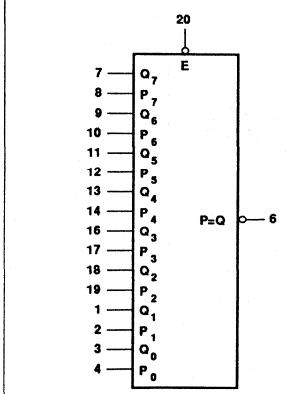
PACKAGES	TEMPERATURE RANGE	ORDER CODE
20-pin plastic DIP (300mil-wide)	-40°C to +85°C	74AC11521N 74ACT11521N
20-pin plastic SO (300mil-wide)	-40°C to +85°C	74AC11521D 74ACT11521D

PIN CONFIGURATION

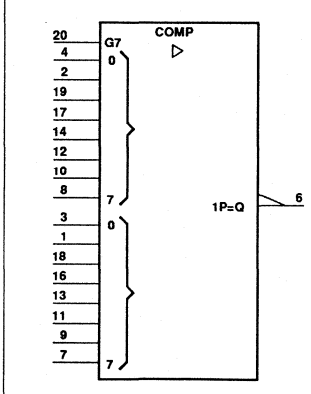
N and D Packages



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



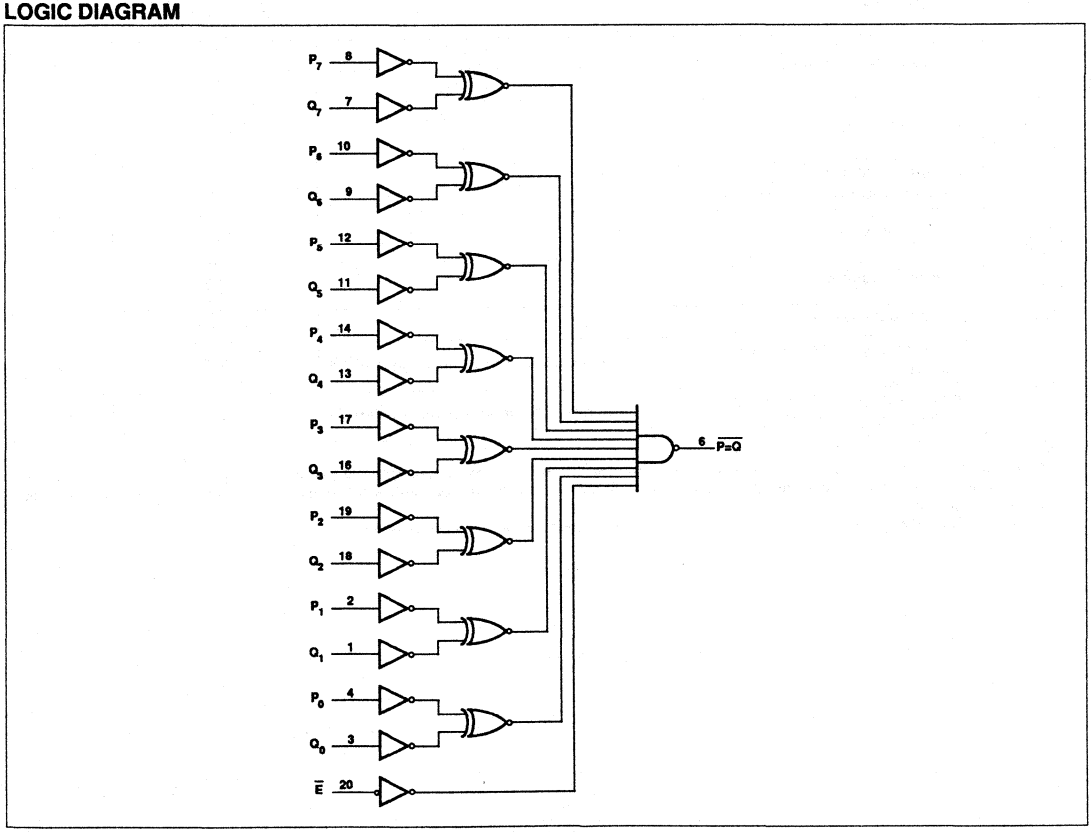
PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
4, 2, 19, 17 14, 12, 10, 8	P_0 to P_7	Data inputs
3, 1, 18, 16 13, 11, 9, 7	Q_0 to Q_7	Data inputs
20	$\overline{E}$	Enable input (active Low)
6	$\overline{P=Q}$	Output
5	GND	Ground (0V)
15	V_{CC}	Positive supply voltage

FUNCTION TABLE

INPUTS		OUTPUT
DATA P, Q	ENABLE $\overline{E}$	$\overline{P=Q}$
P = Q	L	L
P > Q	L	H
P < Q	L	H
X	H	H

LOGIC DIAGRAM



RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	74AC11521			74ACT11521			UNIT
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	DC supply voltage	3.0[1]	5.0	5.5	4.5	5.0	5.5	V
V_I	Input voltage	0		V_{CC}	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	0		V_{CC}	V
$\Delta t/\Delta v$	Input transition rise or fall rate	0		10	0		10	ns/V
T_A	Operating free-air temperature	-40		+85	-40		+85	°C

NOTE:
1. No electrical or switching characteristics are specified at V_{CC} < 3V. Operation between 2V and 3V is not recommended, but within that range, a device output will maintain a previously established logic state.

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	TEST CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 to+7.0	V
I_{IK} or V_I	DC input diode current[2]	$V_I < 0$	-20	mA
		$V_I > V_{CC}$	20	
	DC input voltage		-0.5 to V_{CC} +0.5	V
I_{OK} or V_O	DC output diode current[2]	$V_O < 0$	-50	mA
		$V_O > V_{CC}$	50	
	DC output voltage		-0.5 to V_{CC} +0.5	V
I_O	DC output source or sink current per output pin	V_O = 0 to V_{CC}	±50	mA
I_{CC} or I_{GND}	DC V_{CC} current		±100	mA
	DC ground current		±100	
T_{STG}	Storage temperature		-65 to 150	°C
P_{TOT}	Power dissipation per package Plastic DIP	Above 70°C:derate linearly by 8mW/K	500	mW
	Power dissipation per package Plastic surface mount (SO)	Above 70°C:derate linearly by 6mW/K	400	mW

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		V_{CC}	74AC11521				74ACT11521				UNIT
					T_A = +25°C		T_A = -40°C to +85°C		T_A = +25°C		T_A = -40°C to +85°C		
				V	Min	Max	Min	Max	Min	Max	Min	Max	
V_{IH}	High-level input voltage			3.0	2.10		2.10						V
				4.5	3.15		3.15		2.0		2.0		
				5.5	3.85		3.85		2.0		2.0		
V_{IL}	Low-level input voltage			3.0		0.90		0.90					V
				4.5		1.35		1.35		0.8		0.8	
				5.5		1.65		1.65		0.8		0.8	
V_{OH}	High-level output voltage	V_I = V_{IL} or V_{IH}	I_{OH} = -50μA	3.0	2.9		2.9						V
				4.5	4.4		4.4		4.4		4.4		
				5.5	5.4		5.4		5.4		5.4		
			I_{OH} = -4mA	3.0	2.58		2.48						
			I_{OH} = -24mA	4.5	3.94		3.8		3.94		3.8		
				5.5	4.94		4.8		4.94		4.8		
			I_{OH} = -75mA[1]	5.5			3.85				3.85		
V_{OL}	Low-level output voltage	V_I = V_{IL} or V_{IH}	I_{OL} = 50μA	3.0		0.1		0.1					V
				4.5		0.1		0.1		0.1		0.1	
				5.5		0.1		0.1		0.1		0.1	
			I_{OL} = 12mA	3.0		0.36		0.44					
			I_{OL} = 24mA	4.5		0.36		0.44		0.36		0.44	
				5.5		0.36		0.44		0.36		0.44	
			I_{OL} = 75mA[1]	5.5				1.65				1.65	
I_I	Input leakage current	V_I = V_{CC} or GND		5.5		±0.1		±1.0		±0.1		±1.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC} or GND, I_O = 0		5.5		8.0		80		8.0		80	μA
ΔI_{CC}	Supply current, TTL inputs High[2]	One input at 3.4V, other inputs at V_{CC} or GND		5.5						0.9		1.0	mA

NOTES:
1. Not more than one output should be tested at a time, and the duration of the test should not exceed 10ms.
2. This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0V or V_{CC}.

AC ELECTRICAL CHARACTERISTICS AT 3.3V ±0.3V

SYMBOL	PARAMETER	WAVEFORM	74AC11521					UNIT
			T_A = +25°C			T_A = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay P_n, Q_n to $\overline{P=Q}$	1	1.5 1.5	12.5 10.5	16.6 14.1	1.5 1.5	19.0 16.1	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{E}$ to $\overline{P=Q}$	1	1.5 1.5	7.1 6.4	9.8 8.8	1.5 1.5	10.8 10.1	ns

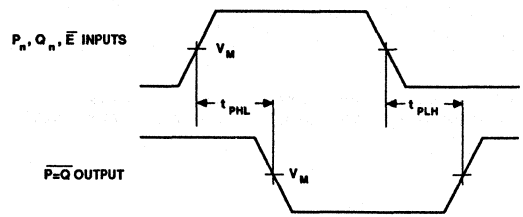
AC ELECTRICAL CHARACTERISTICS AT 5.0V ±0.5V

SYMBOL	PARAMETER	WAVEFORM	74AC11521					UNIT
			T_A = +25°C			T_A = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay P_n, Q_n to $\overline{P=Q}$	1	1.5 1.5	8.3 7.2	11.3 10.1	1.5 1.5	13.0 11.4	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{E}$ to $\overline{P=Q}$	1	1.5 1.5	5.1 4.8	7.1 7.1	1.5 1.5	7.9 8.1	ns

AC ELECTRICAL CHARACTERISTICS AT 5.0V ±0.5V

SYMBOL	PARAMETER	WAVEFORM	74ACT11521					UNIT
			T_A = +25°C			T_A = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay P_n, Q_n to $\overline{P=Q}$	1	1.5 1.5	8.8 8.2	13.0 12.0	1.5 1.5	14.7 13.6	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{E}$ to $\overline{P=Q}$	1	1.5 1.5	6.7 6.8	9.3 8.8	1.5 1.5	10.5 9.7	ns

AC WAVEFORMS

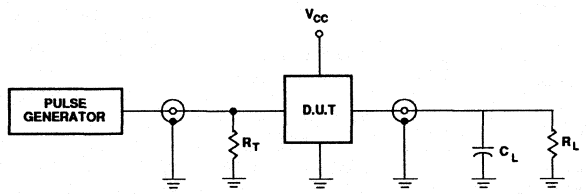


Waveform 1. Waveforms Showing the Inputs (P_n, Q_n, $\overline{E}$) to Output ($\overline{P=Q}$) Propagation Delays

WAVEFORM CONDITIONS

	INPUTS	OUTPUTS
AC	V_{IN} = GND to V_{CC}, V_M = 50% V_{CC}	V_{OUT} = V_{OL} to V_{OH}
ACT	V_{IN} = GND to 3.0V, V_M = 1.5V	V_M = 50% V_{CC}

TEST CIRCUIT



Test Circuit

DEFINITIONS

C_L = Load capacitance, 50pF; includes jig and probe capacitance

R_L = Load resistor, 500Ω

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators

Input pulses: PRR ≤ 10MHz

$t_r = t_f$ = 3ns

74AC/ACT11533

Octal D-Type Transparent Latch (3–State), INV

Product Specification

FEATURES

- **8-bit transparent latch**
- **3-State output buffers**
- **Common 3-State Output Enable**
- **Independent register and 3-State buffer operation**
- **Output capability: ±24 mA**
- **CMOS (AC) and TTL (ACT) voltage level inputs**
- **50Ω incident wave switching**
- **Center-pin V_{CC} and ground configuration to minimize high-speed switching noise**
- **I_{CC} category: MSI**

DESCRIPTION

The 74AC/ACT11533 high-performance CMOS devices combine very high speed and high output drive comparable to the most advanced TTL families.

The 74AC/ACT11533 device is an octal transparent latch coupled to eight 3-State inverting output buffers. The two sections of the device are controlled independently by Latch Enable (LE) and Output Enable ($\overline{OE}$) control gates.

The data on the D inputs are transferred to the latch outputs when the Latch Enable (LE) input is High. The latch remains

GENERAL INFORMATION

SYMBOL	PARAMETER	CONDITIONS T_A = 25°C; GND = 0V; V_{CC} = 5.0V		TYPICAL AC	TYPICAL ACT	UNIT
t_{PLH}/ t_{PHL}	Propagation delay D_n to $\overline{Q}_n$	C_L = 50pF		5.3	6.8	ns
C_{PD}	Power dissipation capacitance per latch[1]	f = 1MHz; C_L = 50pF	Enabled	55	69	pF
			Disabled	44	58	
C_{IN}	Input capacitance	V_I = 0V or V_{CC}		4.0	4.0	pF
C_{OUT}	Output capacitance	V_I = 0V or V_{CC}; Disabled		10	10	pF
I_{LATCH}	Latch-up current	Per Jedec JC40.2 Standard 17		500	500	mA

Note:

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):

$$P_D = C_{PD} \times V_{CC}^2 \times f_I + \Sigma (C_L \times V_{CC}^2 \times f_O)$$ where:

f_I = input frequency in MHz, C_L = output load capacitance in pF,

f_O = output frequency in MHz, V_{CC} = supply voltage in V,

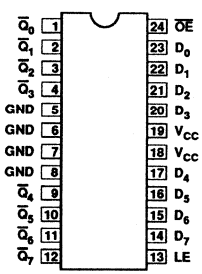
$\Sigma (C_L \times V_{CC}^2 \times f_O)$ = sum of outputs

ORDERING INFORMATION

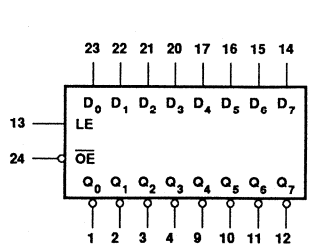
PACKAGES	TEMPERATURE RANGE	ORDER CODE
24-pin plastic DIP (300mil-wide)	-40°C to +85°C	74AC11533N 74ACT11533N
24-pin plastic SO (300mil-wide)	-40°C to +85°C	74AC11533D 74ACT11533D

PIN CONFIGURATION

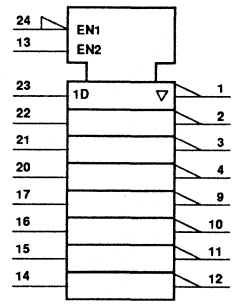
N and D Packages



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



transparent to the data inputs while LE is High, and stores the data that is present one setup time before the High-to-Low enable transition.

The 3-State inverting output buffers are designed to drive heavily loaded 3-State buses, MOS memories, or MOS microprocessors. The active-Low Output Enable ($\overline{OE}$) controls all eight 3-State buffers independent of the latch operation.

When $\overline{OE}$ is Low, the latched or transparent data appears at the outputs. When $\overline{OE}$ is High, the outputs are in the High-impedance "OFF" state, which means they will neither drive nor load the bus.

PIN DESCRIPTION

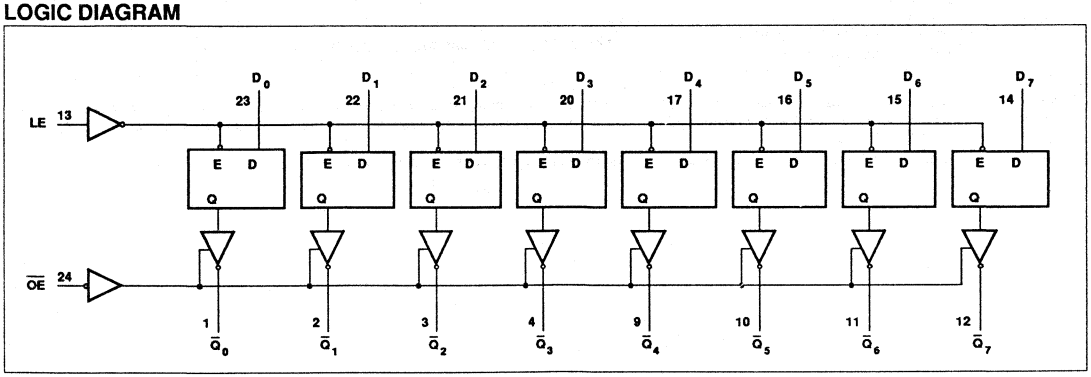
PIN NUMBER	SYMBOL	NAME AND FUNCTION
24	$\overline{OE}$	Output enable
23, 22, 21, 20, 17, 16, 15, 14	$D_0 - D_7$	Data inputs
1, 2, 3, 4, 9, 10, 11, 12	$\overline{Q}_0 - \overline{Q}_7$	Data outputs
13	LE	Latch enable
5, 6, 7, 8	GND	Ground (0V)
18, 19	V_{CC}	Positive supply voltage

FUNCTION TABLE

OPERATING MODES	INPUTS			INTERNAL REGISTER	OUTPUTS
	$\overline{OE}$	LE	D_n		$\overline{Q}_n$
Enable and read register	L	H	L	L	H
	L	H	H	H	L
Latch and read register	L	↓	l	L	H
	L	↓	h	H	L
Hold	L	L	X	NC	NC
Disable outputs	H	X	X	X	Z

H = High voltage level steady state
h = High voltage level one set-up time prior to the High-to-Low E transition
L = Low voltage level steady state
l = Low voltage level one set-up time prior to the High-to-Low E transition
X = Don't care
NC = No change
Z = High-impedance "OFF" state
↓ = High-to-Low transition

LOGIC DIAGRAM



RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		74AC11533			74ACT11533			UNIT
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	DC supply voltage		3.0[1]	5.0	5.5	4.5	5.0	5.5	V
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
$\Delta t/\Delta v$	Input transition rise or fall rate	Data, LE	0		10	0		10	ns/V
		Output enable	0		10	0		10	
T_A	Operating free-air temperature		-40		+85	-40		+85	°C

NOTE:

1. No electrical or switching characteristics are specified at V_{CC} < 3V. Operation between 2V and 3V is not recommended, but within that range, a device output will maintain a previously established logic state.

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	TEST CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 to+7.0	V
I_{IK} or V_I	DC input diode current[2]	$V_I < 0$	-20	mA
		$V_I > V_{CC}$	20	
	DC input voltage		-0.5 to V_{CC} +0.5	V
I_{OK} or V_O	DC output diode current[2]	$V_O < 0$	-50	mA
		$V_O > V_{CC}$	50	
	DC output voltage		-0.5 to V_{CC} +0.5	V
I_O	DC output source or sink current per output pin	V_O = 0 to V_{CC}	±50	mA
I_{CC} or I_{GND}	DC V_{CC} current		±200	mA
	DC ground current		±200	
T_{STG}	Storage temperature		-65 to 150	°C
P_{TOT}	Power dissipation per package Plastic DIP	Above 70°C:derate linearly by 8mW/K	500	mW
	Power dissipation per package Plastic surface mount (SO)	Above 70°C:derate linearly by 6mW/K	400	mW

NOTES:

1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		V_{CC}	74AC11533				74ACT11533				UNIT
					T_A = +25°C		T_A = -40°C to +85°C		T_A = +25°C		T_A = -40°C to +85°C		
				V	Min	Max	Min	Max	Min	Max	Min	Max	
V_{IH}	High-level input voltage			3.0	2.10		2.10						V
				4.5	3.15		3.15		2.0		2.0		
				5.5	3.85		3.85		2.0		2.0		
V_{IL}	Low-level input voltage			3.0		0.90		0.90					V
				4.5		1.35		1.35		0.8		0.8	
				5.5		1.65		1.65		0.8		0.8	
V_{OH}	High-level output voltage	V_I = V_{IL} or V_{IH}	I_{OH} = -50μA	3.0	2.9		2.9						V
				4.5	4.4		4.4		4.4		4.4		
				5.5	5.4		5.4		5.4		5.4		
			I_{OH} = -4mA	3.0	2.58		2.48						
			I_{OH} = -24mA	4.5	3.94		3.8		3.94		3.8		
				5.5	4.94		4.8		4.94		4.8		
			I_{OH} = -75mA[1]	5.5			3.85				3.85		
V_{OL}	Low-level output voltage	V_I = V_{IL} or V_{IH}	I_{OL} = 50μA	3.0		0.1		0.1					V
				4.5		0.1		0.1		0.1		0.1	
				5.5		0.1		0.1		0.1		0.1	
			I_{OL} = 12mA	3.0		0.36		0.44					
			I_{OL} = 24mA	4.5		0.36		0.44		0.36		0.44	
				5.5		0.36		0.44		0.36		0.44	
			I_{OL} = 75mA[1]	5.5				1.65				1.65	
I_I	Input leakage current	V_I = V_{CC} or GND		5.5		±0.1		±1.0		±0.1		±1.0	μA
I_{OZ}	3-State output off-state current	V_I = V_{IL} or V_{IH}, V_O = V_{CC} or GND		5.5		±0.5		±5.0		±0.5		±5.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC} or GND, I_O = 0		5.5		8.0		80		8.0		80	μA
ΔI_{CC}	Supply current, TTL inputs High[2]	One input at 3.4V, other inputs at V_{CC} or GND		5.5						0.9		1.0	mA

NOTES:
1. Not more than one output should be tested at a time, and the duration of the test should not exceed 10ms.
2. This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0V or V_{CC}.

AC ELECTRICAL CHARACTERISTICS AT 3.3V ±0.3V

SYMBOL	PARAMETER	WAVEFORM	74AC11533					UNIT
			T_A = +25°C			T_A = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay D_n to $\overline{Q}_n$	1	1.5 1.5	8.5 7.5	12.6 10.1	1.5 1.5	14.3 11.3	ns
t_{PLH} t_{PHL}	Propagation delay LE to $\overline{Q}_n$	4	1.5 1.5	10.0 9.5	14.5 12.8	1.5 1.5	16.5 14.3	ns
t_{PZH} t_{PZL}	Output enable time to High and Low level	2	1.5 1.5	9.0 8.5	13.1 11.6	1.5 1.5	14.7 13.1	ns
t_{PHZ} t_{PLZ}	Output disable time from High and Low level	2	1.5 1.5	9.5 7.5	12.0 10.2	1.5 1.5	12.8 11.0	ns
t_W	LE Pulse Width High or Low	4	5.5			5.5		ns
t_S	Setup time D_n to LE↓	3	4.0			4.0		ns
t_H	Hold time D_n to LE↓	3	2.0			2.0		ns

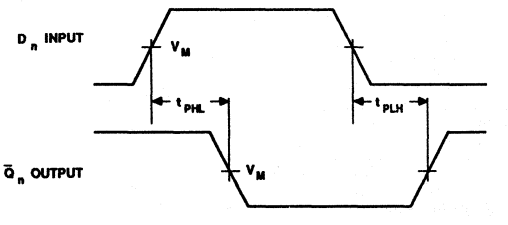
AC ELECTRICAL CHARACTERISTICS AT 5.0V ±0.5V

SYMBOL	PARAMETER	WAVEFORM	74AC11533					UNIT
			T_A = +25°C			T_A = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay D_n to $\overline{Q}_n$	1	1.5 1.5	5.5 5.0	8.4 7.1	1.5 1.5	9.8 8.0	ns
t_{PLH} t_{PHL}	Propagation delay LE to $\overline{Q}_n$	4	1.5 1.5	6.5 6.5	10.0 9.1	1.5 1.5	11.3 10.3	ns
t_{PZH} t_{PZL}	Output enable time to High and Low level	2	1.5 1.5	6.5 6.0	9.5 8.6	1.5 1.5	10.8 9.7	ns
t_{PHZ} t_{PLZ}	Output disable time from High and Low level	2	1.5 1.5	8.5 6.0	10.7 8.2	1.5 1.5	11.4 8.9	ns
t_W	LE Pulse Width High or Low	4	4.0			4.0		ns
t_S	Setup time D_n to LE↓	3	3.5			3.5		ns
t_H	Hold time D_n to LE↓	3	2.0			2.0		ns

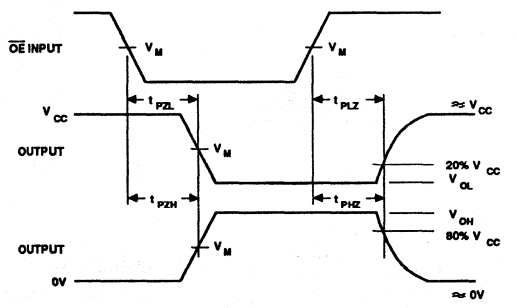
AC ELECTRICAL CHARACTERISTICS AT 5.0V ±0.5V

SYMBOL	PARAMETER	WAVEFORM	74ACT11533					UNIT
			T_A = +25°C			T_A = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay D_n to $\overline{Q}_n$	1	1.5 1.5	7.0 6.5	10.1 8.4	1.5 1.5	11.3 9.5	ns
t_{PLH} t_{PHL}	Propagation delay LE to $\overline{Q}_n$	4	1.5 1.5	8.5 8.5	11.3 10.7	1.5 1.5	13.0 12.2	ns
t_{PZH} t_{PZL}	Output enable time to High and Low level	2	1.5 1.5	7.5 7.5	10.7 10.9	1.5 1.5	12.5 12.0	ns
t_{PHZ} t_{PLZ}	Output disable time from High and Low level	2	1.5 1.5	10.5 7.5	12.1 9.5	1.5 1.5	12.8 10.3	ns
t_W	LE Pulse Width High or Low	4	5.0			5.0		ns
t_S	Setup time D_n to LE↓	3	3.5			3.5		ns
t_H	Hold time D_n to LE↓	3	3.5			3.5		ns

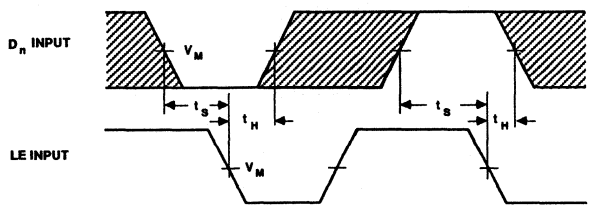
AC WAVEFORMS



Waveform 1. Waveforms Showing the Input (D_n) to Output ($\overline{Q}_n$) Propagation Delays

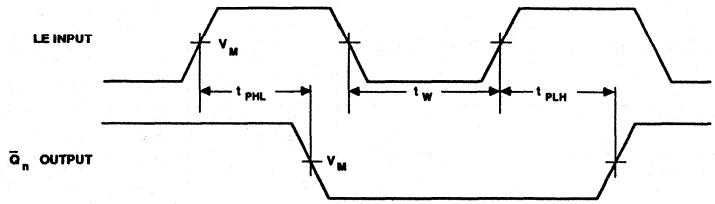


Waveform 2. Waveforms Showing the 3-State Output Enable and Disable Times



Waveform 3. Waveforms Showing the Data Setup and Hold Times for D_n Input to LE Input

AC WAVEFORMS (Continued)

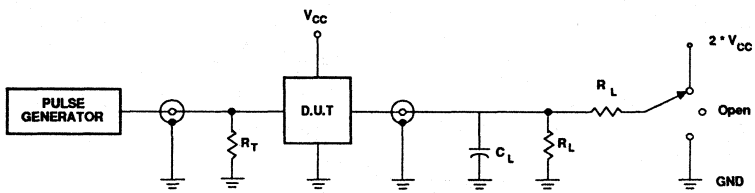


Waveform 4. Waveforms Showing the Latch Enable Input (LE) Pulse Width and the Latch Enable Input to Output ($\overline{Q}_n$) Propagation Delays

WAVEFORM CONDITIONS

	INPUTS	OUTPUTS
AC	V_{IN} = GND to V_{CC}, V_M = 50% V_{CC}	$V_{OUT} = V_{OL}$ to V_{OH}
ACT	V_{IN} = GND to 3.0V, V_M = 1.5V	V_M = 50% V_{CC}

TEST CIRCUIT



Test Circuit

TEST	S1
t_{PLH}/t_{PHL}	Open
$t_{PLZ}t_{PZL}$	2*VCC
t_{PHZ}/t_{PZH}	GND

SWITCH POSITION

DEFINITIONS

C_L = Load capacitance, 50pF; includes jig and probe capacitance

R_L = Load resistor, 500Ω

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators

Input pulses: PRR ≤ 10MHz

$t_r = t_f$ = 3ns

74AC/ACT11534

Octal D-Type Flip-Flop; Positive-Edge Trigger (3-State), INV

Product Specification

FEATURES

- **3-State output buffers**
- **Common 3-State Output Enable**
- **Independent register and 3-State buffer operation**
- **Output capability: ±24 mA**
- **CMOS (AC) and TTL (ACT) voltage level inputs**
- **50Ω incident wave switching**
- **Center-pin V_{CC} and ground configuration to minimize high-speed switching noise**
- **I_{CC} category: MSI**

DESCRIPTION

The 74AC/ACT11534 high-performance CMOS devices combine very high speed and high output drive comparable to the most advanced TTL families.

The 74AC/ACT11534 device is an 8-bit, edge-triggered register coupled to eight 3-State, inverting output buffers. The two sections of the device are controlled independently by Clock (CP) and Output Enable ($\overline{OE}$) control gates. The register is fully edge-triggered. Once the set-up requirements are met, when the Clock Pulse (CP) rises the state of each D input is transferred to the corresponding flip-flop's $\overline{Q}$ output.

GENERAL INFORMATION

SYMBOL	PARAMETER	CONDITIONS T_A = 25°C; GND = 0V; V_{CC} = 5.0V		TYPICAL AC	TYPICAL ACT	UNIT
t_{PLH}/t_{PHL}	Propagation delay CP to $\overline{Q}_n$	C_L = 50pF		7.0	8.5	ns
C_{PD}	Power dissipation capacitance per flip-flop[1]	f = 1MHz; C_L = 50pF	Enabled	75	92	pF
			Disabled	65	82	
C_{IN}	Input capacitance	V_I = 0V or V_{CC}		4	4	pF
C_{OUT}	Output capacitance	V_I = 0V or V_{CC}; Disabled		10	10	pF
I_{LATCH}	Latch-up current	Per Jedec JC40.2 Standard 17		500	500	mA
f_{MAX}	Maximum clock frequency	C_L = 50pF; V_{CC} = 5.5V		100	70	MHz

Note:

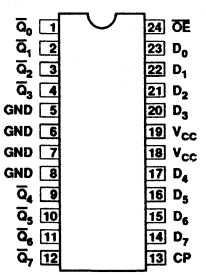
1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_I + \Sigma (C_L \times V_{CC}^2 \times f_O)$ where:
   f_I = input frequency in MHz, C_L = output load capacitance in pF,
   f_O = output frequency in MHz, V_{CC} = supply voltage in V,
   $\Sigma (C_L \times V_{CC}^2 \times f_O)$ = sum of outputs

ORDERING INFORMATION

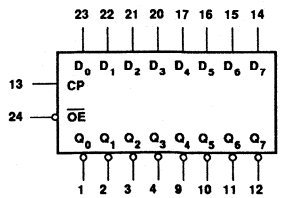
PACKAGES	TEMPERATURE RANGE	ORDER CODE
24-pin plastic DIP (300mil-wide)	-40°C to +85°C	74AC11534N 74ACT11534N
24-pin plastic SO (300mil-wide)	-40°C to +85°C	74AC11534D 74ACT11534D

PIN CONFIGURATION

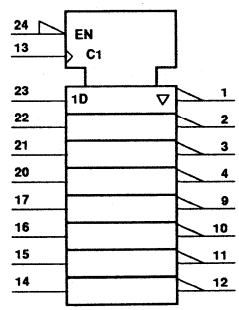
N and D Packages



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



Octal D-Type Flip-Flop; Positive-Edge Trigger (3–State), INV

The 3-State output buffers are designed to drive heavily loaded 3-State buses, MOS memories, or MOS microprocessors. The active-Low Output Enable ($\overline{OE}$) controls all eight 3-State inverting buffers independent of the clock operation.

When $\overline{OE}$ is Low, the stored data appears at the outputs. When $\overline{OE}$ is High, the outputs are in the High-impedance "OFF" state, which means they will neither drive nor load the bus.

PIN DESCRIPTION

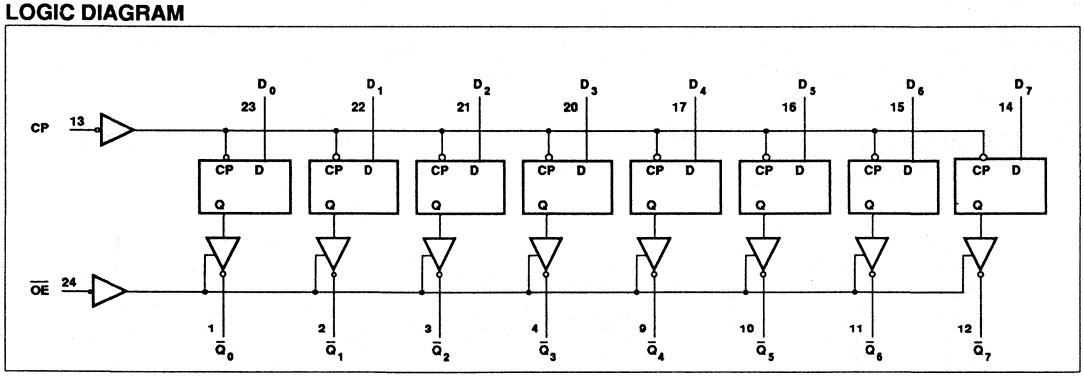
PIN NUMBER	SYMBOL	NAME AND FUNCTION
24	$\overline{OE}$	Output enable
23, 22, 21, 20, 17, 16, 15, 14	D_0 - D_7	Data inputs
1, 2, 3, 4, 9, 10, 11, 12	$\overline{Q}_0$ - $\overline{Q}_7$	Data outputs
13	CP	Clock input
5, 6, 7, 8	GND	Ground (0V)
18, 19	V_{CC}	Positive supply voltage

FUNCTION TABLE

OPERATING MODES	INPUTS			INTERNAL REGISTER	OUTPUTS
	$\overline{OE}$	CP	D_n		$\overline{Q}_n$
Load and read register	L	↑	l	L	H
	L	↑	h	H	L
Disable outputs	H	X	X	X	Z

H = High voltage level steady state
h = High voltage level one set-up time prior to the Low-to-High clock transition
L = Low voltage level steady state
l = Low voltage level one set-up time prior to the Low-to-High clock transition
X = Don't care
Z = High-impedance "OFF" state
↑ = Low-to-High transition

LOGIC DIAGRAM



RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		74AC11534			74ACT11534			UNIT
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	DC supply voltage		3.0[1]	5.0	5.5	4.5	5.0	5.5	V
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
$\Delta t/\Delta v$	Input transition rise or fall rate	Data	0		10	0		10	ns/V
		Output enable	0		5	0		10	
T_A	Operating free-air temperature		-40		+85	-40		+85	°C

NOTE:

1. No electrical or switching characteristics are specified at $V_{CC} < 3V$. Operation between 2V and 3V is not recommended, but within that range, a device output will maintain a previously established logic state.

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	TEST CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 to+7.0	V
I_{IK} or V_I	DC input diode current[2]	$V_I < 0$	-20	mA
		$V_I > V_{CC}$	20	
	DC input voltage		-0.5 to V_{CC} +0.5	V
I_{OK} or V_O	DC output diode current[2]	$V_O < 0$	-50	mA
		$V_O > V_{CC}$	50	
	DC output voltage		-0.5 to V_{CC} +0.5	V
I_O	DC output source or sink current per output pin	V_O = 0 to V_{CC}	±50	mA
I_{CC} or I_{GND}	DC V_{CC} current		±200	mA
	DC ground current		±200	
T_{STG}	Storage temperature		-65 to 150	°C
P_{TOT}	Power dissipation per package Plastic DIP	Above 70°C:derate linearly by 8mW/K	500	mW
	Power dissipation per package Plastic surface mount (SO)	Above 70°C:derate linearly by 6mW/K	400	mW

NOTES:

1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		V_{CC}	74AC11534				74ACT11534				UNIT
					T_A = +25°C		T_A = -40°C to +85°C		T_A = +25°C		T_A = -40°C to +85°C		
				V	Min	Max	Min	Max	Min	Max	Min	Max	
V_{IH}	High-level input voltage			3.0	2.10		2.10						V
				4.5	3.15		3.15		2.0		2.0		
				5.5	3.85		3.85		2.0		2.0		
V_{IL}	Low-level input voltage			3.0		0.90		0.90					V
				4.5		1.35		1.35		0.8		0.8	
				5.5		1.65		1.65		0.8		0.8	
V_{OH}	High-level output voltage	V_I = V_{IL} or V_{IH}	I_{OH} = -50μA	3.0	2.9		2.9						V
				4.5	4.4		4.4		4.4		4.4		
				5.5	5.4		5.4		5.4		5.4		
			I_{OH} = -4mA	3.0	2.58		2.48						
			I_{OH} = -24mA	4.5	3.94		3.8		3.94		3.8		
				5.5	4.94		4.8		4.94		4.8		
			I_{OH} = -75mA[1]	5.5			3.85				3.85		
V_{OL}	Low-level output voltage	V_I = V_{IL} or V_{IH}	I_{OL} = 50μA	3.0		0.1		0.1					V
				4.5		0.1		0.1		0.1		0.1	
				5.5		0.1		0.1		0.1		0.1	
			I_{OL} = 12mA	3.0		0.36		0.44					
			I_{OL} = 24mA	4.5		0.36		0.44		0.36		0.44	
				5.5		0.36		0.44		0.36		0.44	
			I_{OL} = 75mA[1]	5.5				1.65				1.65	
I_I	Input leakage current	V_I = V_{CC} or GND		5.5		±0.1		±1.0		±0.1		±1.0	μA
I_{OZ}	3-State output off-state current	V_I = V_{IL} or V_{IH}, V_O = V_{CC} or GND		5.5		±0.5		±5.0		±0.5		±5.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC} or GND, I_O = 0		5.5		8.0		80		8.0		80	μA
ΔI_{CC}	Supply current, TTL inputs High[2]	One input at 3.4V, other inputs at V_{CC} or GND		5.5						0.9		1.0	mA

NOTES:

1. Not more than one output should be tested at a time, and the duration of the test should not exceed 10ms.
2. This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0V or V_{CC}.

AC ELECTRICAL CHARACTERISTICS AT 3.3V ±0.3V

SYMBOL	PARAMETER	WAVEFORM	74AC11534					UNIT
			T_A = +25°C			T_A = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	1	50	75		50		MHz
t_{PLH} t_{PHL}	Propagation delay CP to $\overline{Q}_n$	1	1.5 1.5	11.0 11.0	15.3 15.7	1.5 1.5	17.6 17.7	ns
t_{PZH} t_{PZL}	Output enable time to High and Low level	2	1.5 1.5	9.0 9.0	12.8 12.6	1.5 1.5	14.6 14.3	ns
t_{PHZ} t_{PLZ}	Output disable time from High and Low level	2	1.5 1.5	10.0 8.0	12.6 13.0	1.5 1.5	13.3 13.8	ns
t_W	Clock pulse width High or Low	1	10.0			10.0		ns
t_S	Setup time D_n to CP	3	3.5			3.5		ns
t_H	Hold time D_n to CP	3	5.5			5.5		ns

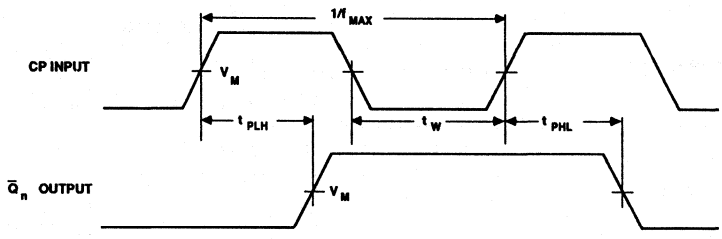
AC ELECTRICAL CHARACTERISTICS AT 5.0V ±0.5V

SYMBOL	PARAMETER	WAVEFORM	74AC11534					UNIT
			T_A = +25°C			T_A = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	1	75	100		75		MHz
t_{PLH} t_{PHL}	Propagation delay CP to $\overline{Q}_n$	1	1.5 1.5	7.0 7.0	10.3 10.7	1.5 1.5	11.7 12.1	ns
t_{PZH} t_{PZL}	Output enable time to High and Low level	2	1.5 1.5	6.0 6.0	9.2 9.2	1.5 1.5	10.4 10.4	ns
t_{PHZ} t_{PLZ}	Output disable time from High and Low level	2	1.5 1.5	9.0 6.0	11.1 8.8	1.5 1.5	11.6 9.2	ns
t_W	Clock pulse width High or Low	1	6.5			6.5		ns
t_S	Setup time D_n to CP	3	3.5			3.5		ns
t_H	Hold time D_n to CP	3	4.5			4.5		ns

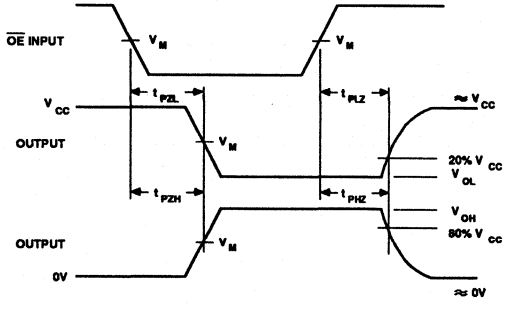
AC ELECTRICAL CHARACTERISTICS AT 5.0V ±0.5V

SYMBOL	PARAMETER	WAVEFORM	74ACT11534					UNIT
			T_A = +25°C			T_A = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	1	55	70		55		MHz
t_{PLH} t_{PHL}	Propagation delay CP to $\overline{Q}_n$	1	1.5 1.5	8.5 8.5	12.7 13.3	1.5 1.5	14.5 15.0	ns
t_{PZH} t_{PZL}	Output enable time to High and Low level	2	1.5 1.5	7.5 7.5	12.0 12.2	1.5 1.5	13.3 13.5	ns
t_{PHZ} t_{PLZ}	Output disable time from High and Low level	2	1.5 1.5	11.0 8.0	12.9 11.2	1.5 1.5	13.5 12.0	ns
t_W	Clock pulse width High or Low	1	9.0			9.0		ns
t_S	Setup time D_n to CP	3	3.0			3.0		ns
t_H	Hold time D_n to CP	3	5.5			5.5		ns

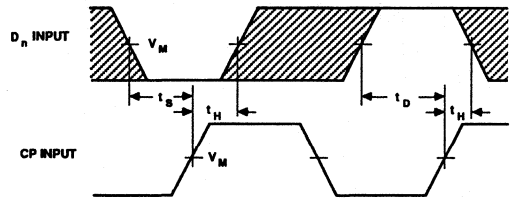
AC WAVEFORMS



Waveform 1. Waveforms Showing the Clock Input (CP) to Output ($\overline{Q}_n$) Propagation Delays and Clock Input (CP) Pulse Width



Waveform 2. Waveforms Showing the 3-State Output Enable and Disable Times

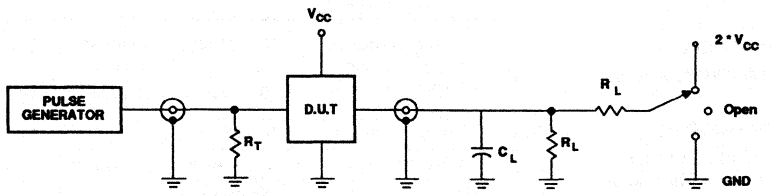


Waveform 3. Waveforms Showing the Data Set-up and Hold Times for D_n Input to CP Input

WAVEFORM CONDITIONS

	INPUTS	OUTPUTS
AC	V_{IN} = GND to V_{CC}, V_M = 50% V_{CC}	V_{OUT} = V_{OL} to V_{OH}
ACT	V_{IN} = GND to 3.0V, V_M = 1.5V	V_M = 50% V_{CC}

TEST CIRCUIT



Test Circuit

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2*VCC
t_{PHZ}/t_{PZH}	GND

SWITCH POSITION

DEFINITIONS

C_L = Load capacitance, 50pF; includes jig and probe capacitance

R_L = Load resistor, 500Ω

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators

Input pulses: PRR ≤ 10MHz

$t_r = t_f$ = 3ns

74AC/ACT11543

Octal Latched Transceiver with Dual Enable; 3-State

Objective Specification

FEATURES

- **Combines '245 and '373 type functions in one chip**
- **8-bit octal transceiver with D-type latch**
- **3-State buffers**
- **Output capability: ±24 mA**
- **CMOS (AC) and TTL (ACT) voltage level inputs**
- **50Ω incident wave switching**
- **Center-pin V_{CC} and ground configuration to minimize high-speed switching noise**
- **I_{CC} category: MSI**

DESCRIPTION

The 74AC/ACT11543 high-performance CMOS devices combine very high speed and high output drive comparable to the most advanced TTL families.

The 74AC/ACT11543 Octal Latched Transceiver contains two sets of D-type latches for temporary storage of data flowing in either direction. Separate Latch Enable ($\overline{LE}_{AB}$, $\overline{LE}_{BA}$) and Output Enable ($\overline{OE}_{AB}$, $\overline{OE}_{BA}$) inputs are provided for each register to permit independent control of inputting and outputting in either direction of data flow.

GENERAL INFORMATION

SYMBOL	PARAMETER	CONDITIONS T_A = 25°C; GND = 0V; V_{CC} = 5.0V		TYPICAL AC	TYPICAL ACT	UNIT
t_{PLH}/t_{PHL}	Propagation delay A_n to B_n or B_n to A_n	C_L = 50pF		5.3	7.0	ns
C_{PD}	Power dissipation capacitance per transceiver[1]	f = 1MHz;	Enabled	200	200	pF
		C_L = 50pF	Disabled	50	50	
C_{IN}	Input capacitance	V_I = 0V or V_{CC}		4.5	4.5	pF
$C_{I/O}$	I/Ocapacitance	$V_{I/O}$ = 0V or V_{CC}; Disabled		12	12	pF
I_{LATCH}	Latch-up current	Per Jedec JC40.2 Standard 17		500	500	mA

Note:

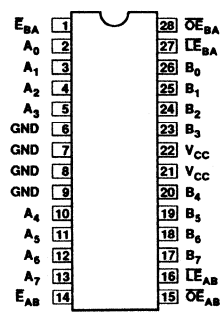
1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_I + \Sigma (C_L \times V_{CC}^2 \times f_O)$ where:
   f_I = input frequency in MHz, C_L = output load capacitance in pF,
   f_O = output frequency in MHz, V_{CC} = supply voltage in V,
   $\Sigma (C_L \times V_{CC}^2 \times f_O)$ = sum of outputs

ORDERING INFORMATION

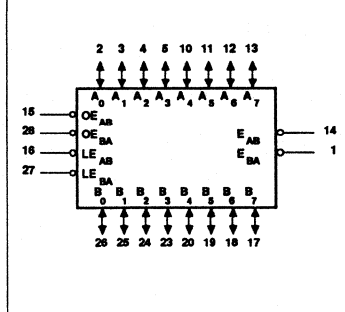
PACKAGES	TEMPERATURE RANGE	ORDER CODE
28-pin plastic DIP (300mil-wide)	-40°C to +85°C	74AC11543N 74ACT11543N
28-pin plastic SO (300mil-wide)	-40°C to +85°C	74AC11543D 74ACT11543D

PIN CONFIGURATION

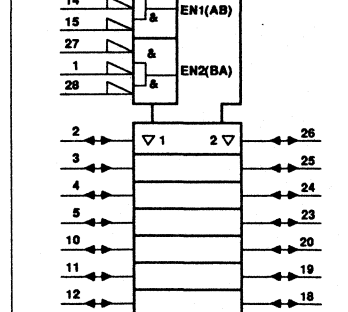
N and D Packages



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



Octal Latched Transceiver with Dual Enable; 3-State

74AC/ACT11543

FUNCTIONAL DESCRIPTION

The 74AC/ACT11543 Octal Latched Transceiver contains two sets of eight D-type latches, with separate input and controls for each set. For data flow from A to B, for example, the A-to-B Enable ($\overline{E}_{AB}$) input must be Low in order to enter data from A_0 - A_7 or take data from B_0 - B_7 as indicated in the Function Table. With $\overline{E}_{AB}$ Low, a Low signal on the A-to-B Latch Enable ($\overline{LE}_{AB}$) input makes the A-to-B latches transparent; a subsequent Low-to-High transition of the $\overline{LE}_{AB}$ signal puts the A latches in the storage mode and their outputs no longer change with the A inputs. With $\overline{E}_{AB}$ and $\overline{OE}_{AB}$ both Low, the 3-State B output buffers are active and display the data present at the outputs of the A latches. Control of data flow from B to A is similar, but using the $\overline{E}_{BA}$, $\overline{LE}_{BA}$, and $\overline{OE}_{BA}$ inputs.

PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
15	$\overline{OE}_{AB}$	A-to-B output enable input (active Low)
28	$\overline{OE}_{BA}$	B-to-A output enable input (active Low)
16	$\overline{LE}_{AB}$	A-to-B latch enable input (active Low)
27	$\overline{LE}_{BA}$	B-to-A latch enable input (active Low)
14	$\overline{E}_{AB}$	A-to-B enable input (active Low)
1	$\overline{E}_{BA}$	B-to-A enable input (active Low)
2, 3, 4, 5, 10, 11, 12, 13	A_0 - A_7	Data inputs/outputs (A side)
26, 25, 24, 23, 20, 19, 18, 17	B_0 - B_7	Data inputs/outputs (B side)
6, 7, 8, 9	GND	Ground (0V)
21, 22	V_{CC}	Positive supply voltage

FUNCTION TABLE

INPUTS				OUTPUTS	STATUS
$\overline{OE}_{XX}$	$\overline{E}_{XX}$	$\overline{LE}_{XX}$	Data		
H	X	X	X	Z	Outputs disabled
X	H	X	X	Z	Outputs disabled
L L	↑ ↑	L L	h l	Z Z	Diasabled + latched
L L	L L	↑ ↑	h l	H L	Latch + display
L L	L L	L L	H L	H L	Transparent
L	L	H	X	NC	Hold

H = High voltage level
h = High state must be present one setup time before the Low-to-High transition of $\overline{LE}_{XX}$ or $\overline{E}_{XX}$ (XX = AB or BA)
L = Low voltage level
= Low state must be present one setup time before the Low-to-High transition of $\overline{LE}_{XX}$ or $\overline{E}_{XX}$ (XX = AB or BA)
↑ = Low-to-High transition of $\overline{LE}_{XX}$ or $\overline{E}_{XX}$ (XX = AB or BA)
X = Don't care
NC = No change
Z = High-impedance state

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	74AC11543			74ACT11543			UNIT
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	DC supply voltage	3.0[1]	5.0	5.5	4.5	5.0	5.5	V
V_I	Input voltage	0		V_{CC}	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	0		V_{CC}	V
$\Delta t/\Delta v$	Input transition rise or fall rate	0		10	0		10	ns/V
T_A	Operating free-air temperature	-40		+85	-40		+85	°C

NOTE:
1. No electrical or switching characteristics are specified at $V_{CC} < 3V$. Operation between 2V and 3V is not recommended, but within that range, a device output will maintain a previously established logic state.

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	TEST CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 to+7.0	V
I_{IK} or V_I	DC input diode current[2]	$V_I < 0$	-20	mA
		$V_I > V_{CC}$	20	
	DC input voltage		-0.5 to V_{CC} +0.5	V
I_{OK} or V_O	DC output diode current[2]	$V_O < 0$	-50	mA
		$V_O > V_{CC}$	50	
	DC output voltage		-0.5 to V_{CC} +0.5	V
I_O	DC output source or sink current per output pin	V_O = 0 to V_{CC}	±50	mA
I_{CC} or I_{GND}	DC V_{CC} current		±200	mA
	DC ground current		±200	
T_{STG}	Storage temperature		-65 to 150	°C
P_{TOT}	Power dissipation per package Plastic DIP	Above 70°C:derate linearly by 8mW/K	500	mW
	Power dissipation per package Plastic surface mount (SO)	Above 70°C:derate linearly by 6mW/K	400	mW

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		V_{CC}	74AC11543				74ACT11543				UNIT
					T_A = +25°C		T_A = -40°C to +85°C		T_A = +25°C		T_A = -40°C to +85°C		
				V	Min	Max	Min	Max	Min	Max	Min	Max	
V_{IH}	High-level input voltage			3.0	2.10		2.10						V
				4.5	3.15		3.15		2.0		2.0		
				5.5	3.85		3.85		2.0		2.0		
V_{IL}	Low-level input voltage			3.0		0.90		0.90					V
				4.5		1.35		1.35		0.8		0.8	
				5.5		1.65		1.65		0.8		0.8	
V_{OH}	High-level output voltage	V_I = V_{IL} or V_{IH}	I_{OH} = -50μA	3.0	2.9		2.9						V
				4.5	4.4		4.4		4.4		4.4		
				5.5	5.4		5.4		5.4		5.4		
			I_{OH} = -4mA	3.0	2.58		2.48						
			I_{OH} = -24mA	4.5	3.94		3.8		3.94		3.8		
				5.5	4.94		4.8		4.94		4.8		
			I_{OH} = -75mA[1]	5.5			3.85				3.85		
V_{OL}	Low-level output voltage	V_I = V_{IL} or V_{IH}	I_{OL} = 50μA	3.0		0.1		0.1					V
				4.5		0.1		0.1		0.1		0.1	
				5.5		0.1		0.1		0.1		0.1	
			I_{OL} = 12mA	3.0		0.36		0.44					
			I_{OL} = 24mA	4.5		0.36		0.44		0.36		0.44	
				5.5		0.36		0.44		0.36		0.44	
			I_{OL} = 75mA[1]	5.5				1.65				1.65	
I_I	Input leakage current	V_I = V_{CC} or GND		5.5		±0.1		±1.0		±0.1		±1.0	μA
I_{OZ}	3-State output off-state current	V_I = V_{IL} or V_{IH}, V_O = V_{CC} or GND		5.5		±0.5		±5.0		±0.5		±5.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC} or GND, I_O = 0		5.5		8.0		80		8.0		80	μA
ΔI_{CC}	Supply current, TTL inputs High[2]	One input at 3.4V, other inputs at V_{CC} or GND		5.5						0.9		1.0	mA

NOTES:
1. Not more than one output should be tested at a time, and the duration of the test should not exceed 10ms.
2. This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0V or V_{CC}.

74AC/ACT11544

Octal Latched Transceiver with Dual Enable; 3-State; INV

Objective Specification

FEATURES

- **Combines '245 and '373 type functions in one chip**
- **8-bit octal transceiver with D-type latch**
- **3-State buffers**
- **Output capability: ±24 mA**
- **CMOS (AC) and TTL (ACT) voltage level inputs**
- **50Ω incident wave switching**
- **Center-pin V_{CC} and ground configuration to minimize high-speed switching noise**
- **I_{CC} category: MSI**

DESCRIPTION

The 74AC/ACT11544 high-performance CMOS devices combine very high speed and high output drive comparable to the most advanced TTL families.

The 74AC/ACT11544 Octal Latched Transceiver contains two sets of D-type latches for temporary storage of data flowing in either direction. Separate Latch Enable ($\overline{LE}_{AB}$, $\overline{LE}_{BA}$) and Output Enable ($\overline{OE}_{AB}$, $\overline{OE}_{BA}$) inputs are provided for each register to permit independent control of inputting and outputting in either direction of data flow.

GENERAL INFORMATION

SYMBOL	PARAMETER	CONDITIONS T_A = 25°C; GND = 0V; V_{CC} = 5.0V		TYPICAL AC	TYPICAL ACT	UNIT
t_{PLH}/t_{PHL}	Propagation delay $\overline{A}_n$ to $\overline{B}_n$ or $\overline{B}_n$ to $\overline{A}_n$	C_L = 50pF		5.6	7.1	ns
C_{PD}	Power dissipation capacitance per transceiver[1]	f = 1MHz;	Enabled	200	200	pF
		C_L = 50pF	Disabled	50	50	
C_{IN}	Input capacitance	V_I = 0V or V_{CC}		4.5	4.5	pF
$C_{I/O}$	I/O capacitance	$V_{I/O}$ = 0V or V_{CC}; Disabled		12	12	pF
I_{LATCH}	Latch-up current	Per Jedec JC40.2 Standard 17		500	500	mA

Note:

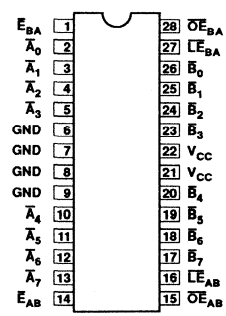
1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz, C_L = output load capacitance in pF,
   f_o = output frequency in MHz, V_{CC} = supply voltage in V,
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs

ORDERING INFORMATION

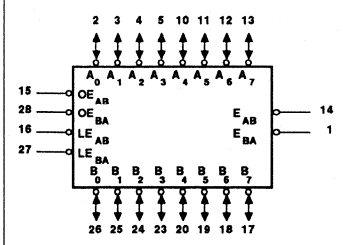
PACKAGES	TEMPERATURE RANGE	ORDER CODE
28-pin plastic DIP (300mil-wide)	-40°C to +85°C	74AC11544N 74ACT11544N
28-pin plastic SO (300mil-wide)	-40°C to +85°C	74AC11544D 74ACT11544D

PIN CONFIGURATION

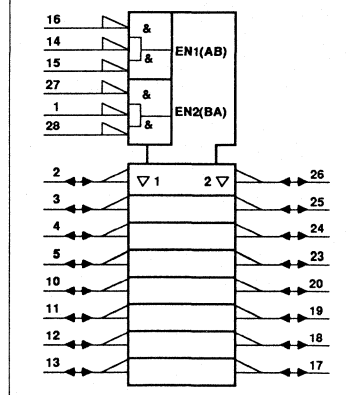
N and D Packages



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



Octal Latched Transceiver with Dual Enable; 3-State; INV

74AC/ACT11544

FUNCTIONAL DESCRIPTION

The 74AC/ACT11543 Octal Latched Transceiver contains two sets of eight D-type latches, with separate input and controls for each set. For data flow from A to B, for example, the A-to-B Enable ($\overline{E}_{AB}$) input must be Low in order to enter data from A_0 - A_7 or take data from B_0 - B_7 as indicated in the Function Table. With $\overline{E}_{AB}$ Low, a Low signal on the A-to-B Latch Enable ($\overline{LE}_{AB}$) input makes the A-to-B latches transparent; a subsequent Low-to-High transition of the $\overline{LE}_{AB}$ signal puts the A latches in the storage mode and their outputs no longer change with the A inputs. With $\overline{E}_{AB}$ and $\overline{OE}_{AB}$ both Low, the 3-State B output buffers are active and display the data present at the outputs of the A latches. Control of data flow from B to A is similar, but using the $\overline{E}_{BA}$, $\overline{LE}_{BA}$, and $\overline{OE}_{BA}$ inputs.

PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
15	$\overline{OE}_{AB}$	A-to-B output enable input (active Low)
28	$\overline{OE}_{BA}$	B-to-A output enable input (active Low)
16	$\overline{LE}_{AB}$	A-to-B latch enable input (active Low)
27	$\overline{LE}_{BA}$	B-to-A latch enable input (active Low)
14	$\overline{E}_{AB}$	A-to-B enable input (active Low)
1	$\overline{E}_{BA}$	B-to-A enable input (active Low)
2, 3, 4, 5, 10, 11, 12, 13	$\overline{A}_0$ - $\overline{A}_7$	Data inputs/outputs (A side)
26, 25, 24, 23, 20, 19, 18, 17	$\overline{B}_0$ - $\overline{B}_7$	Data inputs/outputs (B side)
6, 7, 8, 9	GND	Ground (0V)
21, 22	V_{CC}	Positive supply voltage

FUNCTION TABLE

INPUTS				OUTPUTS	STATUS
$\overline{OE}_{XX}$	$\overline{E}_{XX}$	$\overline{LE}_{XX}$	Data		
H	X	X	X	Z	Outputs disabled
X	H	X	X	Z	Outputs disabled
L L	↑ ↑	L L	h l	Z Z	Diasabled + latched
L L	L L	↑ ↑	h l	L H	Latch + display
L L	L L	L L	H L	L H	Transparent
L	L	H	X	NC	Hold

H = High voltage level
h = High state must be present one setup time before the Low-to-High transition of $\overline{LE}_{XX}$ or $\overline{E}_{XX}$ (XX = AB or BA)
L = Low voltage level
= Low state must be present one setup time before the Low-to-High transition of $\overline{LE}_{XX}$ or $\overline{E}_{XX}$ (XX = AB or BA)
↑ = Low-to-High transition of $\overline{LE}_{XX}$ or $\overline{E}_{XX}$ (XX = AB or BA)
X = Don't care
NC = No change
Z = High-impedance state

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	74AC11544			74ACT11544			UNIT
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	DC supply voltage	3.0[1]	5.0	5.5	4.5	5.0	5.5	V
V_I	Input voltage	0		V_{CC}	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	0		V_{CC}	V
$\Delta t/\Delta v$	Input transition rise or fall rate	0		10	0		10	ns/V
T_A	Operating free-air temperature	-40		+85	-40		+85	°C

NOTE:

1. No electrical or switching characteristics are specified at V_{CC} < 3V. Operation between 2V and 3V is not recommended, but within that range, a device output will maintain a previously established logic state.

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	TEST CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 to+7.0	V
I_{IK} or V_I	DC input diode current[2]	$V_I < 0$	-20	mA
		$V_I > V_{CC}$	20	
	DC input voltage		-0.5 to V_{CC} +0.5	V
I_{OK} or V_O	DC output diode current[2]	$V_O < 0$	-50	mA
		$V_O > V_{CC}$	50	
	DC output voltage		-0.5 to V_{CC} +0.5	V
I_O	DC output source or sink current per output pin	V_O = 0 to V_{CC}	±50	mA
I_{CC} or I_{GND}	DC V_{CC} current		±200	mA
	DC ground current		±200	
T_{STG}	Storage temperature		-65 to 150	°C
P_{TOT}	Power dissipation per package Plastic DIP	Above 70°C:derate linearly by 8mW/K	500	mW
	Power dissipation per package Plastic surface mount (SO)	Above 70°C:derate linearly by 6mW/K	400	mW

NOTES:

1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		V_{CC}	74AC11544				74ACT11544				UNIT
					T_A = +25°C		T_A = -40°C to +85°C		T_A = +25°C		T_A = -40°C to +85°C		
				V	Min	Max	Min	Max	Min	Max	Min	Max	
V_{IH}	High-level input voltage			3.0	2.10		2.10						V
				4.5	3.15		3.15		2.0		2.0		
				5.5	3.85		3.85		2.0		2.0		
V_{IL}	Low-level input voltage			3.0		0.90		0.90					V
				4.5		1.35		1.35		0.8		0.8	
				5.5		1.65		1.65		0.8		0.8	
V_{OH}	High-level output voltage	V_I = V_{IL} or V_{IH}	I_{OH} = -50µA	3.0	2.9		2.9						V
				4.5	4.4		4.4		4.4		4.4		
				5.5	5.4		5.4		5.4		5.4		
			I_{OH} = -4mA	3.0	2.58		2.48						
			I_{OH} = -24mA	4.5	3.94		3.8		3.94		3.8		
				5.5	4.94		4.8		4.94		4.8		
			I_{OH} = -75mA[1]	5.5			3.85				3.85		
V_{OL}	Low-level output voltage	V_I = V_{IL} or V_{IH}	I_{OL} = 50µA	3.0		0.1		0.1					V
				4.5		0.1		0.1		0.1		0.1	
				5.5		0.1		0.1		0.1		0.1	
			I_{OL} = 12mA	3.0		0.36		0.44					
			I_{OL} = 24mA	4.5		0.36		0.44		0.36		0.44	
				5.5		0.36		0.44		0.36		0.44	
			I_{OL} = 75mA[1]	5.5				1.65				1.65	
I_I	Input leakage current	V_I = V_{CC} or GND		5.5		±0.1		±1.0		±0.1		±1.0	µA
I_{OZ}	3-State output off-state current	V_I = V_{IL} or V_{IH}, V_O = V_{CC} or GND		5.5		±0.5		±5.0		±0.5		±5.0	µA
I_{CC}	Quiescent supply current	V_I = V_{CC} or GND, I_O = 0		5.5		8.0		80		8.0		80	µA
ΔI_{CC}	Supply current, TTL inputs High[2]	One input at 3.4V, other inputs at V_{CC} or GND		5.5						0.9		1.0	mA

NOTES:
1. Not more than one output should be tested at a time, and the duration of the test should not exceed 10ms.
2. This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0V or V_{CC}.

74AC/ACT11579

8-Bit Binary Up/Down Counter w/ Common I/O Pins; Synchronous and Asynchronous Reset; 3-State

Objective Specification

FEATURES

- **Multiplexed 3-State I/O ports for bus-oriented applications**
- **Built-in cascading carry capability**
- **Glitchless Terminal Count output**
- **Fully synchronous operation**
- **U/$\overline{D}$ pin to control direction of counting**
- **Separate pins for Master Reset and Synchronous Reset**
- **Output capability: ±24mA**
- **CMOS (AC) and TTL (ACT) voltage level inputs**
- **50Ω incident wave switching**
- **Center-pin V_{CC} and ground configuration to minimize high-speed switching noise**
- **I_{CC} category: MSI**

DESCRIPTION

The 74AC/ACT11579 high-performance CMOS devices combine very high speed and high output drive comparable to the most advanced TTL families.

The AC/ACT11579 is a fully synchronous 8-stage up/down counter with multiplexed 3-State I/O ports for bus-oriented applica-

GENERAL INFORMATION

SYMBOL	PARAMETER	CONDITIONS T_A = 25°C; GND = 0V; V_{CC} = 5.0V		TYPICAL AC	TYPICAL ACT	UNIT
t_{PLH}/ t_{PHL}	Propagation delay CP to I/O_n	C_L = 50pF		6.2	7.8	ns
C_{PD}	Power dissipation capacitance per flip-flop[1]	f = 1MHz;	Enabled	230	210	pF
		C_L = 50pF	Disabled	40	40	
C_{IN}	Input capacitance	V_I = 0V or V_{CC}		4.0	4.0	pF
C_O	Output capacitance	V_{IO} = 0V or V_{CC}; Disabled		10	10	pF
C_{IO}	I/O capacitance	V_{IO} = 0V or V_{CC}; Disabled		12	12	pF
I_{LATCH}	Latch-up current	Per Jedec JC40.2 Standard 17		500	500	mA
f_{MAX}	Maximum clock frequency, CP to I/O_n	C_L = 50pF		160	150	MHz

Note:

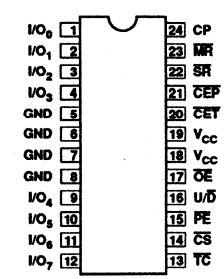
1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_I + \Sigma (C_L \times V_{CC}^2 \times f_O)$ where:
   f_I = input frequency in MHz, C_L = output load capacitance in pF,
   f_O = output frequency in MHz, V_{CC} = supply voltage in V,
   $\Sigma (C_L \times V_{CC}^2 \times f_O)$ = sum of outputs

ORDERING INFORMATION

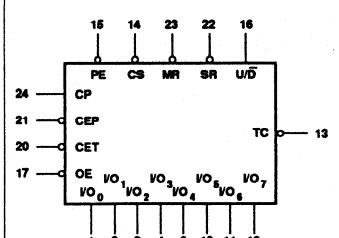
PACKAGES	TEMPERATURE RANGE	ORDER CODE
24-pin plastic DIP (300mil-wide)	-40°C to +85°C	74AC11579N 74ACT11579N
24-pin plastic SO (300mil-wide)	-40°C to +85°C	74AC11579D 74ACT11579D

PIN CONFIGURATION

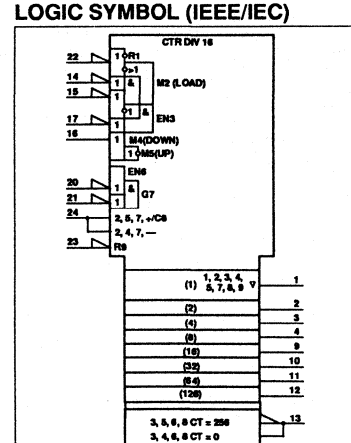
N and D Packages



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



8-Bit Binary Up/Down Counter w/ Common I/O Pins; Synchronous and Asynchronous Reset; 3-State

tions. It features a preset capability for programmable operation, carry look-ahead for easy cascading and a U/$\overline{D}$ input to control the direction of counting. All state changes, except for the case of asynchronous reset, are initiated by the rising edge of the clock.

The AC/ACT11579 uses edge-triggered D-type flip-flops and has no constraints on changing the control or data input signals in either state of the clock. The only requirement is that the various inputs attain the desired state at least a setup time before the rising edge of the clock and remain valid for the recommended hold time thereafter. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other. This mode of operation eliminates the output spikes normally associated with ripple counters. A buffered clock input triggers all flip-flops on the Low-to-High transition. Flip-flop contents appear on the I/O lines only when $\overline{OE}$ and $\overline{CS}$ are Low and $\overline{PE}$ is High.

Both synchronous and asynchronous master resets are provided. All flip-flops are reset whenever $\overline{MR}$ is Low. If $\overline{MR}$ is High and $\overline{SR}$ is Low, all flip-flops are reset on the next Low-to-High transition of the clock.

The counter is fully programmable; that is, the flip-flops may be preset to either level. Presetting is synchronous with the clock and takes precedence over other functions when $\overline{MR}$ and $\overline{SR}$ are High. Both $\overline{PE}$ and $\overline{CS}$ must be Low to preset the counter.

The direction of counting is controlled by the U/$\overline{D}$ input; a High will cause the count to increase, a low will cause the count to decrease.

The carry look-ahead circuitry provides for cascading counters for n-bit synchronous applications without additional components. Instrumental in accomplishing this are tow Count Enable inputs ($\overline{CET}$ and $\overline{CEP}$) and a Terminal Count ($\overline{TC}$) output. Both count enable inputs must be low to count. The $\overline{CET}$ input is fed forward to enable the $\overline{TC}$ output. The $\overline{TC}$ output thus enabled will produce a Low output pulse with a duration approximately equal to the High or Low level portion of the Q_0 output depending on the state of U/$\overline{D}$. This will occur when the counter is at zero when counting down or 15 when counting up.

The Terminal Count ($\overline{TC}$) output is normally High and goes Low when a counter reaches zero in the Count Down mode or reaches 15 in the Count Up mode, provided that $\overline{CET}$ is Low. The $\overline{TC}$ output state is not a function of the Count Enable Parallel ($\overline{CEP}$) input level. The $\overline{TC}$ signal is derived by decoding the D-input signals of the counter flip-flops and using this decoded signal as the D-input driving the $\overline{TC}$ output. Use of this configuration gives a $\overline{TC}$ output which is free of decoding spikes. The possibility exists that on pwer-up that the $\overline{TC}$ output may not give a true indication of the state of the counter (i.e., $\overline{TC}$ may be Low while the counter is not at terminal count or High when it is at terminal count.) Should this occur, $\overline{TC}$ will always go to a correct state on the first Low-to-High transition of the clock.

PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
15	$\overline{PE}$	Parallel enable input
16	U/$\overline{D}$	Up-Down count control input
23	$\overline{MR}$	Master reset input (active-Low)
22	$\overline{SR}$	Synchronous reset input (active-Low)
21	$\overline{CEP}$	Count enable parallel input (active-Low)
20	$\overline{CET}$	Count enable trickle input (active-Low)
14	$\overline{CS}$	Chip select input (active-Low)
17	$\overline{OE}$	Output enable input (active-Low)
24	CP	Clock input
13	$\overline{TC}$	Terminal count output (active-Low)
1, 2, 3, 4, 9, 10, 11, 12	I/O_0 -I/O_7	Data inputs/outputs
5, 6, 7, 8	GND	Ground (0V)
18, 19	V_{CC}	Positive supply voltage

FUNCTION TABLE

$\overline{MR}$	$\overline{SR}$	$\overline{CS}$	$\overline{PE}$	$\overline{CEP}$	$\overline{CET}$	U/$\overline{D}$	$\overline{OE}$	CP	FUNCTION
X	X	H	X	X	X	X	X	X	I/O_0 to I/O_7 in Hi Z (PE disabled)
X	X	L	H	X	X	X	H	X	I/O_0 to I/O_7 in Hi Z
X	X	L	H	X	X	X	L	X	Flip-flop outputs appear on I/O lines
L	X	X	X	X	X	X	X	X	Asynchronous reset for all flip-flops
H	L	X	X	X	X	X	X	↑	Synchronous reset for all flip-flops
H	H	L	L	X	X	X	X	↑	Parallel load all flip-flops
H	H	(not LL)	H	X	X	X	↑		Hold
H	H	(not LL)	X	H	X	X	↑		Hold ($\overline{TC}$ held High)
H	H	(not LL)	L	L	H	X	↑		Count up
H	H	(not LL)	L	L	L	X	↑		Count down

H = High voltage levle
L = Low voltage levels
X = Don't Care
U = Low-to-High clock transition
(not LL) = $\overline{CS}$ and $\overline{PE}$ should never both be at the Low voltage level at the same time

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	74AC11579			74ACT11579			UNIT
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	DC supply voltage	3.0[1]	5.0	5.5	4.5	5.0	5.5	V
V_I	Input voltage	0		V_{CC}	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	0		V_{CC}	V
$\Delta t/\Delta v$	Input transition rise or fall rate	0		10	0		10	ns/V
T_A	Operating free-air temperature	-40		+85	-40		+85	°C

NOTE:

1. No electrical or switching characteristics are specified at $V_{CC} < 3V$. Operation between 2V and 3V is not recommended, but within that range, a device output will maintain a previously established logic state.

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	TEST CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 to+7.0	V
I_{IK} or V_I	DC input diode current[2]	$V_I < 0$	-20	mA
		$V_I > V_{CC}$	20	
	DC input voltage		-0.5 to V_{CC} +0.5	V
I_{OK} or V_O	DC output diode current[2]	$V_O < 0$	-50	mA
		$V_O > V_{CC}$	50	
	DC output voltage		-0.5 to V_{CC} +0.5	V
I_O	DC output source or sink current per output pin	V_O = 0 to V_{CC}	±50	mA
I_{CC} or I_{GND}	DC V_{CC} current		±225	mA
	DC ground current		±225	
T_{STG}	Storage temperature		-65 to 150	°C
P_{TOT}	Power dissipation per package Plastic DIP	Above 70°C:derate linearly by 8mW/K	500	mW
	Power dissipation per package Plastic surface mount (SO)	Above 70°C:derate linearly by 6mW/K	400	mW

NOTES:

1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		V_{CC}	74AC11579				74ACT11579				UNIT
					T_A = +25°C		T_A = -40°C to +85°C		T_A = +25°C		T_A = -40°C to +85°C		
				V	Min	Max	Min	Max	Min	Max	Min	Max	
V_{IH}	High-level input voltage			3.0	2.10		2.10						V
				4.5	3.15		3.15		2.0		2.0		
				5.5	3.85		3.85		2.0		2.0		
V_{IL}	Low-level input voltage			3.0		0.90		0.90					V
				4.5		1.35		1.35		0.8		0.8	
				5.5		1.65		1.65		0.8		0.8	
V_{OH}	High-level output voltage	V_I = V_{IL} or V_{IH}	I_{OH} = -50µA	3.0	2.9		2.9						V
				4.5	4.4		4.4		4.4		4.4		
				5.5	5.4		5.4		5.4		5.4		
			I_{OH} = -4mA	3.0	2.58		2.48						
			I_{OH} = -24mA	4.5	3.94		3.8		3.94		3.8		
				5.5	4.94		4.8		4.94		4.8		
			I_{OH} = -75mA[1]	5.5			3.85				3.85		
V_{OL}	Low-level output voltage	V_I = V_{IL} or V_{IH}	I_{OL} = 50µA	3.0		0.1		0.1					V
				4.5		0.1		0.1		0.1		0.1	
				5.5		0.1		0.1		0.1		0.1	
			I_{OL} = 12mA	3.0		0.36		0.44					
			I_{OL} = 24mA	4.5		0.36		0.44		0.36		0.44	
				5.5		0.36		0.44		0.36		0.44	
			I_{OL} = 75mA[1]	5.5				1.65				1.65	
I_I	Input leakage current	V_I = V_{CC} or GND		5.5		±0.1		±1.0		±0.1		±1.0	µA
I_{OZ}	3-State output off-state current	V_I = V_{IL} or V_{IH}, V_O = V_{CC} or GND		5.5		±0.5		±5.0		±0.5		±5.0	µA
I_{CC}	Quiescent supply current	V_I = V_{CC} or GND, I_O = 0		5.5		8.0		80		8.0		80	µA
ΔI_{CC}	Supply current, TTL inputs High[2]	One input at 3.4V, other inputs at V_{CC} or GND		5.5						0.9		1.0	mA

NOTES:
1. Not more than one output should be tested at a time, and the duration of the test should not exceed 10ms.
2. This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0V or V_{CC}.

74AC/ACT11620

Octal Transceiver with Dual Enable; 3-State; INV

Objective Specification

FEATURES

- **Octal bidirectional bus interface**
- **3-State buffers**
- **Inverting version of '623**
- **Output capability: ±24 mA**
- **CMOS (AC) and TTL (ACT) voltage level inputs**
- **50Ω incident wave switching**
- **Center-pin V_{CC} and ground configuration to minimize high-speed switching noise**
- **I_{CC} category: MSI**

DESCRIPTION

The 74AC/ACT11620 high-performance CMOS devices combine very high speed and high output drive comparable to the most advanced TTL families.

The 74AC/ACT11620 device is an octal transceiver featuring inverting 3-State bus compatible outputs in both send and receive directions.

This octal bus transceivers are designed for asynchronous two-way communication between data buses. The control function implementation allows for maximum flexibility in timing.

GENERAL INFORMATION

SYMBOL	PARAMETER	CONDITIONS T_A = 25°C; GND = 0V; V_{CC} = 5.0V		TYPICAL AC	TYPICAL ACT	UNIT
t_{PLH}/ t_{PHL}	Propagation delay A_n to B_n, or B_n to A_n	C_L = 50pF		5.0	5.8	ns
C_{PD}	Power dissipation capacitance per transceiver[1]	f = 1MHz; C_L = 50pF	Enabled	54	54	pF
			Disabled	11	11	
C_{IN}	Input capacitance	V_I = 0V or V_{CC}		4.0	4.0	pF
C_{IO}	I/O capacitance	$V_{I/O}$ = 0V or V_{CC}; Disabled		12	12	pF
I_{LATCH}	Latch-up current	Per Jedec JC40.2 Standard 17		500	500	mA

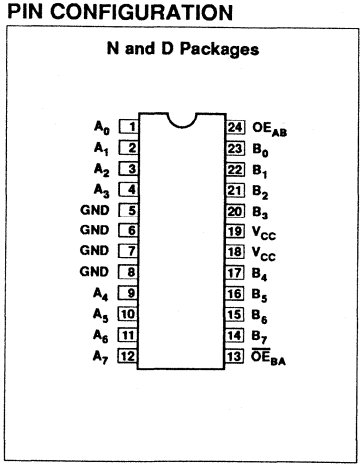
Note:

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz, C_L = output load capacitance in pF,
   f_o = output frequency in MHz, V_{CC} = supply voltage in V,
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs

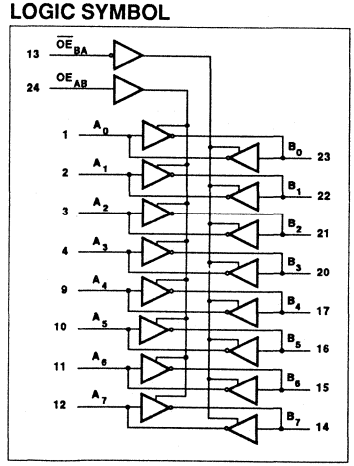
ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE
24-pin plastic DIP (300mil-wide)	-40°C to +85°C	74AC11620N 74ACT11620N
24-pin plastic SO (300mil-wide)	-40°C to +85°C	74AC11620D 74ACT11620D

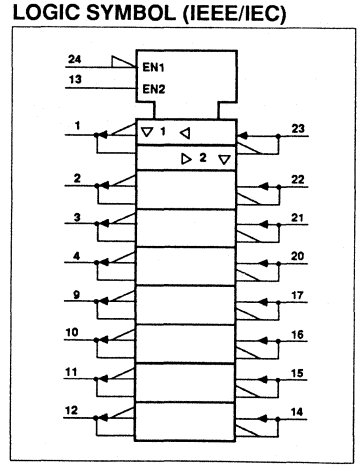
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



This device allows data transmission from the A bus to the B bus or from the B bus to the A bus, depending upon the logic levels at the Enable inputs (OE_{AB}, $\overline{OE}_{BA}$). The Enable inputs can be used to disable the device so that the buses are effectively isolated.

The dual-enable configuration gives this transceiver the capability to store data by the simultaneous enabling of OE_{AB} and $\overline{OE}_{BA}$. Each output reinforces its input in this transceiver configuration. Thus, when both control inputs are enabled and all other data sources to the two sets of the bus lines are at high impedance, both sets of bus lines (16 in all) will remain at their last states.

PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
24	OE_{AB}	3-state output enable (active High)
13	$\overline{OE}_{BA}$	3-state output enable (active Low)
1, 2,3, 4, 9, 10, 11, 12	A_0 - A_7	Data inputs/outputs (A side)
23, 22, 21, 20, 17, 16, 15, 14	B_0 - B_7	Data inputs/outputs (B side)
5, 6, 7, 8	GND	Ground (0V)
18, 19	V_{CC}	Positive supply voltage

FUNCTION TABLE

ENABLE INPUTS		OPERATION
OE_{AB}	$\overline{OE}_{BA}$	
L	L	$\overline{B}$ data to A bus
H	H	$\overline{A}$ data to B bus
L	H	Z
H	L	$\overline{B}$ data to A bus, $\overline{A}$ data to B bus

H = High voltage level
L = Low volatge level
Z = High-impedance (OFF) state

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	74AC11620			74ACT11620			UNIT
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	DC supply voltage	3.0[1]	5.0	5.5	4.5	5.0	5.5	V
V_I	Input voltage	0		V_{CC}	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	0		V_{CC}	V
$\Delta t/\Delta v$	Input transition rise or fall rate	0		10	0		10	ns/V
T_A	Operating free-air temperature	-40		+85	-40		+85	°C

NOTE:
1. No electrical or switching characteristics are specified at V_{CC} < 3V. Operation between 2V and 3V is not recommended, but within that range, a device output will maintain a previously established logic state.

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	TEST CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 to+7.0	V
I_{IK} or V_I	DC input diode current[2]	$V_I < 0$	-20	mA
		$V_I > V_{CC}$	20	
	DC input voltage		-0.5 to V_{CC} +0.5	V
I_{OK} or V_O	DC output diode current[2]	$V_O < 0$	-50	mA
		$V_O > V_{CC}$	50	
	DC output voltage		-0.5 to V_{CC} +0.5	V
I_O	DC output source or sink current per output pin	V_O = 0 to V_{CC}	±50	mA
I_{CC} or I_{GND}	DC V_{CC} current		±200	mA
	DC ground current		±200	
T_{STG}	Storage temperature		-65 to 150	°C
P_{TOT}	Power dissipation per package Plastic DIP	Above 70°C:derate linearly by 8mW/K	500	mW
	Power dissipation per package Plastic surface mount (SO)	Above 70°C:derate linearly by 6mW/K	400	mW

NOTES:

1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		V_{CC}	74AC11620				74ACT11620				UNIT
					T_A = +25°C		T_A = -40°C to +85°C		T_A = +25°C		T_A = -40°C to +85°C		
				V	Min	Max	Min	Max	Min	Max	Min	Max	
V_{IH}	High-level input voltage			3.0	2.10		2.10						V
				4.5	3.15		3.15		2.0		2.0		
				5.5	3.85		3.85		2.0		2.0		
V_{IL}	Low-level input voltage			3.0		0.90		0.90					V
				4.5		1.35		1.35		0.8		0.8	
				5.5		1.65		1.65		0.8		0.8	
V_{OH}	High-level output voltage	V_I = V_{IL} or V_{IH}	I_{OH} = -50μA	3.0	2.9		2.9						V
				4.5	4.4		4.4		4.4		4.4		
				5.5	5.4		5.4		5.4		5.4		
			I_{OH} = -4mA	3.0	2.58		2.48						
			I_{OH} = -24mA	4.5	3.94		3.8		3.94		3.8		
				5.5	4.94		4.8		4.94		4.8		
			I_{OH} = -75mA[1]	5.5			3.85				3.85		
V_{OL}	Low-level output voltage	V_I = V_{IL} or V_{IH}	I_{OL} = 50μA	3.0		0.1		0.1					V
				4.5		0.1		0.1		0.1		0.1	
				5.5		0.1		0.1		0.1		0.1	
			I_{OL} = 12mA	3.0		0.36		0.44					
			I_{OL} = 24mA	4.5		0.36		0.44		0.36		0.44	
				5.5		0.36		0.44		0.36		0.44	
			I_{OL} = 75mA[1]	5.5				1.65				1.65	
I_I	Input leakage current	V_I = V_{CC} or GND		5.5		±0.1		±1.0		±0.1		±1.0	μA
I_{OZ}	3-State output off-state current	V_I = V_{IL} or V_{IH}, V_O = V_{CC} or GND		5.5		±0.5		±5.0		±0.5		±5.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC} or GND, I_O = 0		5.5		8.0		80		8.0		80	μA
ΔI_{CC}	Supply current, TTL inputs High[2]	One input at 3.4V, other inputs at V_{CC} or GND		5.5						0.9		1.0	mA

NOTES:
1. Not more than one output should be tested at a time, and the duration of the test should not exceed 10ms.
2. This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0V or V_{CC}.

74AC/ACT11623

Octal Transceiver with Dual Enable; 3-State

Objective Specification

FEATURES

- **Octal bidirectional bus interface**
- **3-State buffers**
- **Non-inverting version of '620**
- **Output capability: ±24 mA**
- **CMOS (AC) and TTL (ACT) voltage level inputs**
- **50Ω incident wave switching**
- **Center-pin V_{CC} and ground configuration to minimize high-speed switching noise**
- **I_{CC} category: MSI**

DESCRIPTION

The 74AC/ACT11623 high-performance CMOS devices combine very high speed and high output drive comparable to the most advanced TTL families.

The 74AC/ACT11623 device is an octal transceiver featuring non-inverting 3-State bus compatible outputs in both send and receive directions.

This octal bus transceivers are designed for asynchronous two-way communication between data buses. The control function implementation allows for maximum flexibility in timing.

GENERAL INFORMATION

SYMBOL	PARAMETER	CONDITIONS T_A = 25°C; GND = 0V; V_{CC} = 5.0V		TYPICAL AC	TYPICAL ACT	UNIT
t_{PLH}/t_{PHL}	Propagation delay A_n to B_n, or B_n to A_n	C_L = 50pF		4.8	5.8	ns
C_{PD}	Power dissipation capacitance per transceiver[1]	f = 1MHz; C_L = 50pF	Enabled	49	41	pF
			Disabled	9	8	
C_{IN}	Input capacitance	V_I = 0V or V_{CC}		4.0	4.0	pF
C_{IO}	I/O capacitance	$V_{I/O}$ = 0V or V_{CC}; Disabled		12	12	pF
I_{LATCH}	Latch-up current	Per Jedec JC40.2 Standard 17		500	500	mA

Note:

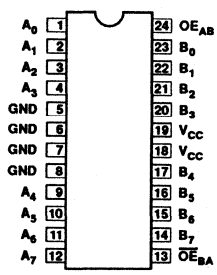
1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_I + \Sigma (C_L \times V_{CC}^2 \times f_O)$ where:
   f_I = input frequency in MHz, C_L = output load capacitance in pF,
   f_O = output frequency in MHz, V_{CC} = supply voltage in V,
   $\Sigma (C_L \times V_{CC}^2 \times f_O)$ = sum of outputs

ORDERING INFORMATION

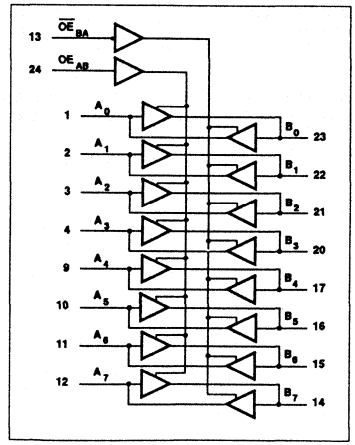
PACKAGES	TEMPERATURE RANGE	ORDER CODE
24-pin plastic DIP (300mil-wide)	-40°C to +85°C	74AC11623N 74ACT11623N
24-pin plastic SO (300mil-wide)	-40°C to +85°C	74AC11623D 74ACT11623D

PIN CONFIGURATION

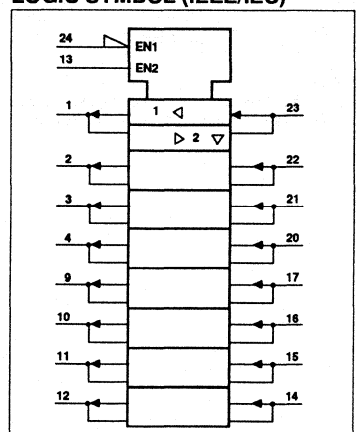
N and D Packages



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



May 12, 1989

This device allows data transmission from the A bus to the B bus or from the B bus to the A bus, depending upon the logic levels at the Enable inputs (OE_{AB}, $\overline{OE}_{BA}$). The Enable inputs can be used to disable the device so that the buses are effectively isolated.

The dual-enable configuration gives this transceiver the capability to store data by the simultaneous enabling of OE_{AB} and $\overline{OE}_{BA}$. Each output reinforces its input in this transceiver configuration. Thus, when both control inputs are enabled and all other data sources to the two sets of the bus lines are at high impedance, both sets of bus lines (16 in all) will remain at their last states.

PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
24	OE_{AB}	3-state output enable (active High)
13	$\overline{OE}_{BA}$	3-state output enable (active Low)
1, 2,3, 4, 9, 10, 11, 12	$A_0 - A_7$	Data inputs/outputs (A side)
23, 22, 21, 20, 17, 16, 15, 14	$B_0 - B_7$	Data inputs/outputs (B side)
5, 6, 7, 8	GND	Ground (0V)
18, 19	V_{CC}	Positive supply voltage

FUNCTION TABLE

ENABLE INPUTS		OPERATION
OE_{AB}	$\overline{OE}_{BA}$	
L	L	B data to A bus
H	H	A data to B bus
L	H	Z
H	L	B data to A bus, A data to B bus

H = High voltage level
L = Low volatge level
Z = High-impedance (OFF) state

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	74AC11623			74ACT11623			UNIT
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	DC supply voltage	3.0[1]	5.0	5.5	4.5	5.0	5.5	V
V_I	Input voltage	0		V_{CC}	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	0		V_{CC}	V
$\Delta t/\Delta v$	Input transition rise or fall rate	0		10	0		10	ns/V
T_A	Operating free-air temperature	-40		+85	-40		+85	°C

NOTE:
1. No electrical or switching characteristics are specified at V_{CC} < 3V. Operation between 2V and 3V is not recommended, but within that range, a device output will maintain a previously established logic state.

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	TEST CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 to+7.0	V
I_{IK} or V_I	DC input diode current[2]	$V_I < 0$	-20	mA
		$V_I > V_{CC}$	20	
	DC input voltage		-0.5 to V_{CC} +0.5	V
I_{OK} or V_O	DC output diode current[2]	$V_O < 0$	-50	mA
		$V_O > V_{CC}$	50	
	DC output voltage		-0.5 to V_{CC} +0.5	V
I_O	DC output source or sink current per output pin	V_O = 0 to V_{CC}	±50	mA
I_{CC} or I_{GND}	DC V_{CC} current		±200	mA
	DC ground current		±200	
T_{STG}	Storage temperature		-65 to 150	°C
P_{TOT}	Power dissipation per package Plastic DIP	Above 70°C:derate linearly by 8mW/K	500	mW
	Power dissipation per package Plastic surface mount (SO)	Above 70°C:derate linearly by 6mW/K	400	mW

NOTES:

1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		V_{CC}	74AC11623				74ACT11623				UNIT
					T_A = +25°C		T_A = -40°C to +85°C		T_A = +25°C		T_A = -40°C to +85°C		
				V	Min	Max	Min	Max	Min	Max	Min	Max	
V_{IH}	High-level input voltage			3.0	2.10		2.10						V
				4.5	3.15		3.15		2.0		2.0		
				5.5	3.85		3.85		2.0		2.0		
V_{IL}	Low-level input voltage			3.0		0.90		0.90					V
				4.5		1.35		1.35		0.8		0.8	
				5.5		1.65		1.65		0.8		0.8	
V_{OH}	High-level output voltage	V_I = V_{IL} or V_{IH}	I_{OH} = -50μA	3.0	2.9		2.9						V
				4.5	4.4		4.4		4.4		4.4		
				5.5	5.4		5.4		5.4		5.4		
			I_{OH} = -4mA	3.0	2.58		2.48						
			I_{OH} = -24mA	4.5	3.94		3.8		3.94		3.8		
				5.5	4.94		4.8		4.94		4.8		
			I_{OH} = -75mA[1]	5.5			3.85				3.85		
V_{OL}	Low-level output voltage	V_I = V_{IL} or V_{IH}	I_{OL} = 50μA	3.0		0.1		0.1					V
				4.5		0.1		0.1		0.1		0.1	
				5.5		0.1		0.1		0.1		0.1	
			I_{OL} = 12mA	3.0		0.36		0.44					
			I_{OL} = 24mA	4.5		0.36		0.44		0.36		0.44	
				5.5		0.36		0.44		0.36		0.44	
			I_{OL} = 75mA[1]	5.5				1.65				1.65	
I_I	Input leakage current	V_I = V_{CC} or GND		5.5		±0.1		±1.0		±0.1		±1.0	μA
I_{OZ}	3-State output off-state current	V_I = V_{IL} or V_{IH}, V_O = V_{CC} or GND		5.5		±0.5		±5.0		±0.5		±5.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC} or GND, I_O = 0		5.5		8.0		80		8.0		80	μA
ΔI_{CC}	Supply current, TTL inputs High[2]	One input at 3.4V, other inputs at V_{CC} or GND		5.5						0.9		1.0	mA

NOTES:
1. Not more than one output should be tested at a time, and the duration of the test should not exceed 10ms.
2. This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0V or V_{CC}.

74AC/ACT11640

Octal Transceiver w/Direction Pin; 3-State; INV

Product Specification

FEATURES

- **Octal bidirectional bus interface**
- **3-State buffers**
- **Inverting version of '245**
- **Output capability: ±24 mA**
- **CMOS (AC) and TTL (ACT) voltage level inputs**
- **50Ω incident wave switching**
- **Center-pin V_{CC} and ground configuration to minimize high-speed switching noise**
- **I_{CC} category: MSI**

DESCRIPTION

The 74AC/ACT11640 high-performance CMOS devices combine very high speed and high output drive comparable to the most advanced TTL families.

The 74AC/ACT11640 device is an octal transceiver featuring inverting 3-State bus compatible outputs in both send and receive directions. The control function implementation minimizes external timing requirements. The device features an Output Enable ($\overline{OE}$) input for easy cascading and a Direction (DIR) input for direction control.

GENERAL INFORMATION

SYMBOL	PARAMETER	CONDITIONS T_A = 25°C; GND = 0V; V_{CC} = 5.0V		TYPICAL AC	TYPICAL ACT	UNIT
t_{PLH}/t_{PHL}	Propagation delay A_n to B_n, or B_n to A_n	C_L = 50pF		4.9	6.0	ns
C_{PD}	Power dissipation capacitance per transceiver[1]	f = 1MHz; C_L = 50pF	Enabled	45	47	pF
			Disabled	12	12	
C_{IN}	Input capacitance	V_I = 0V or V_{CC}		4.0	4.0	pF
C_{IO}	I/O capacitance	$V_{I/O}$ = 0V or V_{CC}; Disabled		12	12	pF
I_{LATCH}	Latch-up current	Per Jedec JC40.2 Standard 17		500	500	mA

Note:

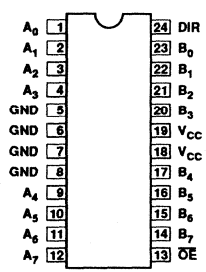
1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_I + \Sigma (C_L \times V_{CC}^2 \times f_O)$ where:
   f_I = input frequency in MHz, C_L = output load capacitance in pF,
   f_O = output frequency in MHz, V_{CC} = supply voltage in V,
   $\Sigma (C_L \times V_{CC}^2 \times f_O)$ = sum of outputs

ORDERING INFORMATION

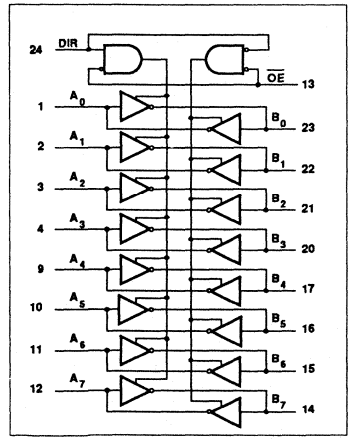
PACKAGES	TEMPERATURE RANGE	ORDER CODE
24-pin plastic DIP (300mil-wide)	-40°C to +85°C	74AC11640N 74ACT11640N
24-pin plastic SO (300mil-wide)	-40°C to +85°C	74AC11640D 74ACT11640D

PIN CONFIGURATION

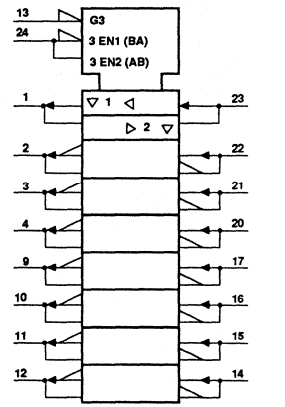
N and D Packages



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
24	DIR	Direction control input
1, 2, 3, 4, 9, 10, 11, 12	A_0 - A_7	Data inputs/outputs (A side)
23, 22, 21, 20, 17, 16, 15, 14	B_0 - B_7	Data inputs/outputs (B side)
13	$\overline{OE}$	Output enable
5, 6, 7, 8	GND	Ground (0V)
18, 19	V_{CC}	Positive supply voltage

FUNCTION TABLE

INPUTS		INPUTS/OUTPUTS	
$\overline{OE}$	DIR	A_n	B_n
L	L	A = $\overline{B}$	inputs
L	H	inputs	B = $\overline{A}$
H	X	Z	Z

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	74AC11640			74ACT11640			UNIT
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	DC supply voltage	3.0[1]	5.0	5.5	4.5	5.0	5.5	V
V_I	Input voltage	0		V_{CC}	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	0		V_{CC}	V
$\Delta t/\Delta v$	Input transition rise or fall rate	0		10	0		10	ns/V
T_A	Operating free-air temperature	-40		+85	-40		+85	°C

NOTE:

1. No electrical or switching characteristics are specified at V_{CC} < 3V. Operation between 2V and 3V is not recommended, but within that range, a device output will maintain a previously established logic state.

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	TEST CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 to+7.0	V
I_{IK} or V_I	DC input diode current[2]	V_I < 0	-20	mA
		V_I > V_{CC}	20	
	DC input voltage		-0.5 to V_{CC} +0.5	V
I_{OK} or V_O	DC output diode current[2]	V_O < 0	-50	mA
		V_O > V_{CC}	50	
	DC output voltage		-0.5 to V_{CC} +0.5	V
I_O	DC output source or sink current per output pin	V_O = 0 to V_{CC}	±50	mA
I_{CC} or I_{GND}	DC V_{CC} current		±200	mA
	DC ground current		±200	
T_{STG}	Storage temperature		-65 to 150	°C
P_{TOT}	Power dissipation per package Plastic DIP	Above 70°C:derate linearly by 8mW/K	500	mW
	Power dissipation per package Plastic surface mount (SO)	Above 70°C:derate linearly by 6mW/K	400	mW

NOTES:

1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		V_{CC}	74AC11640				74ACT11640				UNIT
					T_A = +25°C		T_A = -40°C to +85°C		T_A = +25°C		T_A = -40°C to +85°C		
				V	Min	Max	Min	Max	Min	Max	Min	Max	
V_{IH}	High-level input voltage			3.0	2.10		2.10						V
				4.5	3.15		3.15		2.0		2.0		
				5.5	3.85		3.85		2.0		2.0		
V_{IL}	Low-level input voltage			3.0		0.90		0.90					V
				4.5		1.35		1.35		0.8		0.8	
				5.5		1.65		1.65		0.8		0.8	
V_{OH}	High-level output voltage	V_I = V_{IL} or V_{IH}	I_{OH} = -50μA	3.0	2.9		2.9						V
				4.5	4.4		4.4		4.4		4.4		
				5.5	5.4		5.4		5.4		5.4		
			I_{OH} = -4mA	3.0	2.58		2.48						
			I_{OH} = -24mA	4.5	3.94		3.8		3.94		3.8		
				5.5	4.94		4.8		4.94		4.8		
			I_{OH} = -75mA[1]	5.5			3.85				3.85		
V_{OL}	Low-level output voltage	V_I = V_{IL} or V_{IH}	I_{OL} = 50μA	3.0		0.1		0.1					V
				4.5		0.1		0.1		0.1		0.1	
				5.5		0.1		0.1		0.1		0.1	
			I_{OL} = 12mA	3.0		0.36		0.44					
			I_{OL} = 24mA	4.5		0.36		0.44		0.36		0.44	
				5.5		0.36		0.44		0.36		0.44	
			I_{OL} = 75mA[1]	5.5				1.65				1.65	
I_I	Input leakage current	V_I = V_{CC} or GND		5.5		±0.1		±1.0		±0.1		±1.0	μA
I_{OZ}	3-State output off-state current	V_I = V_{IL} or V_{IH}, V_O = V_{CC} or GND		5.5		±0.5		±5.0		±0.5		±5.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC} or GND, I_O = 0		5.5		8.0		80		8.0		80	μA
ΔI_{CC}	Supply current, TTL inputs High[2]	One input at 3.4V, other inputs at V_{CC} or GND		5.5						0.9		1.0	mA

NOTES:
1. Not more than one output should be tested at a time, and the duration of the test should not exceed 10ms.
2. This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0V or V_{CC}.

AC ELECTRICAL CHARACTERISTICS AT 3.3V ±0.3V

SYMBOL	PARAMETER	WAVEFORM	74AC11640					UNIT
			T_A = +25°C			T_A = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay A_n to B_n, B_n to A_n	1	1.5 1.5	7.0 6.3	10.5 9.1	1.5 1.5	12.0 10.2	ns
t_{PZH} t_{PZL}	Output enable time to High and Low level	2	1.5 1.5	8.9 8.4	12.5 12.9	1.5 1.5	14.3 14.6	ns
t_{PHZ} t_{PLZ}	Output disable time from High and Low level	2	1.5 1.5	7.9 8.6	10.0 11.0	1.5 1.5	10.8 12.0	ns

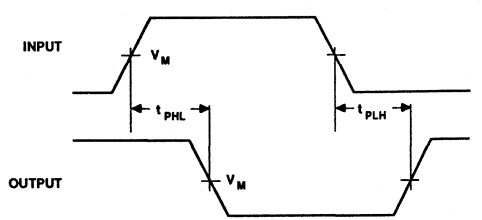
AC ELECTRICAL CHARACTERISTICS AT 5.0V ±0.5V

SYMBOL	PARAMETER	WAVEFORM	74AC11640					UNIT
			T_A = +25°C			T_A = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay A_n to B_n, B_n to A_n	1	1.5 1.5	5.1 4.6	7.7 6.9	1.5 1.5	8.8 7.8	ns
t_{PZH} t_{PZL}	Output enable time to High and Low level	2	1.5 1.5	6.5 6.1	9.4 9.4	1.5 1.5	10.6 10.6	ns
t_{PHZ} t_{PLZ}	Output disable time from High and Low level	2	1.5 1.5	6.7 7.2	8.6 9.1	1.5 1.5	9.3 9.9	ns

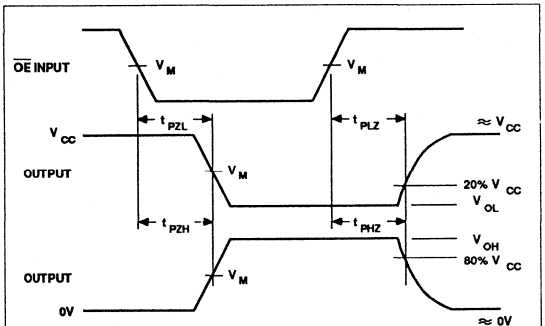
AC ELECTRICAL CHARACTERISTICS AT 5.0V ±0.5V

SYMBOL	PARAMETER	WAVEFORM	74ACT11640					UNIT
			T_A = +25°C			T_A = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay A_n to B_n, B_n to A_n	1	1.5 1.5	6.3 5.7	9.6 8.6	1.5 1.5	10.5 9.5	ns
t_{PZH} t_{PZL}	Output enable time to High and Low level	2	1.5 1.5	8.8 8.4	12.2 12.3	1.5 1.5	13.4 13.6	ns
t_{PHZ} t_{PLZ}	Output disable time from High and Low level	2	1.5 1.5	9.1 9.6	12.9 13.1	1.5 1.5	13.9 14.2	ns

AC WAVEFORMS



Waveform 1. Waveforms Showing the Input to Output Propagation Delays

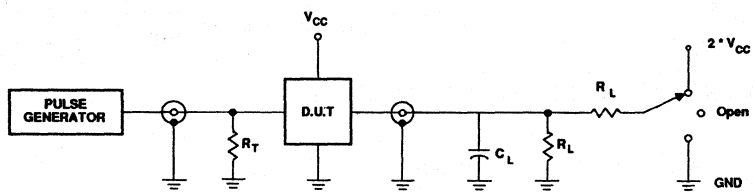


Waveform 2. Waveforms Showing the 3-State Output Enable and Disable Times

WAVEFORM CONDITIONS

	INPUTS	OUTPUTS
AC	V_{IN} = GND to V_{CC}, V_M = 50% V_{CC}	V_{OUT} = V_{OL} to V_{OH}
ACT	V_{IN} = GND to 3.0V, V_M = 1.5V	V_M = 50% V_{CC}

TEST CIRCUIT



Test Circuit

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2*VCC
t_{PHZ}/t_{PZH}	GND

SWITCH POSITION

DEFINITIONS

C_L = Load capacitance, 50pF; includes jig and probe capacitance

R_L = Load resistor, 500Ω

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators

Input pulses: PRR ≤ 10MHz

$t_r = t_f$ = 3ns

74AC/ACT11643

Octal Transceiver; 3-State; True/INV

Preliminary Specification

FEATURES

- **Octal bidirectional bus interface**
- **3-State buffers**
- **Output capability: ±24 mA**
- **CMOS (AC) and TTL (ACT) voltage level inputs**
- **50Ω incident wave switching**
- **Center-pin V_{CC} and ground configuration to minimize high-speed switching noise**
- **I_{CC} category: MSI**

DESCRIPTION

The 74AC/ACT11643 high-performance CMOS devices combine very high speed and high output drive comparable to the most advanced TTL families.

The 74AC/ACT11643 device is an octal transceiver featuring 3-State bus compatible outputs in both send and receive directions. The control function implementation minimizes external timing requirements. The device features an Output Enable ($\overline{OE}$) input for easy cascading and a Direction (DIR) input for direction control. Note that data transmitted from the A side to the B side is inverted and that data transmitted from the B side to the A side is not inverted.

GENERAL INFORMATION

SYMBOL	PARAMETER	CONDITIONS T_A = 25°C; GND = 0V; V_{CC} = 5.0V		TYPICAL AC	TYPICAL ACT	UNIT
t_{PLH}/t_{PHL}	Propagation delay A_n to B_n, or B_n to A_n	C_L = 50pF		5.2	5.7	ns
C_{PD}	Power dissipation capacitance per transceiver[1]	f = 1MHz; C_L = 50pF	Enabled	46	41	pF
			Disabled	9.0	9.0	
C_{IN}	Input capacitance	V_I = 0V or V_{CC}		4.0	4.0	pF
$C_{I/O}$	I/O capacitance	$V_{I/O}$ = 0V or V_{CC}; Disabled		12	12	pF
I_{LATCH}	Latch-up current	Per Jedec JC40.2 Standard 17		500	500	mA

Note:

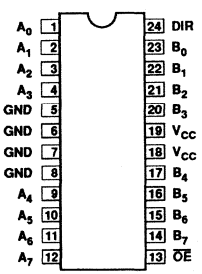
1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_I + \Sigma (C_L \times V_{CC}^2 \times f_O)$ where:
   f_I = input frequency in MHz, C_L = output load capacitance in pF,
   f_O = output frequency in MHz, V_{CC} = supply voltage in V,
   $\Sigma (C_L \times V_{CC}^2 \times f_O)$ = sum of outputs

ORDERING INFORMATION

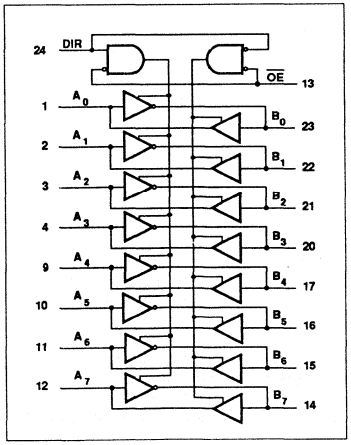
PACKAGES	TEMPERATURE RANGE	ORDER CODE
24-pin plastic DIP (300mil-wide)	-40°C to +85°C	74AC11643N 74ACT11643N
24-pin plastic SO (300mil-wide)	-40°C to +85°C	74AC11643D 74ACT11643D

PIN CONFIGURATION

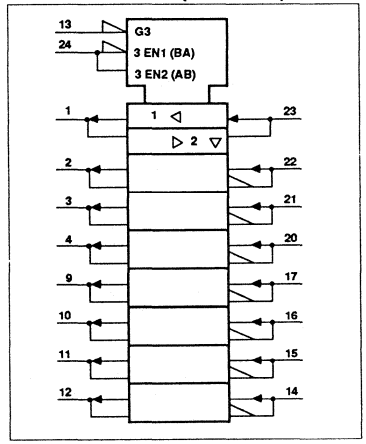
N and D Packages



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
24	DIR	Direction control input
1, 2, 3, 4, 9, 10, 11, 12	A_0 - A_7	Data inputs/outputs (A side)
23, 22, 21, 20, 17, 16, 15, 14	B_0 - B_7	Data inputs/outputs (B side)
13	$\overline{OE}$	Output enable
5, 6, 7, 8	GND	Ground (0V)
18, 19	V_{CC}	Positive supply voltage

FUNCTION TABLE

INPUTS		INPUTS/OUTPUTS	
$\overline{OE}$	DIR	A_n	B_n
L	L	A = B	inputs
L	H	inputs	B = $\overline{A}$
H	X	Z	Z

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	74AC11643			74ACT11643			UNIT
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	DC supply voltage	3.0[1]	5.0	5.5	4.5	5.0	5.5	V
V_I	Input voltage	0		V_{CC}	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	0		V_{CC}	V
$\Delta t/\Delta v$	Input transition rise or fall rate	0		10	0		10	ns/V
T_A	Operating free-air temperature	-40		+85	-40		+85	°C

NOTE:

1. No electrical or switching characteristics are specified at V_{CC} < 3V. Operation between 2V and 3V is not recommended, but within that range, a device output will maintain a previously established logic state.

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	TEST CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 to+7.0	V
I_{IK} or V_I	DC input diode current[2]	V_I < 0	-20	mA
		V_I > V_{CC}	20	
	DC input voltage		-0.5 to V_{CC} +0.5	V
I_{OK} or V_O	DC output diode current[2]	V_O < 0	-50	mA
		V_O > V_{CC}	50	
	DC output voltage		-0.5 to V_{CC} +0.5	V
I_O	DC output source or sink current per output pin	V_O = 0 to V_{CC}	±50	mA
I_{CC} or I_{GND}	DC V_{CC} current		±200	mA
	DC ground current		±200	
T_{STG}	Storage temperature		-65 to 150	°C
P_{TOT}	Power dissipation per package Plastic DIP	Above 70°C:derate linearly by 8mW/K	500	mW
	Power dissipation per package Plastic surface mount (SO)	Above 70°C:derate linearly by 6mW/K	400	mW

NOTES:

1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		V_{CC}	74AC11643				74ACT11643				UNIT
					T_A = +25°C		T_A = -40°C to +85°C		T_A = +25°C		T_A = -40°C to +85°C		
				V	Min	Max	Min	Max	Min	Max	Min	Max	
V_{IH}	High-level input voltage			3.0	2.10		2.10						V
				4.5	3.15		3.15		2.0		2.0		
				5.5	3.85		3.85		2.0		2.0		
V_{IL}	Low-level input voltage			3.0		0.90		0.90					V
				4.5		1.35		1.35		0.8		0.8	
				5.5		1.65		1.65		0.8		0.8	
V_{OH}	High-level output voltage	V_I = V_{IL} or V_{IH}	I_{OH} = -50μA	3.0	2.9		2.9						V
				4.5	4.4		4.4		4.4		4.4		
				5.5	5.4		5.4		5.4		5.4		
			I_{OH} = -4mA	3.0	2.58		2.48						
			I_{OH} = -24mA	4.5	3.94		3.8		3.94		3.8		
				5.5	4.94		4.8		4.94		4.8		
			I_{OH} = -75mA[1]	5.5			3.85				3.85		
V_{OL}	Low-level output voltage	V_I = V_{IL} or V_{IH}	I_{OL} = 50μA	3.0		0.1		0.1					V
				4.5		0.1		0.1		0.1		0.1	
				5.5		0.1		0.1		0.1		0.1	
			I_{OL} = 12mA	3.0		0.36		0.44					
			I_{OL} = 24mA	4.5		0.36		0.44		0.36		0.44	
				5.5		0.36		0.44		0.36		0.44	
			I_{OL} = 75mA[1]	5.5				1.65				1.65	
I_I	Input leakage current	V_I = V_{CC} or GND		5.5		±0.1		±1.0		±0.1		±1.0	μA
I_{OZ}	3-State output off-state current	V_I = V_{IL} or V_{IH}, V_O = V_{CC} or GND		5.5		±0.5		±5.0		±0.5		±5.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC} or GND, I_O = 0		5.5		8.0		80		8.0		80	μA
ΔI_{CC}	Supply current, TTL inputs High[2]	One input at 3.4V, other inputs at V_{CC} or GND		5.5						0.9		1.0	mA

NOTES:
1. Not more than one output should be tested at a time, and the duration of the test should not exceed 10ms.
2. This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0V or V_{CC}.

AC ELECTRICAL CHARACTERISTICS AT 3.3V ±0.3V

SYMBOL	PARAMETER	WAVEFORM	74AC11643					UNIT
			T_A = +25°C			T_A = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay A_n to B_n, B_n to A_n	1	1.5 1.5	7.4 6.6	10.1 8.7	1.5 1.5	11.3 10.0	ns
t_{PZH} t_{PZL}	Output enable time to High and Low level	2	1.5 1.5	9.4 8.9	11.8 11.4	1.5 1.5	13.3 13.0	ns
t_{PHZ} t_{PLZ}	Output disable time from High and Low level	2	1.5 1.5	8.3 8.9	10.1 10.9	1.5 1.5	10.9 12.0	ns

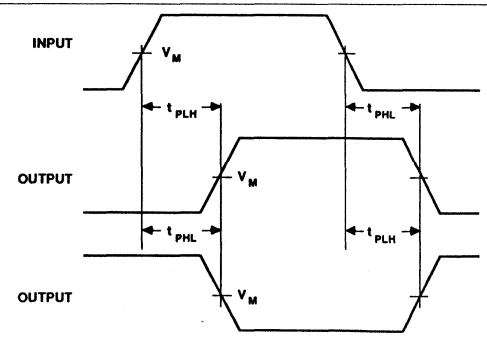
AC ELECTRICAL CHARACTERISTICS AT 5.0V ±0.5V

SYMBOL	PARAMETER	WAVEFORM	74AC11643					UNIT
			T_A = +25°C			T_A = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay A_n to B_n, B_n to A_n	1	1.5 1.5	5.4 5.0	7.7 6.8	1.5 1.5	8.6 7.9	ns
t_{PZH} t_{PZL}	Output enable time to High and Low level	2	1.5 1.5	7.0 6.6	9.2 8.7	1.5 1.5	10.4 10.0	ns
t_{PHZ} t_{PLZ}	Output disable time from High and Low level	2	1.5 1.5	7.1 7.2	8.8 9.0	1.5 1.5	9.4 9.8	ns

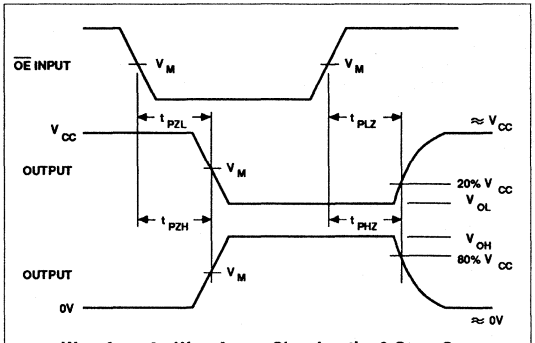
AC ELECTRICAL CHARACTERISTICS AT 5.0V ±0.5V

SYMBOL	PARAMETER	WAVEFORM	74ACT11643					UNIT
			T_A = +25°C			T_A = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay A_n to B_n, B_n to A_n	1	1.5 1.5	5.6 5.7	8.3 7.7	1.5 1.5	9.3 8.8	ns
t_{PZH} t_{PZL}	Output enable time to High and Low level	2	1.5 1.5	8.1 7.7	11.5 10.1	1.5 1.5	12.9 11.4	ns
t_{PHZ} t_{PLZ}	Output disable time from High and Low level	2	1.5 1.5	9.1 9.3	12.0 11.6	1.5 1.5	13.1 12.7	ns

AC WAVEFORMS



Waveform 1. Waveforms Showing the Input to Output Propagation Delays

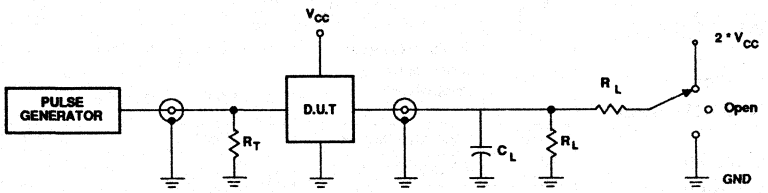


Waveform 2. Waveforms Showing the 3-State Output Enable and Disable Times

WAVEFORM CONDITIONS

	INPUTS	OUTPUTS
AC	V_{IN} = GND to V_{CC}, V_M = 50% V_{CC}	V_{OUT} = V_{OL} to V_{OH}
ACT	V_{IN} = GND to 3.0V, V_M = 1.5V	V_M = 50% V_{CC}

TEST CIRCUIT



Test Circuit

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2*VCC
t_{PHZ}/t_{PZH}	GND

SWITCH POSITION

DEFINITIONS

C_L = Load capacitance, 50pF; includes jig and probe capacitance

R_L = Load resistor, 500Ω

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators

Input pulses: PRR ≤ 10MHz

$t_r = t_f$ = 3ns

74AC/ACT11646

Octal Transceiver/Register w/Direction Pin; 3-State

Objective Specification

FEATURES

- **Octal bidirectional bus interface**
- **3-State buffers**
- **Independent registers for A and B buses**
- **Multiplexed real-time and stored data**
- **Output capability: ±24 mA**
- **CMOS (AC) and TTL (ACT) voltage level inputs**
- **50Ω incident wave switching**
- **Center-pin V_{CC} and ground configuration to minimize high-speed switching noise**
- **I_{CC} category: MSI**

DESCRIPTION

The 74AC/ACT11646 high-performance CMOS devices combine very high speed and high output drive comparable to the most advanced TTL families.

The 74AC/ACT11646 device is an octal transceiver/register featuring non-inverting 3-State bus compatible outputs in both send and receive directions, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the input bus or from internal registers. Data on the A or B bus will be clocked

GENERAL INFORMATION

SYMBOL	PARAMETER	CONDITIONS T_A = 25°C; GND = 0V; V_{CC} = 5.0V		TYPICAL AC	TYPICAL ACT	UNIT
t_{PLH}/t_{PHL}	Propagation delay A_n to B_n, or B_n to A_n	C_L = 50pF		5.9	7.3	ns
C_{PD}	Power dissipation capacitance per transceiver[1]	f = 1MHz; C_L = 50pF	Enabled	59	63	pF
			Disabled	15	14	
C_{IN}	Input capacitance	V_I = 0V or V_{CC}		4.5	4.5	pF
C_{IO}	I/O capacitance	V_O = 0V or V_{CC}; Disabled		12	12	pF
I_{LATCH}	Latch-up current	Per Jedec JC40.2 Standard 17		500	500	mA
f_{MAX}	Maximum clock frequency, CP_x to A or B	C_L = 50pF		125	125	MHz

Note:

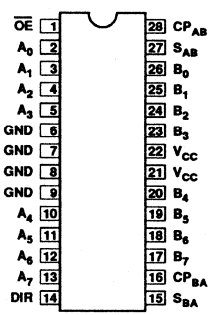
1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_I + \Sigma (C_L \times V_{CC}^2 \times f_O)$ where:
   f_I = input frequency in MHz, C_L = output load capacitance in pF,
   f_O = output frequency in MHz, V_{CC} = supply voltage in V,
   $\Sigma (C_L \times V_{CC}^2 \times f_O)$ = sum of outputs

ORDERING INFORMATION

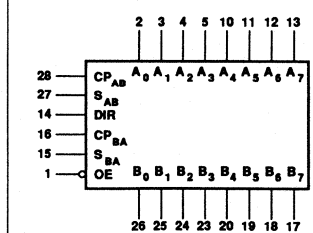
PACKAGES	TEMPERATURE RANGE	ORDER CODE
28-pin plastic DIP (300mil-wide)	-40°C to +85°C	74AC11646N 74ACT11646N
28-pin plastic SO (300mil-wide)	-40°C to +85°C	74AC11646D 74ACT11646D

PIN CONFIGURATION

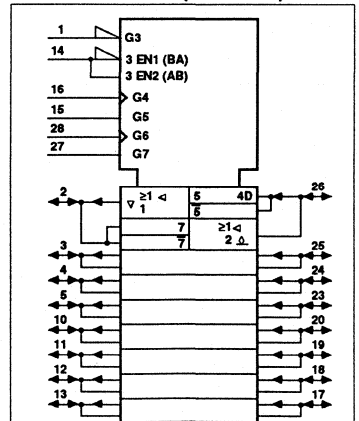
N and D Packages



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



into the registers as the appropriate clock pin goes to a High logic level. Output Enable ($\overline{OE}$) and DIR pins are provided to control the transceiver function. In the transceiver mode, data present at the High-impedance port may be stored in either the A or B register or both.

The Select inputs (S_X) can multiplex stored and real-time (transparent mode) data. The DIR input determines which bus will receive data when the Output Enable is active (Low). In the isolation mode ($\overline{OE}$ is High), A data may be stored in the B register and/or B data may be stored in the A register.

When an output function is disabled, the input function is still enabled and may be used to store and transmit data. Only one of the two buses, A or B, may be driven at a time. Figure 1 demonstrates the four fundamental bus-management functions that can be performed.

PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
1	$\overline{OE}$	Output enable input (active Low)
28	CP_{AB}	A-to-B clock input
16	CP_{BA}	B-to-A clock input
27	S_{AB}	A-to-B select input
15	S_{BA}	B-to-A select input
14	DIR	Data flow directional control input
2, 3, 4, 5, 10, 11, 12, 13	A_0 - A_7	A side inputs/outputs (3-state)
26, 25, 24, 23, 20, 19, 18, 17	B_0 - B_7	B side inputs/outputs (3-state)
6, 7, 8, 9	GND	Ground (0V)
21, 22	V_{CC}	Positive supply voltage

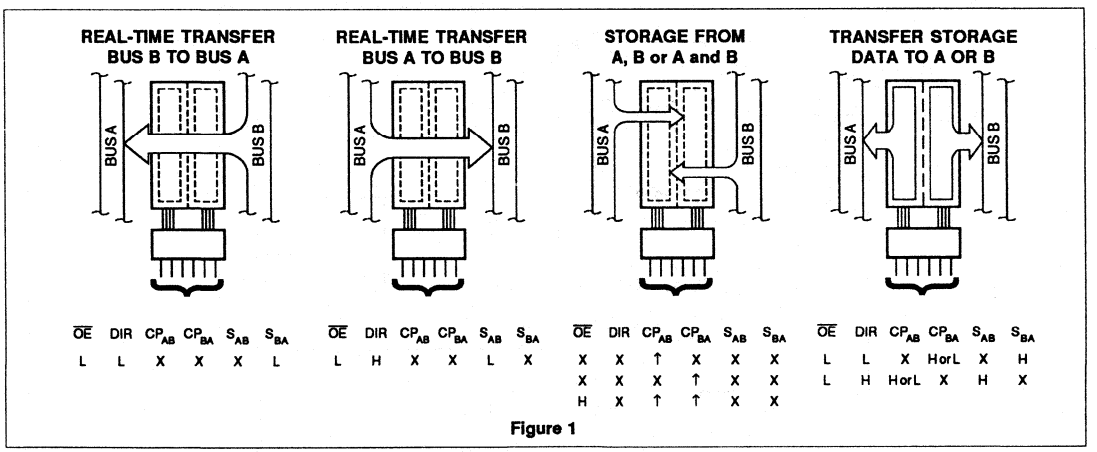


Figure 1

Octal Transceiver/Register w/Direction Pin; 3-State

74AC/ACT11646

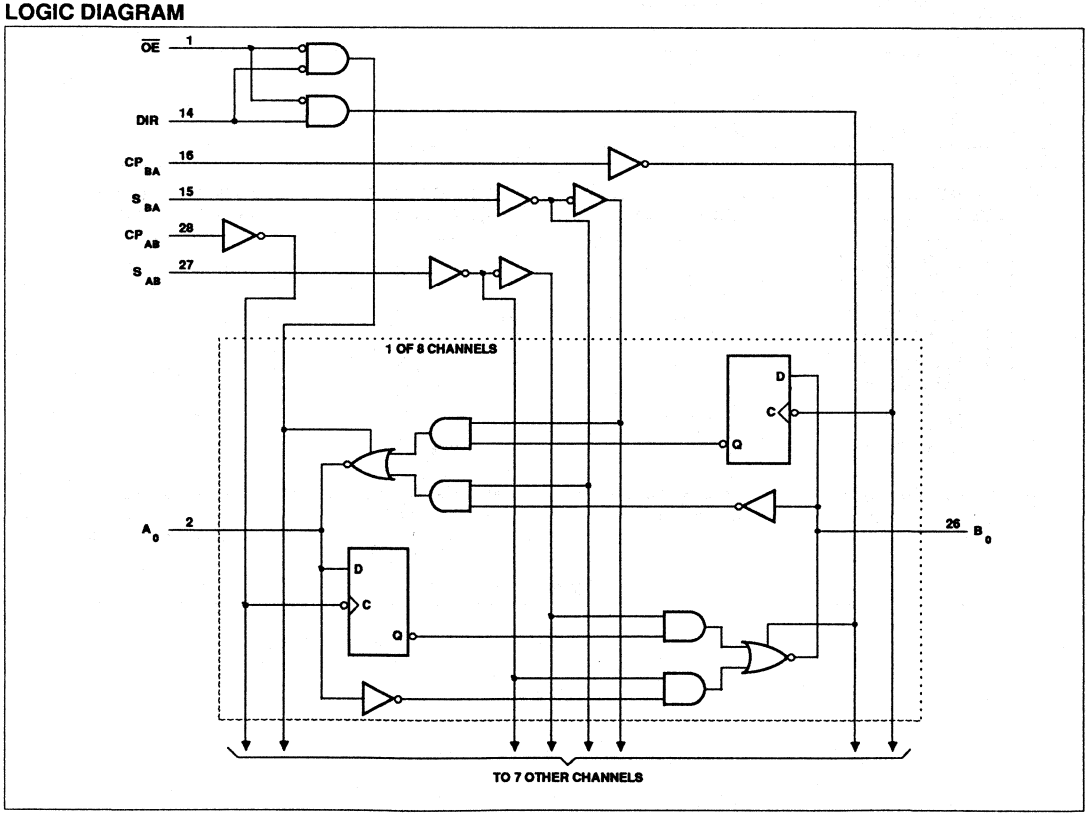
FUNCTION TABLE

INPUTS						DATA I/O*		OPERATING MODE
$\overline{OE}$	DIR	CP_{AB}	CP_{BA}	S_{AB}	S_{BA}	A_0 - A_7	B_0 - B_7	
X	X	↑	X	X	X	Input	un*	Store A, B unspecified*
X	X	X	↑	X	X	un*	Input	Store B, A unspecified*
H	X	↑	↑	X	X	Input	Input	Store A and B Data Isolation,
H	X	H or L	H or L	X	X			hold storage
L	L	X	X	X	L	Output	Input	Real time B data to A bus
L	L	X	H or L	X	H			Stored B Data to A Bus
L	H	X	X	L	X	Input	Output	Real time A data to B bus
L	H	H or L	X	H	X			Stored A data to B bus

* The data output functions may be enabled or disabled by various signals at the $\overline{OE}$ ad DIR inputs. Data input functions are always enabled, i.e, data at the bus pins will be stored on every Low-to-High transition of the clock.

un = unspecified
H = Highvoltage level
L = Low voltage level
X = Don't care
↑ = Low-to-High clock transition

LOGIC DIAGRAM



RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	74AC11646			74ACT11646			UNIT
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	DC supply voltage	3.0[1]	5.0	5.5	4.5	5.0	5.5	V
V_I	Input voltage	0		V_{CC}	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	0		V_{CC}	V
$\Delta t/\Delta v$	Input transition rise or fall rate	0		10	0		10	ns/V
T_A	Operating free-air temperature	-40		+85	-40		+85	°C

NOTE:

1. No electrical or switching characteristics are specified at $V_{CC} < 3V$. Operation between 2V and 3V is not recommended, but within that range, a device output will maintain a previously established logic state.

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	TEST CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 to+7.0	V
I_{IK} or V_I	DC input diode current[2]	$V_I < 0$	-20	mA
		$V_I > V_{CC}$	20	
	DC input voltage		-0.5 to V_{CC} +0.5	V
I_{OK} or V_O	DC output diode current[2]	$V_O < 0$	-50	mA
		$V_O > V_{CC}$	50	
	DC output voltage		-0.5 to V_{CC} +0.5	V
I_O	DC output source or sink current per output pin	V_O = 0 to V_{CC}	±50	mA
I_{CC} or I_{GND}	DC V_{CC} current		±200	mA
	DC ground current		±200	
T_{STG}	Storage temperature		-65 to 150	°C
P_{TOT}	Power dissipation per package Plastic DIP	Above 70°C:derate linearly by 8mW/K	500	mW
	Power dissipation per package Plastic surface mount (SO)	Above 70°C:derate linearly by 6mW/K	400	mW

NOTES:

1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		V_{CC}	74AC11646				74ACT11646				UNIT
					T_A = +25°C		T_A = -40°C to +85°C		T_A = +25°C		T_A = -40°C to +85°C		
				V	Min	Max	Min	Max	Min	Max	Min	Max	
V_{IH}	High-level input voltage			3.0	2.10		2.10						V
				4.5	3.15		3.15		2.0		2.0		
				5.5	3.85		3.85		2.0		2.0		
V_{IL}	Low-level input voltage			3.0		0.90		0.90					V
				4.5		1.35		1.35		0.8		0.8	
				5.5		1.65		1.65		0.8		0.8	
V_{OH}	High-level output voltage	V_I = V_{IL} or V_{IH}	I_{OH} = -50µA	3.0	2.9		2.9						V
				4.5	4.4		4.4		4.4		4.4		
				5.5	5.4		5.4		5.4		5.4		
			I_{OH} = -4mA	3.0	2.58		2.48						
			I_{OH} = -24mA	4.5	3.94		3.8		3.94		3.8		
				5.5	4.94		4.8		4.94		4.8		
			I_{OH} = -75mA[1]	5.5			3.85				3.85		
V_{OL}	Low-level output voltage	V_I = V_{IL} or V_{IH}	I_{OL} = 50µA	3.0		0.1		0.1					V
				4.5		0.1		0.1		0.1		0.1	
				5.5		0.1		0.1		0.1		0.1	
			I_{OL} = 12mA	3.0		0.36		0.44					
			I_{OL} = 24mA	4.5		0.36		0.44		0.36		0.44	
				5.5		0.36		0.44		0.36		0.44	
			I_{OL} = 75mA[1]	5.5				1.65				1.65	
I_I	Input leakage current	V_I = V_{CC} or GND		5.5		±0.1		±1.0		±0.1		±1.0	µA
I_{OZ}	3-State output off-state current	V_I = V_{IL} or V_{IH}, V_O = V_{CC} or GND		5.5		±0.5		±5.0		±0.5		±5.0	µA
I_{CC}	Quiescent supply current	V_I = V_{CC} or GND, I_O = 0		5.5		8.0		80		8.0		80	µA
ΔI_{CC}	Supply current, TTL inputs High[2]	One input at 3.4V, other inputs at V_{CC} or GND		5.5						0.9		1.0	mA

NOTES:
1. Not more than one output should be tested at a time, and the duration of the test should not exceed 10ms.
2. This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0V or V_{CC}.

74AC/ACT11648

Octal Transceiver/Register w/Direction Pin (3-State), INV

Objective Specification

FEATURES

- **Octal bidirectional bus interface**
- **3-State buffers**
- **Independent registers for A and B buses**
- **Multiplexed real-time and stored data**
- **Output capability: ±24 mA**
- **CMOS (AC) and TTL (ACT) voltage level inputs**
- **50Ω incident wave switching**
- **Center-pin V_{CC} and ground configuration to minimize high-speed switching noise**
- **I_{CC} category: MSI**

DESCRIPTION

The 74AC/ACT11648 high-performance CMOS devices combine very high speed and high output drive comparable to the most advanced TTL families.

The 74AC/ACT11648 device is an octal transceiver/register featuring inverting 3-State bus compatible outputs in both send and receive directions, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the input bus or from internal registers. Data on the A or B bus will be clocked into

GENERAL INFORMATION

SYMBOL	PARAMETER	CONDITIONS T_A = 25°C; GND = 0V; V_{CC} = 5.0V		TYPICAL AC	TYPICAL ACT	UNIT
t_{PLH}/t_{PHL}	Propagation delay $\overline{A}_n$ to B_n, or $\overline{B}_n$ to A_n	C_L = 50pF		5.6	6.0	ns
C_{PD}	Power dissipation capacitance per transceiver[1]	f = 1MHz;	Enabled	60	60	pF
		C_L = 50pF	Disabled	15	15	
C_{IN}	Input capacitance	V_I = 0V or V_{CC}		4.5	4.5	pF
C_{IO}	I/O capacitance	V_O = 0V or V_{CC}; Disabled		12	12	pF
I_{LATCH}	Latch-up current	Per Jedec JC40.2 Standard 17		500	500	mA
f_{MAX}	Maximum clock frequency, CP_{XX} to $\overline{A}$ or $\overline{B}$	C_L = 50pF		125	125	MHz

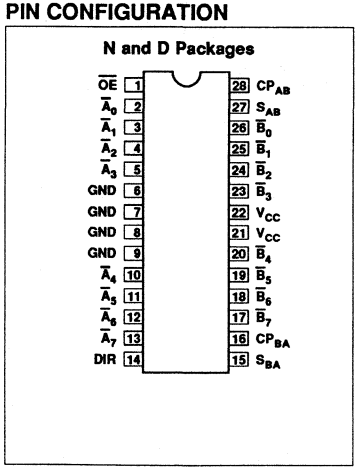
Note:

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_I + \Sigma (C_L \times V_{CC}^2 \times f_O)$ where:
   f_I = input frequency in MHz, C_L = output load capacitance in pF,
   f_O = output frequency in MHz, V_{CC} = supply voltage in V,
   $\Sigma (C_L \times V_{CC}^2 \times f_O)$ = sum of outputs

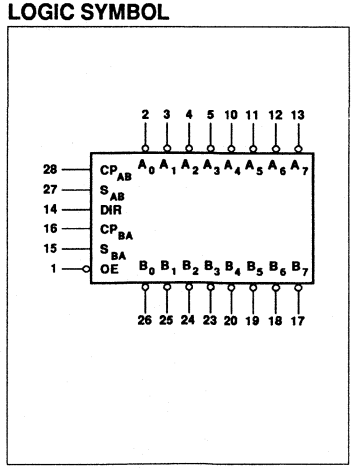
ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE
28-pin plastic DIP (300mil-wide)	-40°C to +85°C	74AC11648N 74ACT11648N
28-pin plastic SO (300mil-wide)	-40°C to +85°C	74AC11648D 74ACT11648D

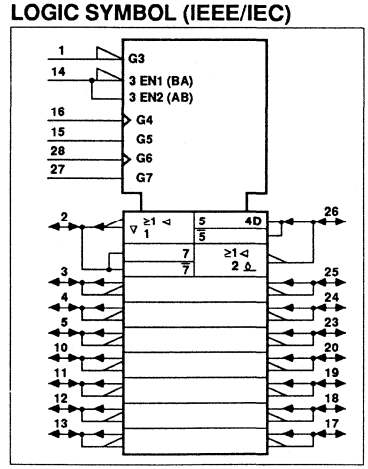
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



the registers as the appropriate clock pin goes to a High logic level. Output Enable ($\overline{OE}$) and DIR pins are provided to control the transceiver function. In the transceiver mode, data present at the High-impedance port may be stored in either the A or B register or both.

The Select inputs (S_X) can multiplex stored and real-time (transparent mode) data. The DIR input determines which bus will receive data when the Output Enable is active (Low). In the isolation mode ($\overline{OE}$ is High), A data may be stored in the B register and/or B data may be stored in the A register.

When an output function is disabled, the input function is still enabled and may be used to store and transmit data. Only one of the two buses, A or B, may be driven at a time. Figure 1 demonstrates the four fundamental bus-management functions that can be performed.

PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
1	$\overline{OE}$	Output enable input (active Low)
28	CP_{AB}	A-to-B clock input
16	CP_{BA}	B-to-A clock input
27	S_{AB}	A-to-B select input
15	S_{BA}	B-to-A select input
14	DIR	Data flow directional control input
2, 3, 4, 5, 10, 11, 12, 13	$\overline{A}_0$ - $\overline{A}_7$	A side inputs/outputs (3-state)
26, 25, 24, 23, 20, 19, 18, 17	$\overline{B}_0$ - $\overline{B}_7$	B side inputs/outputs (3-state)
6, 7, 8, 9	GND	Ground (0V)
21, 22	V_{CC}	Positive supply voltage

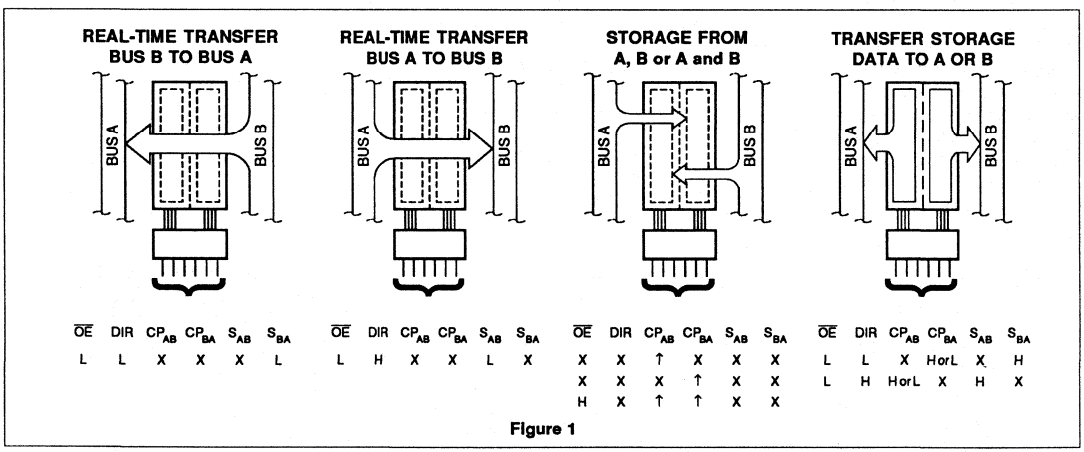


Figure 1

Octal Transceiver/Register w/Direction Pin (3-State), INV

74AC/ACT11648

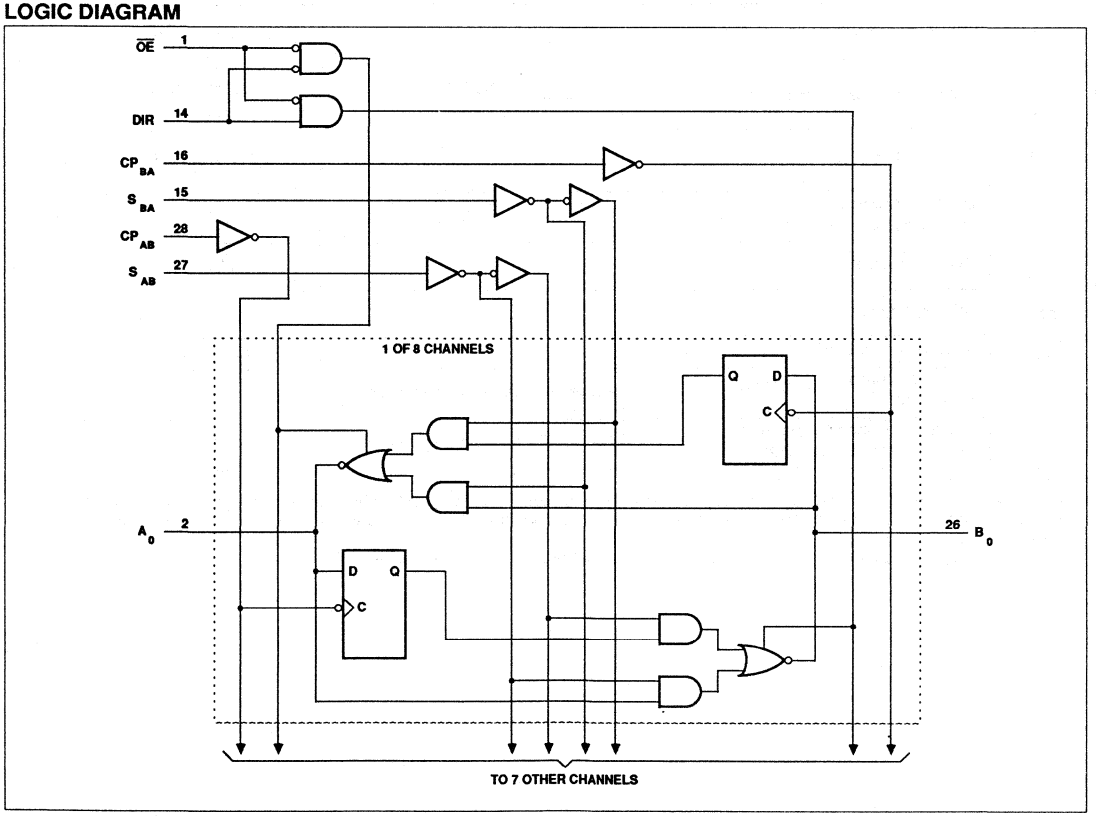
FUNCTION TABLE

INPUTS						DATA I/O*		OPERATING MODE
$\overline{OE}$	DIR	CP_{AB}	CP_{BA}	S_{AB}	S_{BA}	$\overline{A}_0$ - $\overline{A}_7$	$\overline{B}_0$ - $\overline{B}_7$	
X	X	↑	X	X	X	Input	un*	Store A, B unspecified*
X	X	X	↑	X	X	un*	Input	Store B, A unspecified*
H	X	↑	↑	X	X	Input	Input	Store A and B Data Isolation,
H	X	H or L	H or L	X	X			hold storage
L	L	X	X	X	L	Output	Input	Real time $\overline{B}$ data to A bus
L	L	X	H or L	X	H			Stored $\overline{B}$ Data to A Bus
L	H	X	X	L	X	Input	Output	Real time $\overline{A}$ data to B bus
L	H	H or L	X	H	X			Stored $\overline{A}$ data to B bus

* The data output functions may be enabled or disabled by various signals at the $\overline{OE}$ ad DIR inputs. Data input functions are always enabled, i.e, data at the bus pins will be stored on every Low-to-High transition of the clock.

un = unspecified
H = Highvoltage level
L = Low voltage level
X = Don't care
↑ = Low-to-High clock transition

LOGIC DIAGRAM



RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	74AC11648			74ACT11648			UNIT
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	DC supply voltage	3.0[1]	5.0	5.5	4.5	5.0	5.5	V
V_I	Input voltage	0		V_{CC}	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	0		V_{CC}	V
$\Delta t/\Delta v$	Input transition rise or fall rate	0		10	0		10	ns/V
T_A	Operating free-air temperature	-40		+85	-40		+85	°C

NOTE:

1. No electrical or switching characteristics are specified at V_{CC} < 3V. Operation between 2V and 3V is not recommended, but within that range, a device output will maintain a previously established logic state.

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	TEST CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 to+7.0	V
I_{IK} or V_I	DC input diode current[2]	$V_I < 0$	-20	mA
		$V_I > V_{CC}$	20	
	DC input voltage		-0.5 to V_{CC} +0.5	V
I_{OK} or V_O	DC output diode current[2]	$V_O < 0$	-50	mA
		$V_O > V_{CC}$	50	
	DC output voltage		-0.5 to V_{CC} +0.5	V
I_O	DC output source or sink current per output pin	V_O = 0 to V_{CC}	±50	mA
I_{CC} or I_{GND}	DC V_{CC} current		±200	mA
	DC ground current		±200	
T_{STG}	Storage temperature		-65 to 150	°C
P_{TOT}	Power dissipation per package Plastic DIP	Above 70°C:derate linearly by 8mW/K	500	mW
	Power dissipation per package Plastic surface mount (SO)	Above 70°C:derate linearly by 6mW/K	400	mW

NOTES:

1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		V_{CC}	74AC11648				74ACT11648				UNIT
					T_A = +25°C		T_A = -40°C to +85°C		T_A = +25°C		T_A = -40°C to +85°C		
				V	Min	Max	Min	Max	Min	Max	Min	Max	
V_{IH}	High-level input voltage			3.0	2.10		2.10						V
				4.5	3.15		3.15		2.0		2.0		
				5.5	3.85		3.85		2.0		2.0		
V_{IL}	Low-level input voltage			3.0		0.90		0.90					V
				4.5		1.35		1.35		0.8		0.8	
				5.5		1.65		1.65		0.8		0.8	
V_{OH}	High-level output voltage	V_I = V_{IL} or V_{IH}	I_{OH} = -50μA	3.0	2.9		2.9						V
				4.5	4.4		4.4		4.4		4.4		
				5.5	5.4		5.4		5.4		5.4		
			I_{OH} = -4mA	3.0	2.58		2.48						
			I_{OH} = -24mA	4.5	3.94		3.8		3.94		3.8		
				5.5	4.94		4.8		4.94		4.8		
			I_{OH} = -75mA[1]	5.5			3.85				3.85		
V_{OL}	Low-level output voltage	V_I = V_{IL} or V_{IH}	I_{OL} = 50μA	3.0		0.1		0.1					V
				4.5		0.1		0.1		0.1		0.1	
				5.5		0.1		0.1		0.1		0.1	
			I_{OL} = 12mA	3.0		0.36		0.44					
			I_{OL} = 24mA	4.5		0.36		0.44		0.36		0.44	
				5.5		0.36		0.44		0.36		0.44	
			I_{OL} = 75mA[1]	5.5				1.65				1.65	
I_I	Input leakage current	V_I = V_{CC} or GND		5.5		±0.1		±1.0		±0.1		±1.0	μA
I_{OZ}	3-State output off-state current	V_I = V_{IL} or V_{IH}, V_O = V_{CC} or GND		5.5		±0.5		±5.0		±0.5		±5.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC} or GND, I_O = 0		5.5		8.0		80		8.0		80	μA
ΔI_{CC}	Supply current, TTL inputs High[2]	One input at 3.4V, other inputs at V_{CC} or GND		5.5						0.9		1.0	mA

NOTES:
1. Not more than one output should be tested at a time, and the duration of the test should not exceed 10ms.
2. This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0V or V_{CC}.

74AC/ACT11651

Octal Transceiver/Register w/Dual Enable (3-State), INV

Objective Specification

FEATURES

- **Octal bidirectional bus interface**
- **3-State buffers**
- **Independent registers for A and B buses**
- **Multiplexed real-time and stored data**
- **Output capability: ±24 mA**
- **CMOS (AC) and TTL (ACT) voltage level inputs**
- **50Ω incident wave switching**
- **Center-pin V_{CC} and ground configuration to minimize high-speed switching noise**
- **I_{CC} category: MSI**

DESCRIPTION

The 74AC/ACT11651 high-performance CMOS devices combine very high speed and high output drive comparable to the most advanced TTL families.

The 74AC/ACT11651 device is an octal transceiver/register featuring inverting 3-State bus compatible outputs in both send and receive directions, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the input bus or from internal registers. Data on the A or B bus will be clocked into

GENERAL INFORMATION

SYMBOL	PARAMETER	CONDITIONS T_A = 25°C; GND = 0V; V_{CC} = 5.0V		TYPICAL AC	TYPICAL ACT	UNIT
t_{PLH}/ t_{PHL}	Propagation delay $\overline{A}_n$ to B_n, or $\overline{B}_n$ to A_n	C_L = 50pF		5.6	6.0	ns
C_{PD}	Power dissipation capacitance per transceiver[1]	f = 1MHz; C_L = 50pF	Enabled	60	60	pF
			Disabled	15	15	
C_{IN}	Input capacitance	V_I = 0V or V_{CC}		4.5	4.5	pF
C_{IO}	I/O capacitance	V_O = 0V or V_{CC}; Disabled		12	12	pF
I_{LATCH}	Latch-up current	Per Jedec JC40.2 Standard 17		500	500	mA
f_{MAX}	Maximum clock frequency, CP_x to $\overline{A}$ or $\overline{B}$	C_L = 50pF		125	125	MHz

Note:

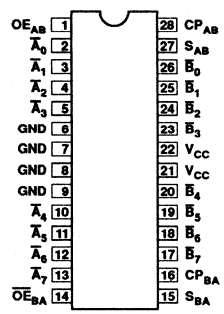
1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_I + \Sigma (C_L \times V_{CC}^2 \times f_O)$ where:
   f_I = input frequency in MHz, C_L = output load capacitance in pF,
   f_O = output frequency in MHz, V_{CC} = supply voltage in V,
   $\Sigma (C_L \times V_{CC}^2 \times f_O)$ = sum of outputs

ORDERING INFORMATION

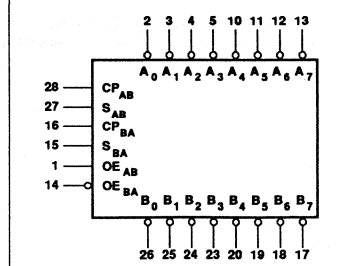
PACKAGES	TEMPERATURE RANGE	ORDER CODE
28-pin plastic DIP (300mil-wide)	-40°C to +85°C	74AC11651N 74ACT11651N
28-pin plastic SO (300mil-wide)	-40°C to +85°C	74AC11651D 74ACT11651D

PIN CONFIGURATION

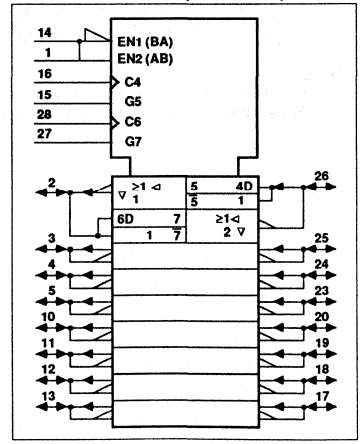
N and D Packages



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



the registers as the appropriate clock pin goes to a High logic level. Output Enable (OE_{AB}, $\overline{OE}_{BA}$) and Select pins (S_{AB}, S_{BA}) are provided for bus management. In the transceiver mode, data present at the High-impedance port may be stored in either the A or B register or both.

Figure 1 demonstrates the four fundamental bus-management functions that can be performed. The select pins (S_{AB}, S_{BA}) determine whether data is stored or transferred through the device in real-time. The Output Enable pins (OE_{AB}, $\overline{OE}_{BA}$) determine the direction of the data flow.

PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
1	OE_{AB}	A-to-B output enable input
14	$\overline{OE}_{BA}$	B-to-A output enable input (active Low)
28	CP_{AB}	A-to-B clock input
16	CP_{BA}	B-to-A clock input
27	S_{AB}	A-to-B select input
15	S_{BA}	B-to-A select input
2, 3, 4, 5, 10, 11, 12, 13	A_0 - A_7	A side inputs/outputs (3-state)
26, 25, 24, 23, 20, 19, 18, 17	B_0 - B_7	B side inputs/outputs (3-state)
6, 7, 8, 9	GND	Ground (0V)
21, 22	V_{CC}	Positive supply voltage

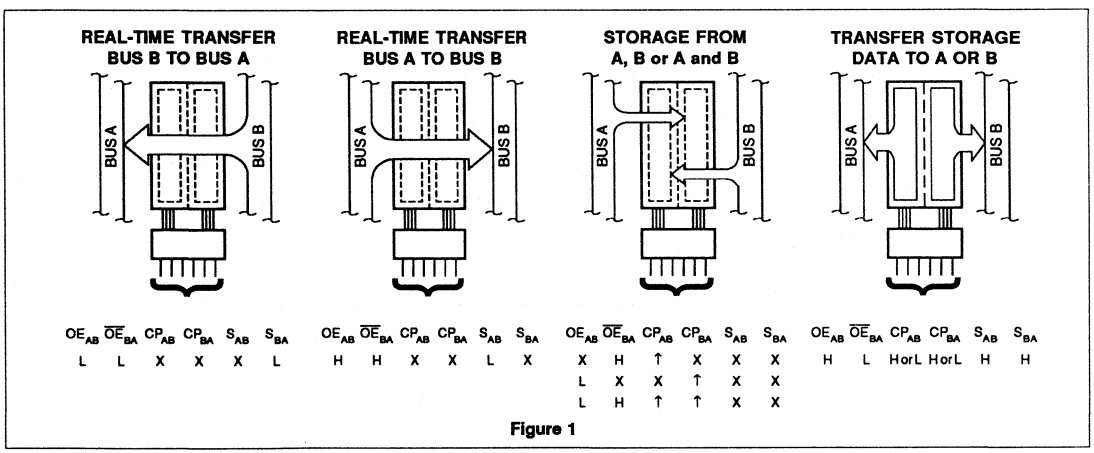


Figure 1

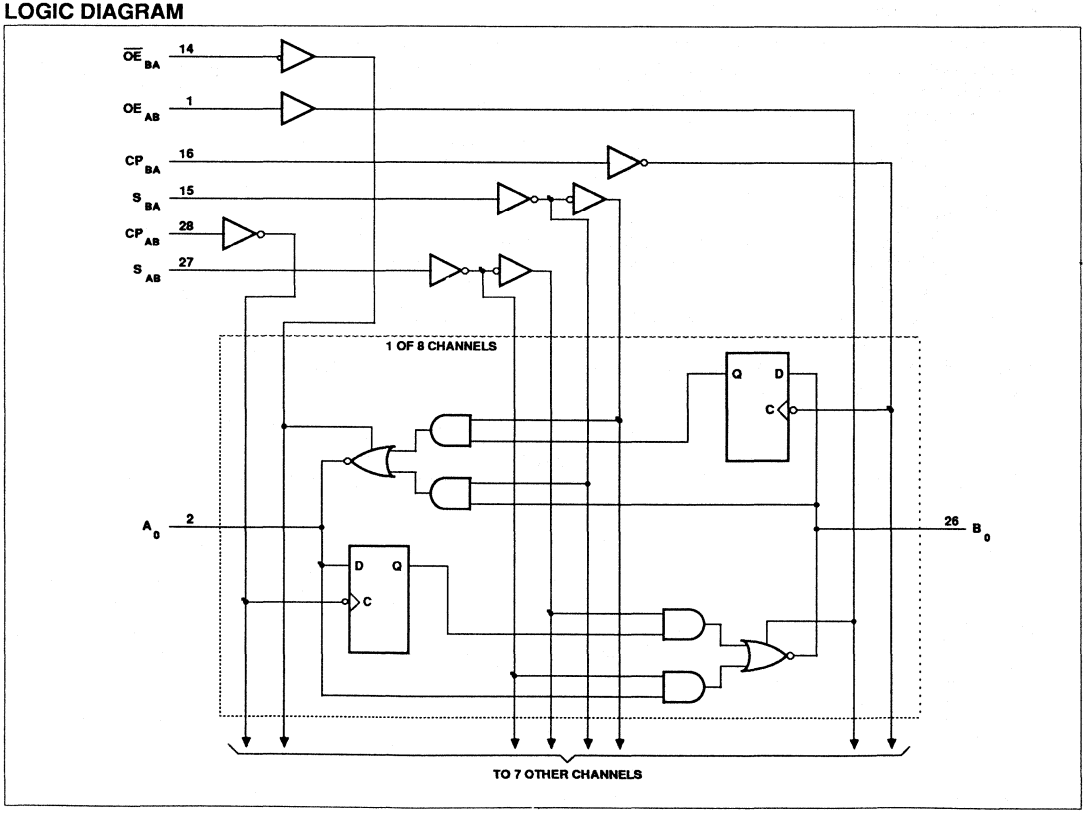
FUNCTION TABLE

OPERATING MODE	INPUTS						DATA I/O*	
	OE_{AB}	$\overline{OE}_{BA}$	CP_{AB}	CP_{BA}	S_{AB}	S_{BA}	$\overline{A}_0$ - $\overline{A}_7$	$\overline{B}_0$ - $\overline{B}_7$
Isolation	L	H	H or L	H or L	X	X	Input	Input
Store A and B data	L	H	↑	↑	X	X		
Store A, Hold B	X	H	↑	H or L	X	X	Input	un*
Store A in both registers	H	H	↑	↑	L	X	Input	Output
Hold A, Store B	L	X	H or L	↑	X	X	un*	Input
Store B in both registers	L	L	↑	↑	X	L	Output	Input
Real time $\overline{B}$ data to A bus	L	L	X	X	X	L	Output	Input
Stored $\overline{B}$ data to A bus	L	L	X	H or L	X	H		
Real time $\overline{A}$ data to B bus	H	H	X	X	L	X	Input	Output
Stored $\overline{A}$ data to B bus	H	H	H or L	X	H	X		
Stored $\overline{A}$ data to B bus	H	L	H or L	H or L	H	H	Output	Output
Stored $\overline{B}$ data to A bus								

* The data output functions may be enabled or disabled by various signals at the OE_{AB} and the $\overline{OE}_{BA}$ inputs. Data input functions are always enabled, i.e., data at the bus pins will be stored on every Low-to-High transition of the clock.

un = unspecified
H = High voltage level
L = Low voltage level
X = Don't care
↑ = Low-to-High clock transition

LOGIC DIAGRAM



RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	74AC11651			74ACT11651			UNIT
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	DC supply voltage	3.0[1]	5.0	5.5	4.5	5.0	5.5	V
V_I	Input voltage	0		V_{CC}	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	0		V_{CC}	V
$\Delta t/\Delta v$	Input transition rise or fall rate	0		10	0		10	ns/V
T_A	Operating free-air temperature	-40		+85	-40		+85	°C

NOTE:

1. No electrical or switching characteristics are specified at V_{CC} < 3V. Operation between 2V and 3V is not recommended, but within that range, a device output will maintain a previously established logic state.

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	TEST CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 to+7.0	V
I_{IK} or V_I	DC input diode current[2]	$V_I < 0$	-20	mA
		$V_I > V_{CC}$	20	
	DC input voltage		-0.5 to V_{CC} +0.5	V
I_{OK} or V_O	DC output diode current[2]	$V_O < 0$	-50	mA
		$V_O > V_{CC}$	50	
	DC output voltage		-0.5 to V_{CC} +0.5	V
I_O	DC output source or sink current per output pin	V_O = 0 to V_{CC}	±50	mA
I_{CC} or I_{GND}	DC V_{CC} current		±200	mA
	DC ground current		±200	
T_{STG}	Storage temperature		-65 to 150	°C
P_{TOT}	Power dissipation per package Plastic DIP	Above 70°C:derate linearly by 8mW/K	500	mW
	Power dissipation per package Plastic surface mount (SO)	Above 70°C:derate linearly by 6mW/K	400	mW

NOTES:

1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		V_{CC}	74AC11651				74ACT11651				UNIT
					T_A = +25°C		T_A = -40°C to +85°C		T_A = +25°C		T_A = -40°C to +85°C		
				V	Min	Max	Min	Max	Min	Max	Min	Max	
V_{IH}	High-level input voltage			3.0	2.10		2.10						V
				4.5	3.15		3.15		2.0		2.0		
				5.5	3.85		3.85		2.0		2.0		
V_{IL}	Low-level input voltage			3.0		0.90		0.90					V
				4.5		1.35		1.35		0.8		0.8	
				5.5		1.65		1.65		0.8		0.8	
V_{OH}	High-level output voltage	V_I = V_{IL} or V_{IH}	I_{OH} = -50μA	3.0	2.9		2.9						V
				4.5	4.4		4.4		4.4		4.4		
				5.5	5.4		5.4		5.4		5.4		
			I_{OH} = -4mA	3.0	2.58		2.48						
			I_{OH} = -24mA	4.5	3.94		3.8		3.94		3.8		
				5.5	4.94		4.8		4.94		4.8		
			I_{OH} = -75mA[1]	5.5			3.85				3.85		
V_{OL}	Low-level output voltage	V_I = V_{IL} or V_{IH}	I_{OL} = 50μA	3.0		0.1		0.1					V
				4.5		0.1		0.1		0.1		0.1	
				5.5		0.1		0.1		0.1		0.1	
			I_{OL} = 12mA	3.0		0.36		0.44					
			I_{OL} = 24mA	4.5		0.36		0.44		0.36		0.44	
				5.5		0.36		0.44		0.36		0.44	
			I_{OL} = 75mA[1]	5.5				1.65				1.65	
I_I	Input leakage current	V_I = V_{CC} or GND		5.5		±0.1		±1.0		±0.1		±1.0	μA
I_{OZ}	3-State output off-state current	V_I = V_{IL} or V_{IH}, V_O = V_{CC} or GND		5.5		±0.5		±5.0		±0.5		±5.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC} or GND, I_O = 0		5.5		8.0		80		8.0		80	μA
ΔI_{CC}	Supply current, TTL inputs High[2]	One input at 3.4V, other inputs at V_{CC} or GND		5.5						0.9		1.0	mA

NOTES:
1. Not more than one output should be tested at a time, and the duration of the test should not exceed 10ms.
2. This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0V or V_{CC}.

74AC/ACT11652

Octal Transceiver/Register w/Dual Enable (3-State)

Objective Specification

FEATURES

- **Octal bidirectional bus interface**
- **3-State buffers**
- **Independent registers for A and B buses**
- **Multiplexed real-time and stored data**
- **Output capability: ±24 mA**
- **CMOS (AC) and TTL (ACT) voltage level inputs**
- **50Ω incident wave switching**
- **Center-pin V_{CC} and ground configuration to minimize high-speed switching noise**
- **I_{CC} category: MSI**

DESCRIPTION

The 74AC/ACT11652 high-performance CMOS devices combine very high speed and high output drive comparable to the most advanced TTL families.

The 74AC/ACT11652 device is an octal transceiver/register featuring non-inverting 3-State bus compatible outputs in both send and receive directions, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the input bus or from internal registers. Data on the A or B bus will be clocked

GENERAL INFORMATION

SYMBOL	PARAMETER	CONDITIONS T_A = 25°C; GND = 0V; V_{CC} = 5.0V		TYPICAL AC	TYPICAL ACT	UNIT
t_{PLH}/t_{PHL}	Propagation delay A_n to B_n, or B_n to A_n	C_L = 50pF		5.4	7.2	ns
C_{PD}	Power dissipation capacitance per transceiver[1]	f = 1MHz;	Enabled	60	60	pF
		C_L = 50pF	Disabled	15	15	
C_{IN}	Input capacitance	V_I = 0V or V_{CC}		4.5	4.5	pF
C_{IO}	I/O capacitance	V_O = 0V or V_{CC}; Disabled		12	12	pF
I_{LATCH}	Latch-up current	Per Jedec JC40.2 Standard 17		500	500	mA
f_{MAX}	Maximum clock frequency, CP_x to A or B	C_L = 50pF		125	125	MHz

Note:

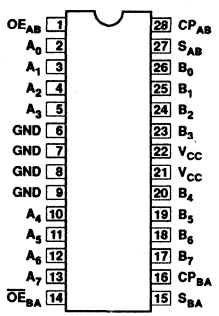
1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_I + \Sigma (C_L \times V_{CC}^2 \times f_O)$ where:
   f_I = input frequency in MHz, C_L = output load capacitance in pF,
   f_O = output frequency in MHz, V_{CC} = supply voltage in V,
   $\Sigma (C_L \times V_{CC}^2 \times f_O)$ = sum of outputs

ORDERING INFORMATION

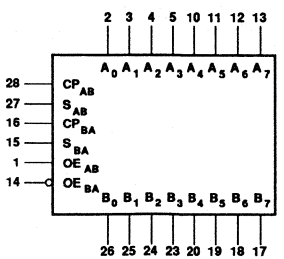
PACKAGES	TEMPERATURE RANGE	ORDER CODE
28-pin plastic DIP (300mil-wide)	-40°C to +85°C	74AC11652N 74ACT11652N
28-pin plastic SO (300mil-wide)	-40°C to +85°C	74AC11652D 74ACT11652D

PIN CONFIGURATION

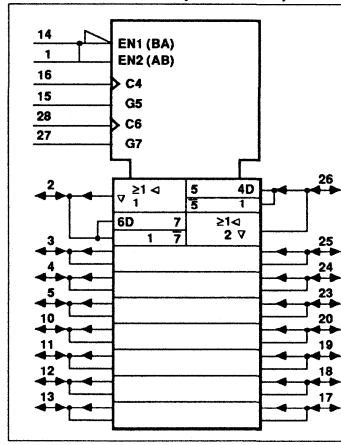
N and D Packages



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



June 12, 1989

Octal Transceiver/Register w/Dual Enable (3-State)

74AC/ACT11652

into the registers as the appropriate clock pin goes to a High logic level. Output Enable (OE_{AB}, $\overline{OE}_{BA}$) and Select pins (S_{AB}, S_{BA}) are provided for bus management. In the transceiver mode, data present at the High-impedance port may be stored in either the A or B register or both.

Figure 1 demonstrates the four fundamental bus-management functions that can be performed. The select pins (S_{AB}, S_{BA}) determine whether data is stored or transferred through the device in real-time. The Output Enable pins (OE_{AB}, $\overline{OE}_{BA}$) determine the direction of the data flow.

PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
1	OE_{AB}	A-to-B output enable input
14	$\overline{OE}_{BA}$	B-to-A output enable input (active Low)
28	CP_{AB}	A-to-B clock input
16	CP_{BA}	B-to-A clock input
27	S_{AB}	A-to-B select input
15	S_{BA}	B-to-A select input
2, 3, 4, 5, 10, 11, 12, 13	$A_0 - A_7$	A side inputs/outputs (3-state)
26, 25, 24, 23, 20, 19, 18, 17	$B_0 - B_7$	B side inputs/outputs (3-state)
6, 7, 8, 9	GND	Ground (0V)
21, 22	V_{CC}	Positive supply voltage

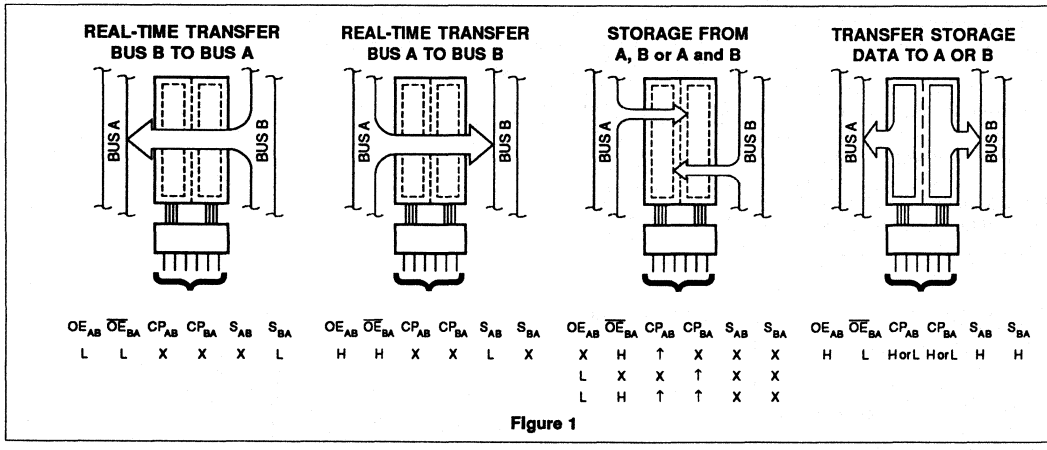


Figure 1

Octal Transceiver/Register w/Dual Enable (3-State)

74AC/ACT11652

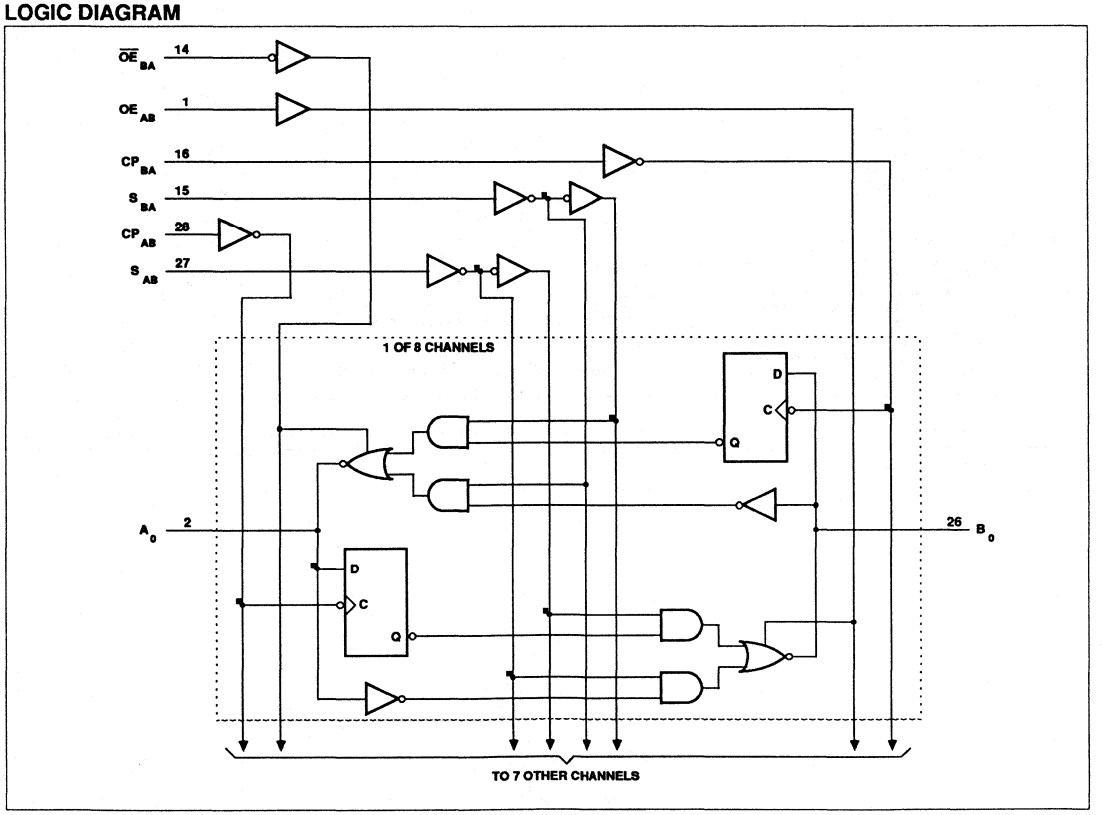
FUNCTION TABLE

OPERATING MODE	INPUTS						DATA I/O*	
	OE_{AB}	$\overline{OE}_{BA}$	CP_{AB}	CP_{BA}	S_{AB}	S_{BA}	$A_0 - A_7$	$B_0 - B_7$
Isolation	L	H	H or L	H or L	X	X	Input	Input
Store A and B data	L	H	↑	↑	X	X		
Store A, Hold B	X	H	↑	H or L	X	X	Input	un*
Store A in both registers	H	H	↑	↑	L	X	Input	Output
Hold A, Store B	L	X	H or L	↑	X	X	un*	Input
Store B in both registers	L	L	↑	↑	X	L	Output	Input
Real time $\overline{B}$ data to A bus	L	L	X	X	X	L	Output	Input
Stored $\overline{B}$ data to A bus	L	L	X	H or L	X	H		
Real time $\overline{A}$ data to B bus	H	H	X	X	L	X	Input	Output
Stored $\overline{A}$ data to B bus	H	H	H or L	X	H	X		
Stored $\overline{A}$ data to B bus	H	L	H or L	H or L	H	H	Output	Output
Stored $\overline{B}$ data to A bus								

* The data output functions may be enabled or disabled by various signals at the OE_{AB} and the $\overline{OE}_{BA}$ inputs. Data input functions are always enabled, i.e., data at the bus pins will be stored on every Low-to-High transition of the clock.

un = unspecified
H = High voltage level
L = Low voltage level
X = Don't care
↑ = Low-to-High clock transition

LOGIC DIAGRAM



RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	74AC11652			74ACT11652			UNIT
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	DC supply voltage	3.0[1]	5.0	5.5	4.5	5.0	5.5	V
V_I	Input voltage	0		V_{CC}	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	0		V_{CC}	V
$\Delta t/\Delta v$	Input transition rise or fall rate	0		10	0		10	ns/V
T_A	Operating free-air temperature	-40		+85	-40		+85	°C

NOTE:

1. No electrical or switching characteristics are specified at $V_{CC} < 3V$. Operation between 2V and 3V is not recommended, but within that range, a device output will maintain a previously established logic state.

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	TEST CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 to+7.0	V
I_{IK} or V_I	DC input diode current[2]	$V_I < 0$	-20	mA
		$V_I > V_{CC}$	20	
	DC input voltage		-0.5 to V_{CC} +0.5	V
I_{OK} or V_O	DC output diode current[2]	$V_O < 0$	-50	mA
		$V_O > V_{CC}$	50	
	DC output voltage		-0.5 to V_{CC} +0.5	V
I_O	DC output source or sink current per output pin	V_O = 0 to V_{CC}	±50	mA
I_{CC} or I_{GND}	DC V_{CC} current		±200	mA
	DC ground current		±200	
T_{STG}	Storage temperature		-65 to 150	°C
P_{TOT}	Power dissipation per package Plastic DIP	Above 70°C:derate linearly by 8mW/K	500	mW
	Power dissipation per package Plastic surface mount (SO)	Above 70°C:derate linearly by 6mW/K	400	mW

NOTES:

1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		V_{CC}	74AC11652				74ACT11652				UNIT
					T_A = +25°C		T_A = -40°C to +85°C		T_A = +25°C		T_A = -40°C to +85°C		
				V	Min	Max	Min	Max	Min	Max	Min	Max	
V_{IH}	High-level input voltage			3.0	2.10		2.10						V
				4.5	3.15		3.15		2.0		2.0		
				5.5	3.85		3.85		2.0		2.0		
V_{IL}	Low-level input voltage			3.0		0.90		0.90					V
				4.5		1.35		1.35		0.8		0.8	
				5.5		1.65		1.65		0.8		0.8	
V_{OH}	High-level output voltage	V_I = V_{IL} or V_{IH}	I_{OH} = -50μA	3.0	2.9		2.9						V
				4.5	4.4		4.4		4.4		4.4		
				5.5	5.4		5.4		5.4		5.4		
			I_{OH} = -4mA	3.0	2.58		2.48						
			I_{OH} = -24mA	4.5	3.94		3.8		3.94		3.8		
				5.5	4.94		4.8		4.94		4.8		
			I_{OH} = -75mA[1]	5.5			3.85				3.85		
V_{OL}	Low-level output voltage	V_I = V_{IL} or V_{IH}	I_{OL} = 50μA	3.0		0.1		0.1					V
				4.5		0.1		0.1		0.1		0.1	
				5.5		0.1		0.1		0.1		0.1	
			I_{OL} = 12mA	3.0		0.36		0.44					
			I_{OL} = 24mA	4.5		0.36		0.44		0.36		0.44	
				5.5		0.36		0.44		0.36		0.44	
			I_{OL} = 75mA[1]	5.5				1.65				1.65	
I_I	Input leakage current	V_I = V_{CC} or GND		5.5		±0.1		±1.0		±0.1		±1.0	μA
I_{OZ}	3-State output off-state current	V_I = V_{IL} or V_{IH}, V_O = V_{CC} or GND		5.5		±0.5		±5.0		±0.5		±5.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC} or GND, I_O = 0		5.5		8.0		80		8.0		80	μA
ΔI_{CC}	Supply current, TTL inputs High[2]	One input at 3.4V, other inputs at V_{CC} or GND		5.5						0.9		1.0	mA

NOTES:
1. Not more than one output should be tested at a time, and the duration of the test should not exceed 10ms.
2. This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0V or V_{CC}.

74AC/ACT11655

Octal Buffer/Line Driver with 9-Bit Parity Checker/Generator (3-State), INV

Objective Specification

FEATURES

- **Inverting 3-State outputs**
- **Combines '240 and '280 functions in one package**
- **Output capability: ±24 mA**
- **CMOS (AC) and TTL (ACT) voltage level inputs**
- **50Ω incident wave switching**
- **Center-pin V_{CC} and ground configuration to minimize high-speed switching noise**
- **I_{CC} category: MSI**

DESCRIPTION

The 74AC/ACT11655 high-performance CMOS devices combine very high speed and high output drive comparable to the most advanced TTL families.

The 74AC/ACT11655 device is an octal buffer and line driver with parity generator/checker designed for use with memory address drivers, clock drivers, and bus-oriented transmitters/receivers.

GENERAL INFORMATION

SYMBOL	PARAMETER	CONDITIONS T_A = 25°C; GND = 0V; V_{CC} = 5.0V		TYPICAL AC	TYPICAL ACT	UNIT
t_{PLH}/ t_{PHL}	Propagation delay D_n to $\overline{Q}_n$	C_L = 50pF		4.1	5.8	ns
C_{PD}	Power dissipation capacitance per buffer[1]	f = 1MHz; C_L = 50pF	Enabled	21	23	pF
			Disabled	8	8	
C_{IN}	Input capacitance	V_I = 0V or V_{CC}		4.5	4.5	pF
C_{OUT}	Output capacitance	V_O = 0V or V_{CC}; Disabled		10	10	pF
I_{LATCH}	Latch-up current	Per Jedec JC40.2 Standard 17		500	500	mA

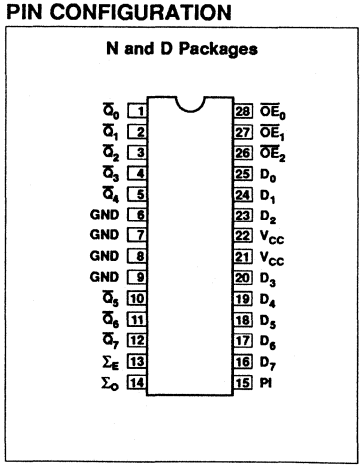
Note:

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_I + \Sigma (C_L \times V_{CC}^2 \times f_O)$ where:
   f_I = input frequency in MHz, C_L = output load capacitance in pF,
   f_O = output frequency in MHz, V_{CC} = supply voltage in V,
   $\Sigma (C_L \times V_{CC}^2 \times f_O)$ = sum of outputs

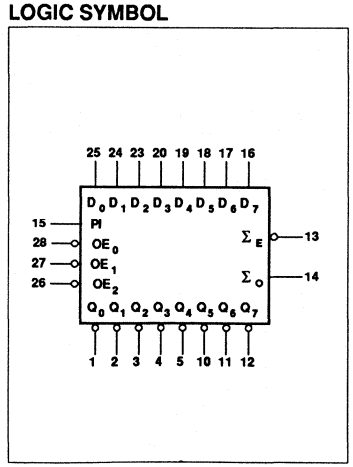
ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE
28-pin plastic DIP (300mil-wide)	-40°C to +85°C	74AC11655N 74ACT11655N
28-pin plastic SO (300mil-wide)	-40°C to +85°C	74AC11655D 74ACT11655D

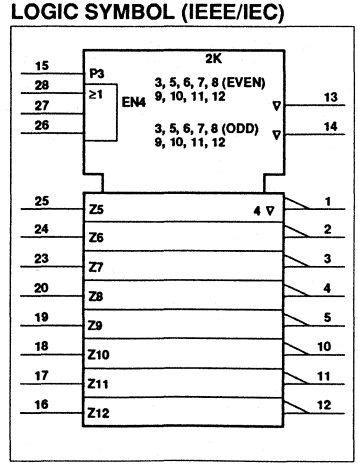
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



Octal Buffer/Line Driver with 9-Bit Parity Checker/Generator (3-State), INV

74AC/ACT11655

PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
15	PI	Parity input
28, 27, 26	$\overline{OE}_0$, $\overline{OE}_1$, $\overline{OE}_2$	Output enable input (active-Low)
25, 24, 23, 20, 19, 18, 17, 16	D_0 - D_7	Data inputs
1, 2, 3, 4, 5, 10, 11, 12	$\overline{Q}_0$ - $\overline{Q}_7$	Data outputs
13, 14	Σ_E, Σ_O	Parity outputs
6, 7, 8, 9	GND	Ground (0V)
21, 22	V_{CC}	Positive supply voltage

FUNCTION TABLE

INPUTS				OUTPUTS
$\overline{OE}_0$	$\overline{OE}_1$	$\overline{OE}_2$	D_n	$\overline{Q}_n$
L	L	L	L	H
L	L	L	H	L
H	X	X	X	Z
X	H	X	X	Z
X	X	H	X	Z

H = High voltage level
L = Low voltage level
X = Don't care
Z = High-impedance state

INPUTS	PARITY OUTPUTS	
Number of inputs High (PI, D_0 - D_7)	Σ_E	Σ_O
EVEN—0, 2, 4, 6, 8	H	L
ODD—1, 3, 5, 7, 9	L	H
Any $\overline{OE}$ = High	Z	Z

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	74AC11655			74ACT11655			UNIT
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	DC supply voltage	3.0[1]	5.0	5.5	4.5	5.0	5.5	V
V_I	Input voltage	0		V_{CC}	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	0		V_{CC}	V
$\Delta t/\Delta v$	Input transition rise or fall rate	0		10	0		10	ns/V
T_A	Operating free-air temperature	-40		+85	-40		+85	°C

NOTE:

1. No electrical or switching characteristics are specified at $V_{CC} < 3V$. Operation between 2V and 3V is not recommended, but within that range, a device output will maintain a previously established logic state.

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	TEST CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 to+7.0	V
I_{IK} or V_I	DC input diode current[2]	$V_I < 0$	-20	mA
		$V_I > V_{CC}$	20	
	DC input voltage		-0.5 to V_{CC} +0.5	V
I_{OK} or V_O	DC output diode current[2]	$V_O < 0$	-50	mA
		$V_O > V_{CC}$	50	
	DC output voltage		-0.5 to V_{CC} +0.5	V
I_O	DC output source or sink current per output pin	V_O = 0 to V_{CC}	±50	mA
I_{CC} or I_{GND}	DC V_{CC} current		±250	mA
	DC ground current		±250	
T_{STG}	Storage temperature		-65 to 150	°C
P_{TOT}	Power dissipation per package Plastic DIP	Above 70°C:derate linearly by 8mW/K	500	mW
	Power dissipation per package Plastic surface mount (SO)	Above 70°C:derate linearly by 6mW/K	400	mW

NOTES:

1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		V_{CC}	74AC11655				74ACT11655				UNIT
					T_A = +25°C		T_A = -40°C to +85°C		T_A = +25°C		T_A = -40°C to +85°C		
				V	Min	Max	Min	Max	Min	Max	Min	Max	
V_{IH}	High-level input voltage			3.0	2.10		2.10						V
				4.5	3.15		3.15		2.0		2.0		
				5.5	3.85		3.85		2.0		2.0		
V_{IL}	Low-level input voltage			3.0		0.90		0.90					V
				4.5		1.35		1.35		0.8		0.8	
				5.5		1.65		1.65		0.8		0.8	
V_{OH}	High-level output voltage	V_I = V_{IL} or V_{IH}	I_{OH} = -50μA	3.0	2.9		2.9						V
				4.5	4.4		4.4		4.4		4.4		
				5.5	5.4		5.4		5.4		5.4		
			I_{OH} = -4mA	3.0	2.58		2.48						
			I_{OH} = -24mA	4.5	3.94		3.8		3.94		3.8		
				5.5	4.94		4.8		4.94		4.8		
			I_{OH} = -75mA[1]	5.5			3.85				3.85		
V_{OL}	Low-level output voltage	V_I = V_{IL} or V_{IH}	I_{OL} = 50μA	3.0		0.1		0.1					V
				4.5		0.1		0.1		0.1		0.1	
				5.5		0.1		0.1		0.1		0.1	
			I_{OL} = 12mA	3.0		0.36		0.44					
			I_{OL} = 24mA	4.5		0.36		0.44		0.36		0.44	
				5.5		0.36		0.44		0.36		0.44	
			I_{OL} = 75mA[1]	5.5				1.65				1.65	
I_I	Input leakage current	V_I = V_{CC} or GND		5.5		±0.1		±1.0		±0.1		±1.0	μA
I_{OZ}	3-State output off-state current	V_I = V_{IL} or V_{IH}, V_O = V_{CC} or GND		5.5		±0.5		±5.0		±0.5		±5.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC} or GND, I_O = 0		5.5		8.0		80		8.0		80	μA
ΔI_{CC}	Supply current, TTL inputs High[2]	One input at 3.4V, other inputs at V_{CC} or GND		5.5						0.9		1.0	mA

NOTES:
1. Not more than one output should be tested at a time, and the duration of the test should not exceed 10ms.
2. This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0V or V_{CC}.

74AC/ACT11656

Octal Buffer/Line Driver with 9-Bit Parity Checker/Generator (3-State)

Objective Specification

FEATURES

- **3-State outputs**
- **Combines '244 and '280 functions in one package**
- **Output capability: ±24 mA**
- **CMOS (AC) and TTL (ACT) voltage level inputs**
- **50Ω incident wave switching**
- **Center-pin V_{CC} and ground configuration to minimize high-speed switching noise**
- **I_{CC} category: MSI**

DESCRIPTION

The 74AC/ACT11656 high-performance CMOS devices combine very high speed and high output drive comparable to the most advanced TTL families.

The 74AC/ACT11656 device is an octal buffer and line driver with parity generator/checker designed for use with memory address drivers, clock drivers, and bus-oriented transmitters/receivers.

GENERAL INFORMATION

SYMBOL	PARAMETER	CONDITIONS T_A = 25°C; GND = 0V; V_{CC} = 5.0V		TYPICAL AC	TYPICAL ACT	UNIT
t_{PLH}/t_{PHL}	Propagation delay D_n to Q_n	C_L = 50pF		4.4	5.6	ns
C_{PD}	Power dissipation capacitance per buffer[1]	f = 1MHz; C_L = 50pF	Enabled	22	23	pF
			Disabled	8	8	
C_{IN}	Input capacitance	V_I = 0V or V_{CC}		4.5	4.5	pF
C_{OUT}	Output capacitance	V_O = 0V or V_{CC}; Disabled		10	10	pF
I_{LATCH}	Latch-up current	Per Jedec JC40.2 Standard 17		500	500	mA

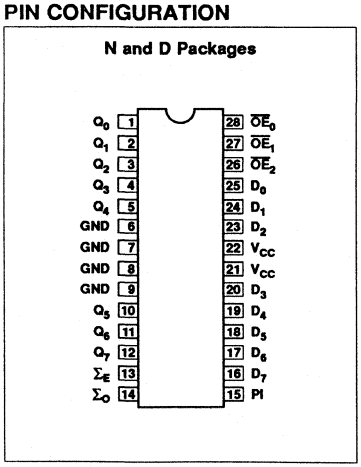
Note:

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_I + \Sigma (C_L \times V_{CC}^2 \times f_O)$ where:
   f_I = input frequency in MHz, C_L = output load capacitance in pF,
   f_O = output frequency in MHz, V_{CC} = supply voltage in V,
   $\Sigma (C_L \times V_{CC}^2 \times f_O)$ = sum of outputs

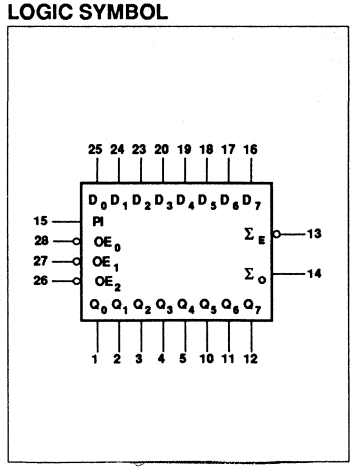
ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE
28-pin plastic DIP (300mil-wide)	-40°C to +85°C	74AC11656N 74ACT11656N
28-pin plastic SO (300mil-wide)	-40°C to +85°C	74AC11656D 74ACT11656D

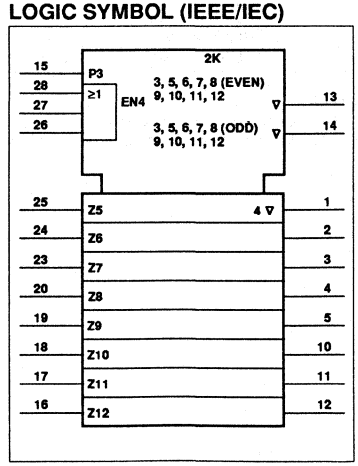
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



Octal Buffer/Line Driver with 9-Bit Parity Checker/Generator (3-State)

PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
15	PI	Parity input
28, 27, 26	$\overline{OE}_0$, $\overline{OE}_1$, $\overline{OE}_2$	Output enable input (active-Low)
25, 24, 23, 20, 19, 18, 17, 16	D_0 - D_7	Data inputs
1, 2, 3, 4, 5, 10, 11, 12	Q_0 - Q_7	Data outputs
13, 14	Σ_E, Σ_O	Parity outputs
6, 7, 8, 9	GND	Ground (0V)
21, 22	V_{CC}	Positive supply voltage

FUNCTION TABLE

INPUTS				OUTPUTS
$\overline{OE}_0$	$\overline{OE}_1$	$\overline{OE}_2$	D_n	Q_n
L	L	L	L	L
L	L	L	H	H
H	X	X	X	Z
X	H	X	X	Z
X	X	H	X	Z

H = High voltage level
L = Low voltage level
X = Don't care
Z = High-impedance state

INPUTS	PARITY OUTPUTS	
Number of inputs High (PI, D_0 - D_7)	Σ_E	Σ_O
EVEN—0, 2, 4, 6, 8	H	L
ODD—1, 3, 5, 7, 9	L	H
Any $\overline{OE}$ = High	Z	Z

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	74AC11656			74ACT11656			UNIT
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	DC supply voltage	3.0[1]	5.0	5.5	4.5	5.0	5.5	V
V_I	Input voltage	0		V_{CC}	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	0		V_{CC}	V
$\Delta t/\Delta v$	Input transition rise or fall rate	0		10	0		10	ns/V
T_A	Operating free-air temperature	-40		+85	-40		+85	°C

NOTE:

1. No electrical or switching characteristics are specified at V_{CC} < 3V. Operation between 2V and 3V is not recommended, but within that range, a device output will maintain a previously established logic state.

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	TEST CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 to+7.0	V
I_{IK} or V_I	DC input diode current[2]	$V_I < 0$	-20	mA
		$V_I > V_{CC}$	20	
	DC input voltage		-0.5 to V_{CC} +0.5	V
I_{OK} or V_O	DC output diode current[2]	$V_O < 0$	-50	mA
		$V_O > V_{CC}$	50	
	DC output voltage		-0.5 to V_{CC} +0.5	V
I_O	DC output source or sink current per output pin	V_O = 0 to V_{CC}	±50	mA
I_{CC} or I_{GND}	DC V_{CC} current		±250	mA
	DC ground current		±250	
T_{STG}	Storage temperature		-65 to 150	°C
P_{TOT}	Power dissipation per package Plastic DIP	Above 70°C:derate linearly by 8mW/K	500	mW
	Power dissipation per package Plastic surface mount (SO)	Above 70°C:derate linearly by 6mW/K	400	mW

NOTES:

1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		V_{CC}	74AC11656				74ACT11656				UNIT
					T_A = +25°C		T_A = -40°C to +85°C		T_A = +25°C		T_A = -40°C to +85°C		
				V	Min	Max	Min	Max	Min	Max	Min	Max	
V_{IH}	High-level input voltage			3.0	2.10		2.10						V
				4.5	3.15		3.15		2.0		2.0		
				5.5	3.85		3.85		2.0		2.0		
V_{IL}	Low-level input voltage			3.0		0.90		0.90					V
				4.5		1.35		1.35		0.8		0.8	
				5.5		1.65		1.65		0.8		0.8	
V_{OH}	High-level output voltage	V_I = V_{IL} or V_{IH}	I_{OH} = -50μA	3.0	2.9		2.9						V
				4.5	4.4		4.4		4.4		4.4		
				5.5	5.4		5.4		5.4		5.4		
			I_{OH} = -4mA	3.0	2.58		2.48						
			I_{OH} = -24mA	4.5	3.94		3.8		3.94		3.8		
				5.5	4.94		4.8		4.94		4.8		
			I_{OH} = -75mA[1]	5.5			3.85				3.85		
V_{OL}	Low-level output voltage	V_I = V_{IL} or V_{IH}	I_{OL} = 50μA	3.0		0.1		0.1					V
				4.5		0.1		0.1		0.1		0.1	
				5.5		0.1		0.1		0.1		0.1	
			I_{OL} = 12mA	3.0		0.36		0.44					
			I_{OL} = 24mA	4.5		0.36		0.44		0.36		0.44	
				5.5		0.36		0.44		0.36		0.44	
			I_{OL} = 75mA[1]	5.5				1.65				1.65	
I_I	Input leakage current	V_I = V_{CC} or GND		5.5		±0.1		±1.0		±0.1		±1.0	μA
I_{OZ}	3-State output off-state current	V_I = V_{IL} or V_{IH}, V_O = V_{CC} or GND		5.5		±0.5		±5.0		±0.5		±5.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC} or GND, I_O = 0		5.5		8.0		80		8.0		80	μA
ΔI_{CC}	Supply current, TTL inputs High[2]	One input at 3.4V, other inputs at V_{CC} or GND		5.5						0.9		1.0	mA

NOTES:
1. Not more than one output should be tested at a time, and the duration of the test should not exceed 10ms.
2. This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0V or V_{CC}.

74AC/ACT11657

Octal Transceiver with 8-Bit Parity Checker/Generator

Objective Specification

FEATURES

- **3-State outputs**
- **Combines '245 and '280 functions in one package**
- **Output capability: ±24 mA**
- **CMOS (AC) and TTL (ACT) voltage level inputs**
- **50Ω incident wave switching**
- **Center-pin V_{CC} and ground configuration to minimize high-speed switching noise**
- **I_{CC} category: MSI**

DESCRIPTION

The 74AC/ACT11657 high-performance CMOS devices combine very high speed and high output drive comparable to the most advanced TTL families.

The 74AC/ACT11657 device is an octal transceiver featuring non-inverting buffers and an 8-bit parity generator/checker, and is intended for bus-oriented applications.

The Transmit/Receive (T/$\overline{R}$) input determines the direction of the data flow through the bidirectional transceivers. Transmit (active-High) enables data from A ports to B ports; Receive (active-Low) enables data from B ports to A ports.

GENERAL INFORMATION

SYMBOL	PARAMETER	CONDITIONS T_A = 25°C; GND = 0V; V_{CC} = 5.0V		TYPICAL AC	TYPICAL ACT	UNIT
t_{PLH}/ t_{PHL}	Propagation delay A_n to B_n	C_L = 50pF		4.2	5.2	ns
C_{PD}	Power dissipation capacitance per transceiver[1]	f = 1MHz; C_L = 50pF	Enabled	29	28	pF
			Disabled	8	8	
C_{IN}	Input capacitance	V_I = 0V or V_{CC}		4.5	4.5	pF
C_{OUT}	Output capacitance	V_O = 0V or V_{CC}; Disabled		10	10	pF
C_{IO}	I/O capacitance	$V_{I/O}$ = 0V or V_{CC}; Disabled		12	12	pF
I_{LATCH}	Latch-up current	Per Jedec JC40.2 Standard 17		500	500	mA

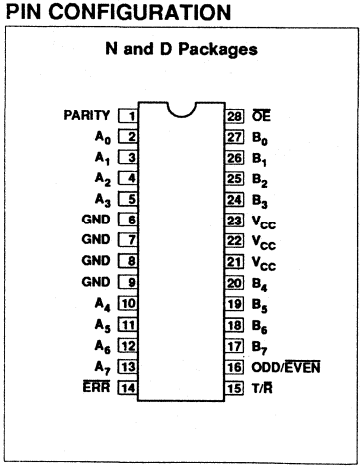
Note:

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_I + \Sigma (C_L \times V_{CC}^2 \times f_O)$ where:
   f_I = input frequency in MHz, C_L = output load capacitance in pF,
   f_O = output frequency in MHz, V_{CC} = supply voltage in V,
   $\Sigma (C_L \times V_{CC}^2 \times f_O)$ = sum of outputs

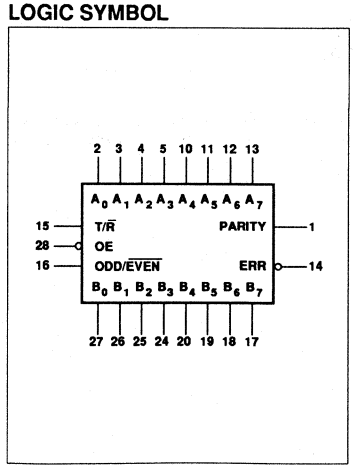
ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE
28-pin plastic DIP (300mil-wide)	-40°C to +85°C	74AC11657N 74ACT11657N
28-pin plastic SO (300mil-wide)	-40°C to +85°C	74AC11657D 74ACT11657D

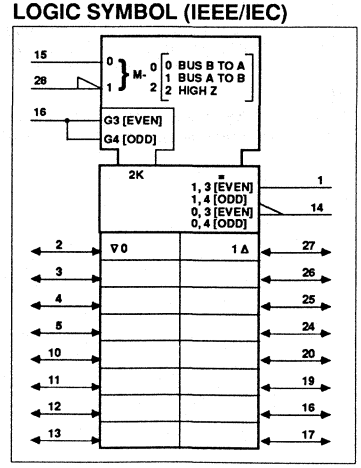
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



The Output Enable ($\overline{OE}$) input disables both the A and B ports by placing them in a high impedance condition when the $\overline{OE}$ input is High. The parity select (ODD/$\overline{EVEN}$) input gives the user the option of odd or even parity systems. The parity (PARITY) pin is an output from the generator/checker when transmitting from port A to B (T/$\overline{R}$ = High) and an input when receiving from port B to A (T/$\overline{R}$ = Low). When transmitting (T/$\overline{R}$ = High) the parity select (ODD/$\overline{EVEN}$) input is set, then the A port data is polled to determine the number of High bits. The parity (PARITY) output then goes to the logic state determined by the parity select (ODD/$\overline{EVEN}$) setting and by the number of High bits on port A. For example, if the parity select (ODD/$\overline{EVEN}$) is set Low (even parity), and the number of High bits on port A is odd, then the parity (PARITY) output will be High, transmitting even parity. If the number of High bits on port A is even, then the parity (PARITY) output will be Low, keeping even parity. When in receive mode (T/$\overline{R}$ = Low) the B port is polled to determine the number of High bits.

If parity select (ODD/$\overline{EVEN}$) is Low (even parity) and the number of Highs on port B is:

(1) odd and the parity (PARITY) input is High, then $\overline{ERR}$ will be High, signifying no error.

(2) even and the parity (PARITY) input is High, then $\overline{ERR}$ will be asserted Low, indicating an error.

PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
15	T/$\overline{R}$	Transmit/receive input
16	ODD/$\overline{EVEN}$	Parity select input
28	$\overline{OE}$	Output enable input (active-Low)
2, 3, 4, 5, 10, 11, 12, 13	A_0 - A_7	A ports 3-State inputs/output
27, 26, 25, 24, 20, 19, 18, 17	B_0 - B_7	B ports 3-State inputs/output
1	PARITY	Parity input/output
14	$\overline{ERR}$	Error output
6, 7, 8, 9	GND	Ground (0V)
21, 22, 23	V_{CC}	Positive supply voltage

FUNCTION TABLE

NUMBER OF INPUTS THAT ARE HIGH	INPUTS			INPUT/ OUTPUT	OUTPUTS	
	$\overline{OE}$	T/$\overline{R}$	ODD/$\overline{EVEN}$	PARITY	$\overline{ERR}$	OUTPUTS MODE
0, 2, 4, 6, 8	L	H	H	H	Z	Transmit
	L	H	L	L	Z	Transmit
	L	L	H	H	H	Receive
	L	L	H	L	L	Receive
	L	L	L	H	L	Receive
	L	L	L	L	H	Receive
1,3, 5, 7	L	H	H	L	Z	Transmit
	L	H	L	H	Z	Transmit
	L	L	H	H	L	Receive
	L	L	H	L	H	Receive
	L	L	L	H	H	Receive
	L	L	L	L	L	Receive
Don't care	H	X	X	Z	Z	Z

H = High voltage level
L = Low voltage level
X = Don't care
Z = High-impedance state

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	74AC11657			74ACT11657			UNIT
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	DC supply voltage	3.0[1]	5.0	5.5	4.5	5.0	5.5	V
V_I	Input voltage	0		V_{CC}	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	0		V_{CC}	V
$\Delta t/\Delta v$	Input transition rise or fall rate	0		10	0		10	ns/V
T_A	Operating free-air temperature	-40		+85	-40		+85	°C

NOTE:

1. No electrical or switching characteristics are specified at $V_{CC} < 3V$. Operation between 2V and 3V is not recommended, but within that range, a device output will maintain a previously established logic state.

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	TEST CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 to+7.0	V
I_{IK} or V_I	DC input diode current[2]	$V_I < 0$	-20	mA
		$V_I > V_{CC}$	20	
	DC input voltage		-0.5 to V_{CC} +0.5	V
I_{OK} or V_O	DC output diode current[2]	$V_O < 0$	-50	mA
		$V_O > V_{CC}$	50	
	DC output voltage		-0.5 to V_{CC} +0.5	V
I_O	DC output source or sink current per output pin	V_O = 0 to V_{CC}	±50	mA
I_{CC} or I_{GND}	DC V_{CC} current		±250	mA
	DC ground current		±250	
T_{STG}	Storage temperature		-65 to 150	°C
P_{TOT}	Power dissipation per package Plastic DIP	Above 70°C:derate linearly by 8mW/K	500	mW
	Power dissipation per package Plastic surface mount (SO)	Above 70°C:derate linearly by 6mW/K	400	mW

NOTES:

1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		V_{CC}	74AC11657				74ACT11657				UNIT
					T_A = +25°C		T_A = -40°C to +85°C		T_A = +25°C		T_A = -40°C to +85°C		
				V	Min	Max	Min	Max	Min	Max	Min	Max	
V_{IH}	High-level input voltage			3.0	2.10		2.10						V
				4.5	3.15		3.15		2.0		2.0		
				5.5	3.85		3.85		2.0		2.0		
V_{IL}	Low-level input voltage			3.0		0.90		0.90					V
				4.5		1.35		1.35		0.8		0.8	
				5.5		1.65		1.65		0.8		0.8	
V_{OH}	High-level output voltage	V_I = V_{IL} or V_{IH}	I_{OH} = -50µA	3.0	2.9		2.9						V
				4.5	4.4		4.4		4.4		4.4		
				5.5	5.4		5.4		5.4		5.4		
			I_{OH} = -4mA	3.0	2.58		2.48						
			I_{OH} = -24mA	4.5	3.94		3.8		3.94		3.8		
				5.5	4.94		4.8		4.94		4.8		
			I_{OH} = -75mA[1]	5.5			3.85				3.85		
V_{OL}	Low-level output voltage	V_I = V_{IL} or V_{IH}	I_{OL} = 50µA	3.0		0.1		0.1					V
				4.5		0.1		0.1		0.1		0.1	
				5.5		0.1		0.1		0.1		0.1	
			I_{OL} = 12mA	3.0		0.36		0.44					
			I_{OL} = 24mA	4.5		0.36		0.44		0.36		0.44	
				5.5		0.36		0.44		0.36		0.44	
			I_{OL} = 75mA[1]	5.5				1.65				1.65	
I_I	Input leakage current	V_I = V_{CC} or GND		5.5		±0.1		±1.0		±0.1		±1.0	µA
I_{OZ}	3-State output off-state current	V_I = V_{IL} or V_{IH}, V_O = V_{CC} or GND		5.5		±0.5		±5.0		±0.5		±5.0	µA
I_{CC}	Quiescent supply current	V_I = V_{CC} or GND, I_O = 0		5.5		8.0		80		8.0		80	µA
ΔI_{CC}	Supply current, TTL inputs High[2]	One input at 3.4V, other inputs at V_{CC} or GND		5.5						0.9		1.0	mA

NOTES:
1. Not more than one output should be tested at a time, and the duration of the test should not exceed 10ms.
2. This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0V or V_{CC}.

74AC/ACT11810

Quad 2-Input Exclusive-NOR Gate

Preliminary Specification

FEATURES

- **Output capability: ±24 mA**
- **CMOS (AC) and TTL (ACT) voltage level inputs**
- **50Ω incident wave switching**
- **Center-pin V_{CC} and ground configuration to minimize high-speed switching noise**
- **I_{CC} category: SSI**

DESCRIPTION

The 74AC/ACT11810 high-performance CMOS devices combine very high speed and high output drive comparable to the most advanced TTL families.

The 74AC/ACT11810 provides four separate 2-input exclusive-NOR gate functions.

GENERAL INFORMATION

SYMBOL	PARAMETER	CONDITIONS T_A = 25°C; GND = 0V; V_{CC} = 5.0V	TYPICAL		UNIT
			AC	ACT	
t_{PLH}/t_{PHL}	Propagation delay A, B, to $\overline{Y}$	C_L = 50pF	4.5	5.6	ns
C_{PD}	Power dissipation capacitance per gate[1]	f = 1MHz; C_L = 50pF	24	26	pF
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	3.5	3.5	pF
I_{LATCH}	Latch-up current	Per Jedec JC40.2 Standard 17	500	500	mA

Note:

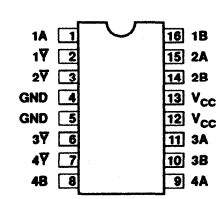
1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_I + \Sigma (C_L \times V_{CC}^2 \times f_O)$ where:
   f_I = input frequency in MHz, C_L = output load capacitance in pF,
   f_O = output frequency in MHz, V_{CC} = supply voltage in V,
   $\Sigma (C_L \times V_{CC}^2 \times f_O)$ = sum of outputs

ORDERING INFORMATION

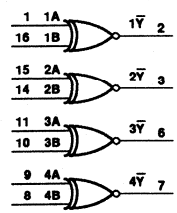
PACKAGES	TEMPERATURE RANGE	ORDER CODE
16-pin plastic DIP (300mil-wide)	-40°C to +85°C	74AC11810N 74ACT11810N
16-pin plastic SO (150mil-wide)	-40°C to +85°C	74AC11810D 74ACT11810D

PIN CONFIGURATION

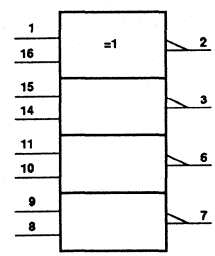
N and D Packages



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
1, 15, 11, 9	1A - 4A	Data inputs
16, 14, 10, 8	1B - 4B	Data inputs
2, 3, 6, 7	$1\overline{Y}$ - $4\overline{Y}$	Data outputs
4, 5	GND	Ground (0V)
12, 13	V_{CC}	Positive supply voltage

FUNCTION TABLE

INPUTS		OUTPUT
nA	nB	$n\overline{Y}$
L	L	H
L	H	L
H	L	L
H	H	H

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	74AC11810			74ACT11810			UNIT
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	DC supply voltage	3.0[1]	5.0	5.5	4.5	5.0	5.5	V
V_I	Input voltage	0		V_{CC}	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	0		V_{CC}	V
$\Delta t/\Delta v$	Input transition rise or fall rate	0		10	0		10	ns/V
T_A	Operating free-air temperature	-40		+85	-40		+85	°C

NOTE:
1. No electrical or switching characteristics are specified at V_{CC} < 3V. Operation between 2V and 3V is not recommended, but within that range, a device output will maintain a previously established logic state.

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	TEST CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 to+7.0	V
I_{IK} or V_I	DC input diode current[2]	$V_I < 0$	-20	mA
		$V_I > V_{CC}$	20	
	DC input voltage		-0.5 to V_{CC} +0.5	V
I_{OK} or V_O	DC output diode current[2]	$V_O < 0$	-50	mA
		$V_O > V_{CC}$	50	
	DC output voltage		-0.5 to V_{CC} +0.5	V
I_O	DC output source or sink current per output pin	V_O = 0 to V_{CC}	±50	mA
I_{CC} or I_{GND}	DC V_{CC} current		±100	mA
	DC ground current		±100	
T_{STG}	Storage temperature		-65 to 150	°C
P_{TOT}	Power dissipation per package Plastic DIP	Above 70°C:derate linearly by 8mW/K	500	mW
	Power dissipation per package Plastic surface mount (SO)	Above 70°C:derate linearly by 6mW/K	400	mW

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		V_{CC}	74AC11810				74ACT11810				UNIT
					T_A = +25°C		T_A = -40°C to +85°C		T_A = +25°C		T_A = -40°C to +85°C		
				V	Min	Max	Min	Max	Min	Max	Min	Max	
V_{IH}	High-level input voltage			3.0	2.10		2.10						V
				4.5	3.15		3.15		2.0		2.0		
				5.5	3.85		3.85		2.0		2.0		
V_{IL}	Low-level input voltage			3.0		0.90		0.90					V
				4.5		1.35		1.35		0.8		0.8	
				5.5		1.65		1.65		0.8		0.8	
V_{OH}	High-level output voltage	V_I = V_{IL} or V_{IH}	I_{OH} = -50μA	3.0	2.9		2.9						V
				4.5	4.4		4.4		4.4		4.4		
				5.5	5.4		5.4		5.4		5.4		
			I_{OH} = -4mA	3.0	2.58		2.48						
			I_{OH} = -24mA	4.5	3.94		3.8		3.94		3.8		
				5.5	4.94		4.8		4.94		4.8		
			I_{OH} = -75mA[1]	5.5			3.85				3.85		
V_{OL}	Low-level output voltage	V_I = V_{IL} or V_{IH}	I_{OL} = 50μA	3.0		0.1		0.1					V
				4.5		0.1		0.1		0.1		0.1	
				5.5		0.1		0.1		0.1		0.1	
			I_{OL} = 12mA	3.0		0.36		0.44					
			I_{OL} = 24mA	4.5		0.36		0.44		0.36		0.44	
				5.5		0.36		0.44		0.36		0.44	
			I_{OL} = 75mA[1]	5.5				1.65				1.65	
I_I	Input leakage current	V_I = V_{CC} or GND		5.5		±0.1		±1.0		±0.1		±1.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC} or GND, I_O = 0		5.5		4.0		40		4.0		40	μA
ΔI_{CC}	Supply current, TTL inputs High[2]	One input at 3.4V, other inputs at V_{CC} or GND		5.5						0.9		1.0	mA

NOTES:
1. Not more than one output should be tested at a time, and the duration of the test should not exceed 10ms.
2. This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0V or V_{CC}.

AC ELECTRICAL CHARACTERISTICS AT 3.3V ±0.3V

SYMBOL	PARAMETER	WAVEFORM	74AC11810					UNIT
			T_A = +25°C			T_A = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay nA, nB to n$\overline{Y}$	1	1.5 1.5	5.9 5.3	7.9 6.7	1.5 1.5	8.6 7.4	ns

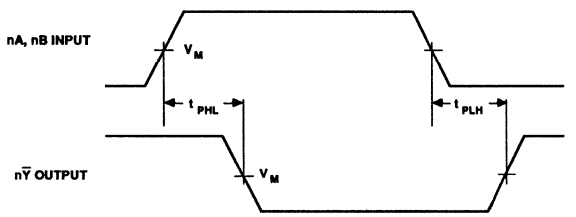
AC ELECTRICAL CHARACTERISTICS AT 5.0V ±0.5V

SYMBOL	PARAMETER	WAVEFORM	74AC11810					UNIT
			T_A = +25°C			T_A = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay nA, nB to n$\overline{Y}$	1	1.5 1.5	4.5 4.4	6.2 5.7	1.5 1.5	6.7 6.2	ns

AC ELECTRICAL CHARACTERISTICS AT 5.0V ±0.5V

SYMBOL	PARAMETER	WAVEFORM	74ACT11810					UNIT
			T_A = +25°C			T_A = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay nA, nB to n$\overline{Y}$	1	1.5 1.5	5.6 5.6	7.2 7.1	1.5 1.5	7.8 7.7	ns

AC WAVEFORMS

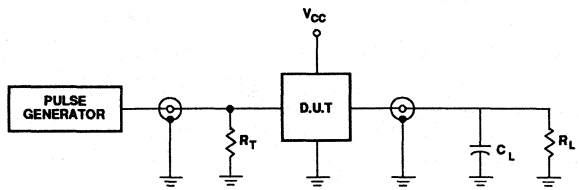


Waveform 1. Waveforms Showing the Input (nA, nB) to Output (n$\overline{Y}$) Propagation Delays

WAVEFORM CONDITIONS

	INPUTS	OUTPUTS
AC	V_{IN} = GND to V_{CC}, V_M = 50% V_{CC}	V_{OUT} = V_{OL} to V_{OH}
ACT	V_{IN} = GND to 3.0V, V_M = 1.5V	V_M = 50% V_{CC}

TEST CIRCUIT



Test Circuit

DEFINITIONS

C_L = Load capacitance, 50pF; includes jig and probe capacitance

R_L = Load resistor, 500Ω

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators

Input pulses: PRR ≤ 10MHz

$t_r = t_f$ = 3ns

74AC/ACT11818

8-Bit Diagnostic/Pipe-Line Register

Objective Specification

FEATURES

- **High-speed 8-bit parallel Output Register**
- **Serial diagnostic register with right-shift only**
- **Performs parallel-to-serial and serial to parallel conversion**
- **Output capability: ±24 mA**
- **CMOS (AC) and TTL (ACT) voltage level inputs**
- **50Ω incident wave switching**
- **Center-pin V_{CC} and ground configuration to minimize high-speed switching noise**
- **I_{CC} category: MSI**

DESCRIPTION

The 74AC/ACT11818 high-performance CMOS devices combine very high speed and high output drive comparable to the most advanced TTL families.

The 74AC/ACT11818 is a high-speed, general purpose pipeline register with an on-board diagnostic register for performing serial register diagnostics and write control store applications.

The D_n to Q_n path provides an 8-bit parallel data path pipeline register for normal system operation. The diagnostic register

GENERAL INFORMATION

SYMBOL	PARAMETER	CONDITIONS T_A = 25°C; GND = 0V V_{CC} = 5.0V		TYPICAL AC	TYPICAL ACT	UNIT
t_{PLH}/ t_{PHL}	Propagation delay PCP to Q_n	C_L = 50pF		5.4	5.6	ns
C_{PD}	Power dissipation capacitance[1]	f = 1MHz; C_L = 50pF	Enabled	17	17	pF
			Disabled	6	6	
C_{IN}	Input capacitance	V_I = 0V or V_{CC}		4.5	4.5	pF
C_{OUT}	Output capacitance	V_O = 0V or V_{CC}; Disabled		10	10	pF
$C_{I/O}$	I/O capacitance	$V_{I/O}$ = 0V or V_{CC}; Disabled		12	12	pF
I_{LATCH}	Latch-up current	Per Jedec JC40.2 Standard 17		500	500	mA
f_{MAX}	Maximum clock frequency	C_L = 50pF; V_{CC} = 5.5V		100	100	MHz

Note:

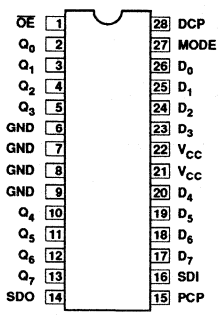
1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_I + \Sigma (C_L \times V_{CC}^2 \times f_O)$ where:
   f_I = input frequency in MHz, C_L = output load capacitance in pF,
   f_O = output frequency in MHz, V_{CC} = supply voltage in V,
   $\Sigma (C_L \times V_{CC}^2 \times f_O)$ = sum of outputs

ORDERING INFORMATION

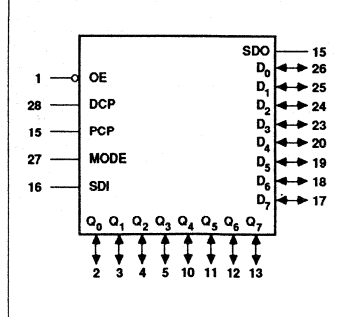
PACKAGES	TEMPERATURE RANGE	ORDER CODE
28-pin plastic DIP (300mil-wide)	-40°C to +85°C	74AC11818N 74ACT11818N
28-pin plastic SO (300mil-wide)	-40°C to +85°C	74AC11818D 74ACT11818D

PIN CONFIGURATION

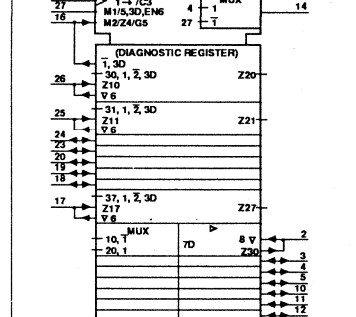
N and D Packages



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



can load parallel data to or from the pipe-line register and can output data through the D_n I/O port.

The 8-bit diagnostic register has multiplexer inputs that select parallel inputs from the Q_n port or adjacent bits in the diagnostic register to operate as a right-shift-only shift register. This register can then participate in a serial loop throughout the system where normal data, address, status, and control registers are replaced with the 74AC/ACT11818 Diagnostic Pipe-Line Registers. The loop can be used to scan in a complete test routine starting point (data, address, etc.). Then after a specified number of clock cycles, the data clocked out can be compared to the expected results. Write control store loading can be accomplished using the same technique. An instruction word can be serially shifted into the diagnostic register and written into a write control store RAM by enabling the D_n outputs.

PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
1	$\overline{OE}$	Output enable input (active Low)
28	DCP	Data (shadow register) clock
15	PCP	Pipe-line (output register) clock
27	MODE	Mode control input
16	SDI	Serial data control input
14	SDO	Serial data output
26, 25, 24, 23, 20, 19, 18, 17	D_0 - D_7	Data inputs/outputs
2,3, 4, 5, 10, 11, 12, 13	Q_0 - Q_7	Data inputs/outputs
6, 7, 8, 9	GND	Ground (0V)
21, 22	V_{CC}	Positive supply voltage

FUNCTION TABLE

INPUTS					OUTPUT AND I/O			STATUS
MODE	$\overline{OE}$	SDI	DCP	PCP	SDO	Q_0 - Q_7	D_0 - D_7	
L	X	X	↑	X	DR7*	—	Z	Serial input, shift right, disable D_0 - D_7
H	H	L	↑	X	SDI	INPUT	Z	Parallel load diagnostic register from Q_0 - Q_7, disable D_0 - D_7
H	L	L	↑	No↑	SDI	OUTPUT	Z	Parallel load diagnostic register from pipeline register, disable D_0 - D_7
L	X	X	X	↑	DR7*	—	INPUT†	Load pipeline register from D_0 - D_7
L	X	X	↑	↑	DR7*	—	INPUT†	Load pipeline register from D_0 - D_7 while shifting diagnostic register
H	X	X	No↑	↑	SDI	—	—	Load pipeline register from diagnostic register
H	X	X	X	X	SDI	—	—	Serial data in to serial data out
H	L	L	↑	↑	SDI	OUTPUT	Z	Exchange data between registers, D_0 - D_7 disabled
H	X	H	X	X	SDI	—	—	Hold diagnostic register, transitions on DCP do not effect diagnostic register
H	X	H	↑	X	SDI	—	OUTPUT	Enable D_0 - D_7 for parallel diagnostic register output

H = High voltage level
L = Low voltage level
↑ = Low-to-High clock transition
No↑ = Don't allow Low-to-High clock transition
X = Don't care
Z = High-impedance state

* Internal node corresponding to the 8th bit of the Diagnostic Register
† The D_0 - D_7 outputs must be disabled before applying data to D_0 - D_7.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	74AC11818			74ACT11818			UNIT
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	DC supply voltage	3.0[1]	5.0	5.5	4.5	5.0	5.5	V
V_I	Input voltage	0		V_{CC}	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	0		V_{CC}	V
$\Delta t/\Delta v$	Input transition rise or fall rate	0		10	0		10	ns/V
T_A	Operating free-air temperature	-40		+85	-40		+85	°C

NOTE:
1. No electrical or switching characteristics are specified at V_{CC} < 3V. Operation between 2V and 3V is not recommended, but within that range, a device output will maintain a previously established logic state.

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	TEST CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 to+7.0	V
I_{IK} or V_I	DC input diode current[2]	$V_I < 0$	-20	mA
		$V_I > V_{CC}$	20	
	DC input voltage		-0.5 to V_{CC} +0.5	V
I_{OK} or V_O	DC output diode current[2]	$V_O < 0$	-50	mA
		$V_O > V_{CC}$	50	
	DC output voltage		-0.5 to V_{CC} +0.5	V
I_O	DC output source or sink current per output pin	V_O = 0 to V_{CC}	±50	mA
I_{CC} or I_{GND}	DC V_{CC} current		±225	mA
	DC ground current		±225	
T_{STG}	Storage temperature		-65 to 150	°C
P_{TOT}	Power dissipation per package Plastic DIP	Above 70°C:derate linearly by 8mW/K	500	mW
	Power dissipation per package Plastic surface mount (SO)	Above 70°C:derate linearly by 6mW/K	400	mW

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		V_{CC}	74AC11818				74ACT11818				UNIT
					T_A = +25°C		T_A = -40°C to +85°C		T_A = +25°C		T_A = -40°C to +85°C		
				V	Min	Max	Min	Max	Min	Max	Min	Max	
V_{IH}	High-level input voltage			3.0	2.1		2.1						V
				4.5	3.15		3.15		2.0		2.0		
				5.5	3.85		3.85		2.0		2.0		
V_{IL}	Low-level input voltage			3.0		0.90		0.90					V
				4.5		1.35		1.35		0.8		0.8	
				5.5		1.65		1.65		0.8		0.8	
V_{OH}	High-level output voltage	V_I = V_{IL} or V_{IH}	I_{OH} = -50μA	3.0	2.9		2.9						V
				4.5	4.4		4.4		4.4		4.4		
				5.5	5.4		5.4		5.4		5.4		
			I_{OH} = -4mA	3.0	2.58		2.48						
			I_{OH} = -24mA	4.5	3.94		3.8		3.94		3.8		
				5.5	4.94		4.8		4.94		4.8		
			I_{OH} = -75mA[1]	5.5			3.85				3.85		
V_{OL}	Low-level output voltage	V_I = V_{IL} or V_{IH}	I_{OL} = 50μA	3.0		0.1		0.1					V
				4.5		0.1		0.1		0.1		0.1	
				5.5		0.1		0.1		0.1		0.1	
			I_{OL} = 12mA	3.0		0.36		0.44					
			I_{OL} = 24mA	4.5		0.36		0.44		0.36		0.44	
				5.5		0.36		0.44		0.36		0.44	
			I_{OL} = 75mA[1]	5.5				1.65				1.65	
I_I	Input leakage current	V_I = V_{CC} or GND		5.5		±0.1		±1.0		±0.1		±1.0	μA
I_{OZ}	3-State output off-state current	V_I = V_{IL} or V_{IH}, V_O = V_{CC} or GND		5.5		±0.5		±5.0		±0.5		±5.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC} or GND, I_O = 0		5.5		8.0		80		8.0		80	μA
ΔI_{CC}	Supply current, TTL inputs High[2]	One input at 3.4V, other inputs at V_{CC} or GND		5.5						0.9		1.0	mA

NOTES:
1. Not more than one output should be tested at a time, and the duration of the test should not exceed 10ms.
2. This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0V or V_{CC}.

74AC/ACT11819

8-Bit Diagnostic/Pipe-Line Register with Parity Even Output

Objective Specification

FEATURES

- **High-speed 8-bit parallel Output Register**
- **Serial shadow register with right-shift only**
- **Provides even-parity output**
- **Output capability: ±24 mA**
- **CMOS (AC) and TTL (ACT) voltage level inputs**
- **50Ω incident wave switching**
- **Center-pin V_{CC} and ground configuration to minimize high-speed switching noise**
- **I_{CC} category: MSI**

DESCRIPTION

The 74AC/ACT11819 high-performance CMOS devices combine very high speed and high output drive comparable to the most advanced TTL families.

The 74AC/ACT11819 is a high-speed, general purpose pipeline register with a parity even output and an on-board diagnostic register for performing serial register diagnostics and write control store applications.

The D_n to Q_n path provides an 8-bit parallel data path pipeline register for normal system operation. The diagnostic register

GENERAL INFORMATION

SYMBOL	PARAMETER	CONDITIONS T_A = 25°C; GND = 0V V_{CC} = 5.0V		TYPICAL AC	TYPICAL ACT	UNIT
t_{PLH}/ t_{PHL}	Propagation delay PCP to Q_n	C_L = 50pF		5.4	5.6	ns
C_{PD}	Power dissipation capacitance[1]	f = 1MHz; C_L = 50pF	Enabled	17	17	pF
			Disabled	6	6	
C_{IN}	Input capacitance	V_I = 0V or V_{CC}		4.5	4.5	pF
C_{OUT}	Output capacitance	V_O = 0V or V_{CC}; Disabled		10	10	pF
$C_{I/O}$	I/O capacitance	$V_{I/O}$ = 0V or V_{CC}; Disabled		12	12	pF
I_{LATCH}	Latch-up current	Per Jedec JC40.2 Standard 17		500	500	mA
f_{MAX}	Maximum clock frequency	C_L = 50pF; V_{CC} = 5.5V		100	100	MHz

Note:

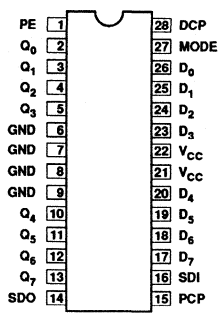
1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_O)$ where:
   f_i = input frequency in MHz, C_L = output load capacitance in pF,
   f_O = output frequency in MHz, V_{CC} = supply voltage in V,
   $\Sigma (C_L \times V_{CC}^2 \times f_O)$ = sum of outputs

ORDERING INFORMATION

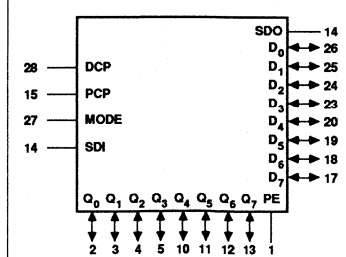
PACKAGES	TEMPERATURE RANGE	ORDER CODE
28-pin plastic DIP (300mil-wide)	-40°C to +85°C	74AC11819N 74ACT11819N
28-pin plastic SO (300mil-wide)	-40°C to +85°C	74AC11819D 74ACT11819D

PIN CONFIGURATION

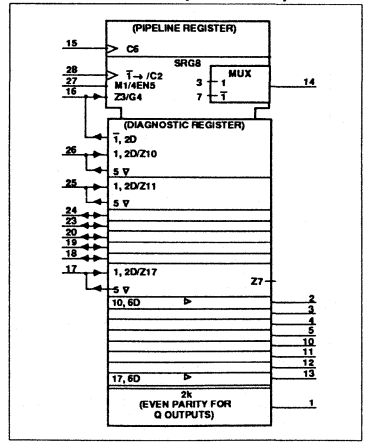
N and D Packages



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



8-Bit Diagnostic/Pipe-Line Register with Parity Even Output

74AC/ACT11819

can load parallel data to the pipeline register and can output data through the D_n I/O port.

The 8-bit diagnostic register has multiplexer inputs that select parallel inputs from the Q_n port or adjacent bits in the diagnostic register to operate as a right-shift-only shift register. This register can then participate in a serial loop throughout the system where normal data, address, status, and control registers are replaced with the 74AC/ACT11819 Diagnostic Pipe-Line Registers. The loop can be used to scan in a complete test routine starting point (data, address, etc.). Then after a specified number of clock cycles, the data clocked out can be compared to the expected results. Write control store loading can be accomplished using the same technique. An instruction word can be serially shifted into the diagnostic register and written into a write control store RAM by enabling the D_n outputs.

PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
28	DCP	Data (diagnostic register) clock
15	PCP	Pipe-line (output register) clock
27	MODE	Mode control input
16	SDI	Serial data control input
14	SDO	Serial data output
1	PE	Parity Even output
26, 25, 24, 23, 20, 19, 18, 17	D_0 - D_7	Data inputs/outputs
2,3, 4, 5, 10, 11, 12, 13	Q_0 - Q_7	Data outputs
6, 7, 8, 9	GND	Ground (0V)
21, 22	V_{CC}	Positive supply voltage

FUNCTION TABLE

INPUTS				OUTPUT AND I/O			STATUS
MODE	SDI	DCP	PCP	SDO	D_0 - D_7, PE	Q_0 - Q_7	
L	X	↑	X	DR7*	OUTPUT	Z	Serial input, shift right
H	L	↑	X	SDI (L)	OUTPUT	INPUT	Parallel load diagnostic register from Q_0 - Q
H	L	↑	↑	SDI (L)	OUTPUT	INPUT	Parallel load diagnostic register from pipeline register from D_0 - D_7
L X	X L	X X	↑ ↑	DR7*	OUTPUT	INPUT	Load pipeline register from D_0 - D_7
L	X	↑	↑	DR7*	OUTPUT	INPUT	Load pipeline register from D_0 - D_7 while shifting diagnostic register
H	H	No ↑	↑	SDI (H)	OUTPUT	OUTPUT	Load pipeline register from diagnostic register
H	X	X	X	SDI	OUTPUT	—	Serial data in to serial data out
H	H	X	X	SDI (H)	OUTPUT	OUTPUT HOLD	Hold diagnostic register, enable D_0 - D_7, transitions on DCP ignored
L X	X L	X X	X X	—	OUTPUT	Z	Disable D_0 - D_7 outputs

H = High voltage level
L = Low voltage level
↑ = Low-to-High clock transition
No ↑ = Don't allow Low-to-High clock transition
X = Don't care
Z = High-impedance state

* Internal node corresponding to the 8th bit of the Diagnostic Register

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	74AC11819			74ACT11819			UNIT
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	DC supply voltage	3.0[1]	5.0	5.5	4.5	5.0	5.5	V
V_I	Input voltage	0		V_{CC}	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	0		V_{CC}	V
$\Delta t/\Delta v$	Input transition rise or fall rate	0		10	0		10	ns/V
T_A	Operating free-air temperature	-40		+85	-40		+85	°C

NOTE:
1. No electrical or switching characteristics are specified at V_{CC} < 3V. Operation between 2V and 3V is not recommended, but within that range, a device output will maintain a previously established logic state.

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	TEST CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 to+7.0	V
I_{IK} or V_I	DC input diode current[2]	$V_I < 0$	-20	mA
		$V_I > V_{CC}$	20	
	DC input voltage		-0.5 to V_{CC} +0.5	V
I_{OK} or V_O	DC output diode current[2]	$V_O < 0$	-50	mA
		$V_O > V_{CC}$	50	
	DC output voltage		-0.5 to V_{CC} +0.5	V
I_O	DC output source or sink current per output pin	V_O = 0 to V_{CC}	±50	mA
I_{CC} or I_{GND}	DC V_{CC} current		±250	mA
	DC ground current		±250	
T_{STG}	Storage temperature		-65 to 150	°C
P_{TOT}	Power dissipation per package Plastic DIP	Above 70°C:derate linearly by 8mW/K	500	mW
	Power dissipation per package Plastic surface mount (SO)	Above 70°C:derate linearly by 6mW/K	400	mW

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		V_{CC}	74AC11819				74ACT11819				UNIT
					T_A = +25°C		T_A = -40°C to +85°C		T_A = +25°C		T_A = -40°C to +85°C		
				V	Min	Max	Min	Max	Min	Max	Min	Max	
V_{IH}	High-level input voltage			3.0	2.10		2.10						V
				4.5	3.15		3.15		2.0		2.0		
				5.5	3.85		3.85		2.0		2.0		
V_{IL}	Low-level input voltage			3.0		0.90		0.90					V
				4.5		1.35		1.35		0.8		0.8	
				5.5		1.65		1.65		0.8		0.8	
V_{OH}	High-level output voltage	V_I = V_{IL} or V_{IH}	I_{OH} = -50µA	3.0	2.9		2.9						V
				4.5	4.4		4.4		4.4		4.4		
				5.5	5.4		5.4		5.4		5.4		
			I_{OH} = -4mA	3.0	2.58		2.48						
			I_{OH} = -24mA	4.5	3.94		3.8		3.94		3.8		
				5.5	4.94		4.8		4.94		4.8		
			I_{OH} = -75mA[1]	5.5			3.85				3.85		
V_{OL}	Low-level output voltage	V_I = V_{IL} or V_{IH}	I_{OL} = 50µA	3.0		0.1		0.1					V
				4.5		0.1		0.1		0.1		0.1	
				5.5		0.1		0.1		0.1		0.1	
			I_{OL} = 12mA	3.0		0.36		0.44					
			I_{OL} = 24mA	4.5		0.36		0.44		0.36		0.44	
				5.5		0.36		0.44		0.36		0.44	
			I_{OL} = 75mA[1]	5.5				1.65				1.65	
I_I	Input leakage current	V_I = V_{CC} or GND		5.5		±0.1		±1.0		±0.1		±1.0	µA
I_{OZ}	3-State output off-state current	V_I = V_{IL} or V_{IH}, V_O = V_{CC} or GND		5.5		±0.5		±5.0		±0.5		±5.0	µA
I_{CC}	Quiescent supply current	V_I = V_{CC} or GND, I_O = 0		5.5		8.0		80		8.0		80	µA
ΔI_{CC}	Supply current, TTL inputs High[2]	One input at 3.4V, other inputs at V_{CC} or GND		5.5						0.9		1.0	mA

NOTES:
1. Not more than one output should be tested at a time, and the duration of the test should not exceed 10ms.
2. This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0V or V_{CC}.

74AC/ACT11821

10-Wide D-Type Flip-Flop; Positive-Edge Trigger; 3-State

Objective Specification

FEATURES

- **High-speed parallel registers with positive edge-triggered D-type flip-flops**
- **Extra data width for wide address/ data paths or buses with parity**
- **Output capability: ±24mA**
- **CMOS (AC) and TTL (ACT) voltage level inputs**
- **50Ω incident wave switching**
- **Center-pin V_{CC} and ground configuration to minimize high-speed switching noise**
- **I_{CC} category: MSI**

DESCRIPTION

The 74AC/ACT11821 high-performance CMOS devices combine very high speed and high output drive comparable to the most advanced TTL families.

The AC/ACT11821 Bus Interface Register is designed to eliminate the extra packages required to buffer existing registers and provides extra data width (10-wide) for the wider address/data paths or buses carrying parity.

GENERAL INFORMATION

SYMBOL	PARAMETER	CONDITIONS T_A = 25°C; GND = 0V; V_{CC} = 5.0V		TYPICAL AC	TYPICAL ACT	UNIT
t_{PLH}/t_{PHL}	Propagation delay CP to Q_n	C_L = 50pF		6.0	8.5	ns
C_{PD}	Power dissipation capacitance per flip-flop[1]	f = 1MHz; C_L = 50pF	Enabled	75	100	pF
			Disabled	65	80	
C_{IN}	Input capacitance	V_I = 0V or V_{CC}		4.5	4.5	pF
C_{OUT}	Output capacitance	V_O = 0V or V_{CC}; Disabled		10	10	pF
I_{LATCH}	Latch-up current	Per Jedec JC40.2 Standard 17		500	500	mA
f_{MAX}	Maximum clock frequency; CP to Q_n	C_L = 50pF		125	100	MHz

Note:

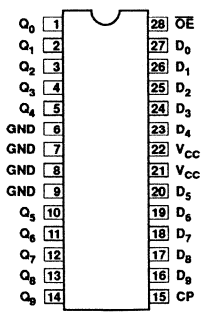
1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_O)$ where:
   f_i = input frequency in MHz, C_L = output load capacitance in pF,
   f_O = output frequency in MHz, V_{CC} = supply voltage in V,
   $\Sigma (C_L \times V_{CC}^2 \times f_O)$ = sum of outputs

ORDERING INFORMATION

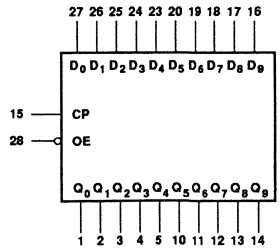
PACKAGES	TEMPERATURE RANGE	ORDER CODE
28-pin plastic DIP (300mil-wide)	-40°C to +85°C	74AC11821N 74ACT11821N
28-pin plastic SO (300mil-wide)	-40°C to +85°C	74AC11821D 74ACT11821D

PIN CONFIGURATION

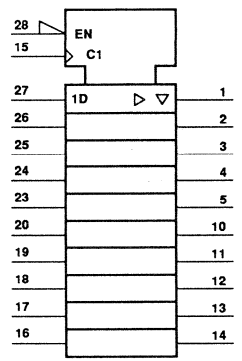
N and D Packages



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



PIN DESCRIPTION

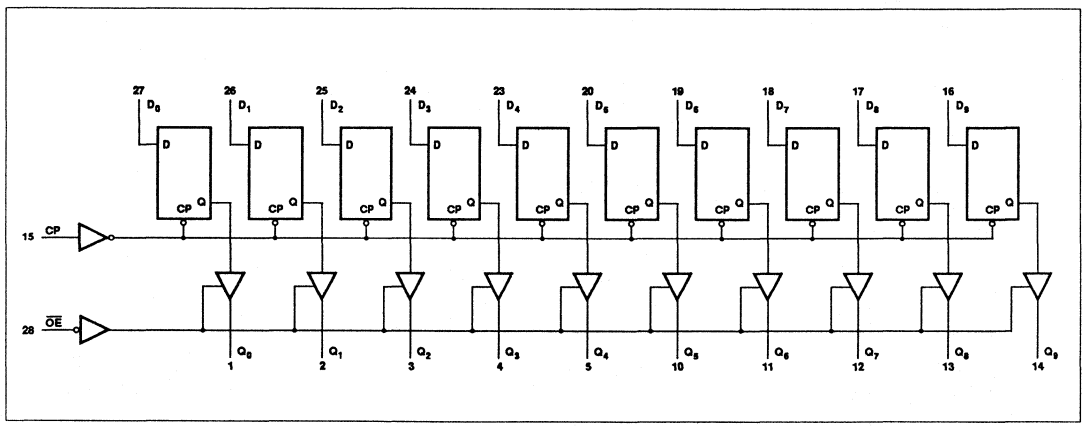
PIN NUMBER	SYMBOL	NAME AND FUNCTION
28	$\overline{OE}$	Output enable input (active-Low)
15	CP	Clock input
1, 2, 3, 4, 5, 10, 11, 12, 13, 14	D_0 - D_9	Data inputs
27, 26, 25, 24, 23, 20, 19, 18, 17, 16	Q_0 - Q_9	Data outputs
6, 7, 8, 9	GND	Ground (0V)
21, 22	V_{CC}	Positive supply voltage

FUNCTION TABLE

INPUTS			OUTPUTS
$\overline{OE}$	CP	D_n	Q_n
L	↑	l	L
L	↑	h	H
L	L	X	No change
L	H	X	No change
H	X	X	Z

H = High voltage levle
h = High voltage level one setup time prior to the Low-to-High clock transition
L = Low voltage levels
l = Low voltage level one setup time prior to the Low-to-High clock transition
X = Don't Care
↑ = Low-to-High clock transition

LOGIC DIAGRAM



RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	74AC11821			74ACT11821			UNIT
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	DC supply voltage	3.0[1]	5.0	5.5	4.5	5.0	5.5	V
V_I	Input voltage	0		V_{CC}	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	0		V_{CC}	V
$\Delta t/\Delta v$	Input transition rise or fall rate	0		10	0		10	ns/V
T_A	Operating free-air temperature	-40		+85	-40		+85	°C

NOTE:

1. No electrical or switching characteristics are specified at V_{CC} < 3V. Operation between 2V and 3V is not recommended, but within that range, a device output will maintain a previously established logic state.

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	TEST CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 to+7.0	V
I_{IK} or V_I	DC input diode current[2]	$V_I < 0$	-20	mA
		$V_I > V_{CC}$	20	
	DC input voltage		-0.5 to V_{CC} +0.5	V
I_{OK} or V_O	DC output diode current[2]	$V_O < 0$	-50	mA
		$V_O > V_{CC}$	50	
	DC output voltage		-0.5 to V_{CC} +0.5	V
I_O	DC output source or sink current per output pin	V_O = 0 to V_{CC}	±50	mA
I_{CC} or I_{GND}	DC V_{CC} current		±250	mA
	DC ground current		±250	
T_{STG}	Storage temperature		-65 to 150	°C
P_{TOT}	Power dissipation per package Plastic DIP	Above 70°C:derate linearly by 8mW/K	500	mW
	Power dissipation per package Plastic surface mount (SO)	Above 70°C:derate linearly by 6mW/K	400	mW

NOTES:

1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		V_{CC}	74AC11821				74ACT11821				UNIT
					T_A = +25°C		T_A = -40°C to +85°C		T_A = +25°C		T_A = -40°C to +85°C		
				V	Min	Max	Min	Max	Min	Max	Min	Max	
V_{IH}	High-level input voltage			3.0	2.10		2.10						V
				4.5	3.15		3.15		2.0		2.0		
				5.5	3.85		3.85		2.0		2.0		
V_{IL}	Low-level input voltage			3.0		0.90		0.90					V
				4.5		1.35		1.35		0.8		0.8	
				5.5		1.65		1.65		0.8		0.8	
V_{OH}	High-level output voltage	V_I = V_{IL} or V_{IH}	I_{OH} = -50μA	3.0	2.9		2.9						V
				4.5	4.4		4.4		4.4		4.4		
				5.5	5.4		5.4		5.4		5.4		
			I_{OH} = -4mA	3.0	2.58		2.48						
			I_{OH} = -24mA	4.5	3.94		3.8		3.94		3.8		
				5.5	4.94		4.8		4.94		4.8		
			I_{OH} = -75mA[1]	5.5			3.85				3.85		
V_{OL}	Low-level output voltage	V_I = V_{IL} or V_{IH}	I_{OL} = 50μA	3.0		0.1		0.1					V
				4.5		0.1		0.1		0.1		0.1	
				5.5		0.1		0.1		0.1		0.1	
			I_{OL} = 12mA	3.0		0.36		0.44					
			I_{OL} = 24mA	4.5		0.36		0.44		0.36		0.44	
				5.5		0.36		0.44		0.36		0.44	
			I_{OL} = 75mA[1]	5.5				1.65				1.65	
I_I	Input leakage current	V_I = V_{CC} or GND		5.5		±0.1		±1.0		±0.1		±1.0	μA
I_{OZ}	3-State output off-state current	V_I = V_{IL} or V_{IH}, V_O = V_{CC} or GND		5.5		±0.5		±5.0		±0.5		±5.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC} or GND, I_O = 0		5.5		8.0		80		8.0		80	μA
ΔI_{CC}	Supply current, TTL inputs High[2]	One input at 3.4V, other inputs at V_{CC} or GND		5.5						0.9		1.0	mA

NOTES:

1. Not more than one output should be tested at a time, and the duration of the test should not exceed 10ms.
2. This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0V or V_{CC}.

74AC/ACT11822

10-Wide D-Type Flip-Flop; Positive-Edge Trigger; 3-State; INV

Objective Specification

FEATURES

- **High-speed parallel registers with positive edge-triggered D-type flip-flops**
- **Extra data width for wide address/ data paths or buses with parity**
- **Output capability: ±24mA**
- **CMOS (AC) and TTL (ACT) voltage level inputs**
- **50Ω incident wave switching**
- **Center-pin V_{CC} and ground configuration to minimize high-speed switching noise**
- **I_{CC} category: MSI**

DESCRIPTION

The 74AC/ACT11822 high-performance CMOS devices combine very high speed and high output drive comparable to the most advanced TTL families.

The AC/ACT11822 Bus Interface Register is designed to eliminate the extra packages required to buffer existing registers and provides extra data width (10-wide) for the wider address/data paths or buses carrying parity.

GENERAL INFORMATION

SYMBOL	PARAMETER	CONDITIONS T_A = 25°C; GND = 0V; V_{CC} = 5.0V		TYPICAL AC	TYPICAL ACT	UNIT
t_{PLH}/t_{PHL}	Propagation delay CP to $\overline{Q}_n$	C_L = 50pF		6.0	8.5	ns
C_{PD}	Power dissipation capacitance per flip-flop[1]	f = 1MHz; C_L = 50pF	Enabled	75	100	pF
			Disabled	65	80	
C_{IN}	Input capacitance	V_I = 0V or V_{CC}		4.5	4.5	pF
C_{OUT}	Output capacitance	V_O = 0V or V_{CC}; Disabled		10	10	pF
I_{LATCH}	Latch-up current	Per Jedec JC40.2 Standard 17		500	500	mA
f_{MAX}	Maximum clock frequency; CP to $\overline{Q}_n$	C_L = 50pF		125	100	MHz

Note:

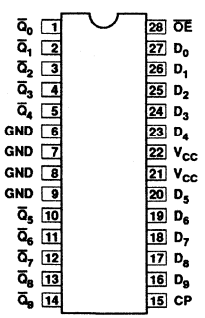
1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_I + \Sigma (C_L \times V_{CC}^2 \times f_O)$ where:
   f_I = input frequency in MHz, C_L = output load capacitance in pF,
   f_O = output frequency in MHz, V_{CC} = supply voltage in V,
   $\Sigma (C_L \times V_{CC}^2 \times f_O)$ = sum of outputs

ORDERING INFORMATION

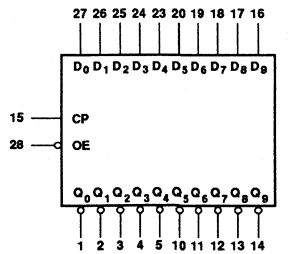
PACKAGES	TEMPERATURE RANGE	ORDER CODE
28-pin plastic DIP (300mil-wide)	-40°C to +85°C	74AC11822N 74ACT11822N
28-pin plastic SO (300mil-wide)	-40°C to +85°C	74AC11822D 74ACT11822D

PIN CONFIGURATION

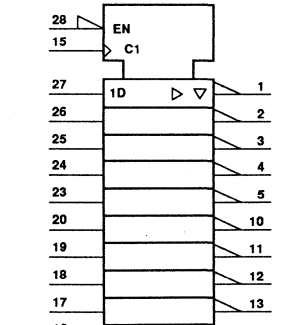
N and D Packages



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



10-Wide D-Type Flip-Flop; Positive-Edge Trigger; 3-State; INV

74AC/ACT11822

PIN DESCRIPTION

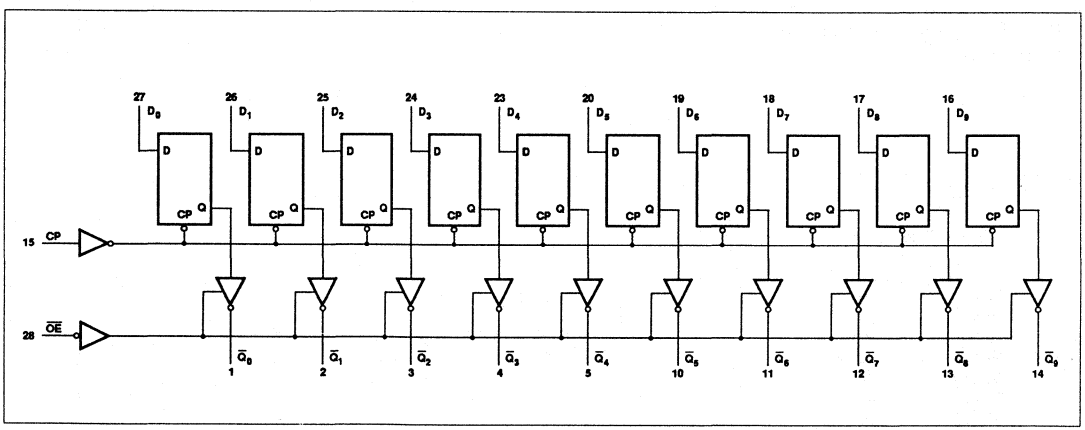
PIN NUMBER	SYMBOL	NAME AND FUNCTION
28	$\overline{OE}$	Output enable input (active-Low)
15	CP	Clock input
1, 2, 3, 4, 5, 10, 11, 12, 13, 14	D_0 - D_9	Data inputs
27, 26, 25, 24, 23, 20, 19, 18, 17, 16	$\overline{Q}_0$ - $\overline{Q}_9$	Data outputs
6, 7, 8, 9	GND	Ground (0V)
21, 22	V_{CC}	Positive supply voltage

FUNCTION TABLE

INPUTS			OUTPUTS
$\overline{OE}$	CP	D_n	$\overline{Q}_n$
L	↑	l	H
L	↑	h	L
L	L	X	No change
L	H	X	No change
H	X	X	Z

H = High voltage levle
h = High voltage level one setup time prior to the Low-to-High clock transition
L = Low voltage levels
l = Low voltage level one setup time prior to the Low-to-High clock transition
X = Don't Care
↑ = Low-to-High clock transition

LOGIC DIAGRAM



RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	74AC11822			74ACT11822			UNIT
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	DC supply voltage	3.0[1]	5.0	5.5	4.5	5.0	5.5	V
V_I	Input voltage	0		V_{CC}	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	0		V_{CC}	V
$\Delta t/\Delta v$	Input transition rise or fall rate	0		10	0		10	ns/V
T_A	Operating free-air temperature	-40		+85	-40		+85	°C

NOTE:

1. No electrical or switching characteristics are specified at $V_{CC} < 3V$. Operation between 2V and 3V is not recommended, but within that range, a device output will maintain a previously established logic state.

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	TEST CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 to+7.0	V
I_{IK} or V_I	DC input diode current[2]	$V_I < 0$	-20	mA
		$V_I > V_{CC}$	20	
	DC input voltage		-0.5 to V_{CC} +0.5	V
I_{OK} or V_O	DC output diode current[2]	$V_O < 0$	-50	mA
		$V_O > V_{CC}$	50	
	DC output voltage		-0.5 to V_{CC} +0.5	V
I_O	DC output source or sink current per output pin	V_O = 0 to V_{CC}	±50	mA
I_{CC} or I_{GND}	DC V_{CC} current		±250	mA
	DC ground current		±250	
T_{STG}	Storage temperature		-65 to 150	°C
P_{TOT}	Power dissipation per package Plastic DIP	Above 70°C:derate linearly by 8mW/K	500	mW
	Power dissipation per package Plastic surface mount (SO)	Above 70°C:derate linearly by 6mW/K	400	mW

NOTES:

1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		V_{CC}	74AC11822				74ACT11822				UNIT
					T_A = +25°C		T_A = -40°C to +85°C		T_A = +25°C		T_A = -40°C to +85°C		
				V	Min	Max	Min	Max	Min	Max	Min	Max	
V_{IH}	High-level input voltage			3.0	2.10		2.10						V
				4.5	3.15		3.15		2.0		2.0		
				5.5	3.85		3.85		2.0		2.0		
V_{IL}	Low-level input voltage			3.0		0.90		0.90					V
				4.5		1.35		1.35		0.8		0.8	
				5.5		1.65		1.65		0.8		0.8	
V_{OH}	High-level output voltage	V_I = V_{IL} or V_{IH}	I_{OH} = -50μA	3.0	2.9		2.9						V
				4.5	4.4		4.4		4.4		4.4		
				5.5	5.4		5.4		5.4		5.4		
			I_{OH} = -4mA	3.0	2.58		2.48						
			I_{OH} = -24mA	4.5	3.94		3.8		3.94		3.8		
				5.5	4.94		4.8		4.94		4.8		
			I_{OH} = -75mA[1]	5.5			3.85				3.85		
V_{OL}	Low-level output voltage	V_I = V_{IL} or V_{IH}	I_{OL} = 50μA	3.0		0.1		0.1					V
				4.5		0.1		0.1		0.1		0.1	
				5.5		0.1		0.1		0.1		0.1	
			I_{OL} = 12mA	3.0		0.36		0.44					
			I_{OL} = 24mA	4.5		0.36		0.44		0.36		0.44	
				5.5		0.36		0.44		0.36		0.44	
			I_{OL} = 75mA[1]	5.5				1.65				1.65	
I_I	Input leakage current	V_I = V_{CC} or GND		5.5		±0.1		±1.0		±0.1		±1.0	μA
I_{OZ}	3-State output off-state current	V_I = V_{IL} or V_{IH}; V_O = V_{CC} or GND		5.5		±0.5		±5.0		±0.5		±5.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC} or GND, I_O = 0		5.5		8.0		80		8.0		80	μA
ΔI_{CC}	Supply current, TTL inputs High[2]	One input at 3.4V, other inputs at V_{CC} or GND		5.5						0.9		1.0	mA

NOTES:
1. Not more than one output should be tested at a time, and the duration of the test should not exceed 10ms.
2. This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0V or V_{CC}.

74AC/ACT11823

9-Wide D-Type Flip-Flop with Reset and Enable; Positive-Edge Trigger; 3-State

Objective Specification

FEATURES

- **High-speed parallel registers with positive edge-triggered D-type flip-flops**
- **Extra data width for wide address/ data paths or buses with parity**
- **Output capability: ±24mA**
- **CMOS (AC) and TTL (ACT) voltage level inputs**
- **50Ω incident wave switching**
- **Center-pin V_{CC} and ground configuration to minimize high-speed switching noise**
- **I_{CC} category: MSI**

DESCRIPTION

The 74AC/ACT11823 high-performance CMOS devices combine very high speed and high output drive comparable to the most advanced TTL families.

The AC/ACT11823 is a 9-bit wide buffered register with Clock Enable and Master Reset which are ideal for parity bus interfacing in high-performance microprogrammed systems.

GENERAL INFORMATION

SYMBOL	PARAMETER	CONDITIONS T_A = 25°C; GND = 0V; V_{CC} = 5.0V		TYPICAL AC	TYPICAL ACT	UNIT
t_{PLH}/t_{PHL}	Propagation delay CP to Q_n	C_L = 50pF		6.0	8.5	ns
C_{PD}	Power dissipation capacitance per flip-flop[1]	f = 1MHz; C_L = 50pF	Enabled	75	100	pF
			Disabled	65	80	
C_{IN}	Input capacitance	V_I = 0V or V_{CC}		4.5	4.5	pF
C_{OUT}	Output capacitance	V_O = 0V or V_{CC}; Disabled		10	10	pF
I_{LATCH}	Latch-up current	Per Jedec JC40.2 Standard 17		500	500	mA
f_{MAX}	Maximum clock frequency; CP to Q_n	C_L = 50pF		125	100	MHz

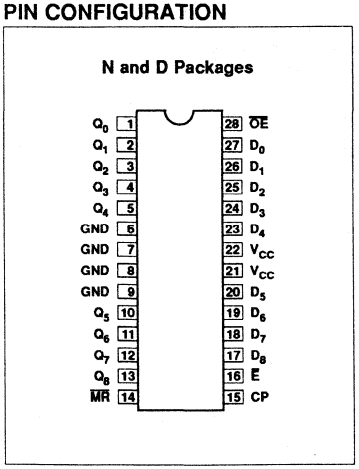
Note:

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_O)$ where:
   f_i = input frequency in MHz, C_L = output load capacitance in pF,
   f_O = output frequency in MHz, V_{CC} = supply voltage in V,
   $\Sigma (C_L \times V_{CC}^2 \times f_O)$ = sum of outputs

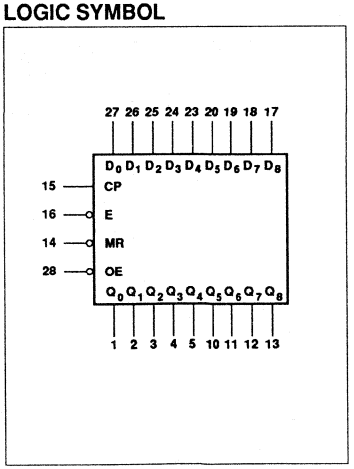
ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE
28-pin plastic DIP (300mil-wide)	-40°C to +85°C	74AC11823N 74ACT11823N
28-pin plastic SO (300mil-wide)	-40°C to +85°C	74AC11823D 74ACT11823D

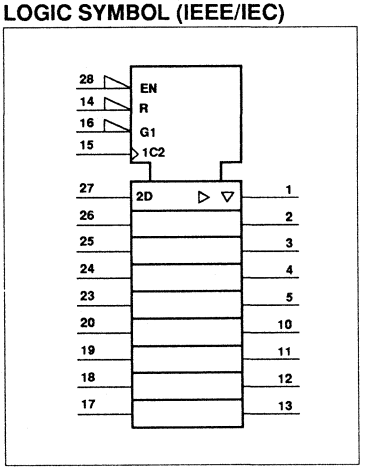
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



9-Wide D-Type Flip-Flop with Reset and Enable; Positive-Edge Trigger; 3-State

74AC/ACT11823

PIN DESCRIPTION

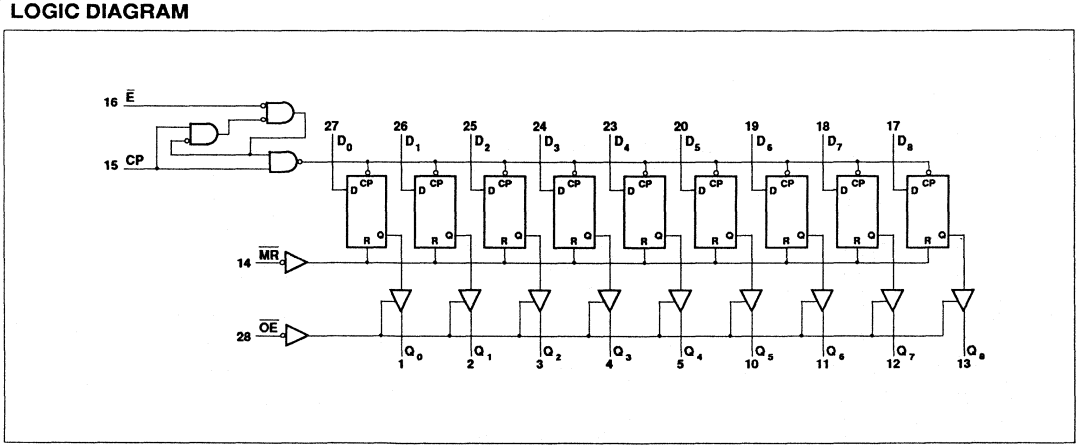
PIN NUMBER	SYMBOL	NAME AND FUNCTION
28	$\overline{OE}$	Output enable input (active-Low)
15	CP	Clock input
16	$\overline{E}$	Clock enable input (active-Low)
14	$\overline{MR}$	Master reset input (active-Low)
1, 2, 3, 4, 5, 10, 11, 12, 13	D_0 - D_8	Data inputs
27, 26, 25, 24, 23, 20, 19, 18, 17	Q_0 - Q_8	Data outputs
6, 7, 8, 9	GND	Ground (0V)
21, 22	V_{CC}	Positive supply voltage

FUNCTION TABLE

INPUTS					OUTPUTS
$\overline{OE}$	$\overline{MR}$	$\overline{E}$	CP	D_n	Q_n
L	L	X	X	X	L
L	H	L	↑	l	L
L	H	L	↑	h	H
L	H	H	X	X	No change
H	X	X	X	X	Z

H = High voltage levle
h = High voltage level one setup time prior to the Low-to-High clock transition
L = Low voltage levels
l = Low voltage level one setup time prior to the Low-to-High clock transition
X = Don't Care
↑ = Low-to-High clock transition

LOGIC DIAGRAM



RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	74AC11823			74ACT11823			UNIT
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	DC supply voltage	3.0[1]	5.0	5.5	4.5	5.0	5.5	V
V_I	Input voltage	0		V_{CC}	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	0		V_{CC}	V
$\Delta t/\Delta v$	Input transition rise or fall rate	0		10	0		10	ns/V
T_A	Operating free-air temperature	-40		+85	-40		+85	°C

NOTE:
1. No electrical or switching characteristics are specified at $V_{CC} < 3V$. Operation between 2V and 3V is not recommended, but within that range, a device output will maintain a previously established logic state.

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	TEST CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 to+7.0	V
I_{IK} or V_I	DC input diode current[2]	$V_I < 0$	-20	mA
		$V_I > V_{CC}$	20	
	DC input voltage		-0.5 to V_{CC} +0.5	V
I_{OK} or V_O	DC output diode current[2]	$V_O < 0$	-50	mA
		$V_O > V_{CC}$	50	
	DC output voltage		-0.5 to V_{CC} +0.5	V
I_O	DC output source or sink current per output pin	V_O = 0 to V_{CC}	±50	mA
I_{CC} or I_{GND}	DC V_{CC} current		±225	mA
	DC ground current		±225	
T_{STG}	Storage temperature		-65 to 150	°C
P_{TOT}	Power dissipation per package Plastic DIP	Above 70°C:derate linearly by 8mW/K	500	mW
	Power dissipation per package Plastic surface mount (SO)	Above 70°C:derate linearly by 6mW/K	400	mW

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		V_{CC}	74AC11823				74ACT11823				UNIT
					T_A = +25°C		T_A = -40°C to +85°C		T_A = +25°C		T_A = -40°C to +85°C		
				V	Min	Max	Min	Max	Min	Max	Min	Max	
V_{IH}	High-level input voltage			3.0	2.10		2.10						V
				4.5	3.15		3.15		2.0		2.0		
				5.5	3.85		3.85		2.0		2.0		
V_{IL}	Low-level input voltage			3.0		0.90		0.90					V
				4.5		1.35		1.35		0.8		0.8	
				5.5		1.65		1.65		0.8		0.8	
V_{OH}	High-level output voltage	V_I = V_{IL} or V_{IH}	I_{OH} = -50μA	3.0	2.9		2.9						V
				4.5	4.4		4.4		4.4		4.4		
				5.5	5.4		5.4		5.4		5.4		
			I_{OH} = -4mA	3.0	2.58		2.48						
			I_{OH} = -24mA	4.5	3.94		3.8		3.94		3.8		
				5.5	4.94		4.8		4.94		4.8		
			I_{OH} = -75mA[1]	5.5			3.85				3.85		
V_{OL}	Low-level output voltage	V_I = V_{IL} or V_{IH}	I_{OL} = 50μA	3.0		0.1		0.1					V
				4.5		0.1		0.1		0.1		0.1	
				5.5		0.1		0.1		0.1		0.1	
			I_{OL} = 12mA	3.0		0.36		0.44					
			I_{OL} = 24mA	4.5		0.36		0.44		0.36		0.44	
				5.5		0.36		0.44		0.36		0.44	
			I_{OL} = 75mA[1]	5.5				1.65				1.65	
I_I	Input leakage current	V_I = V_{CC} or GND		5.5		±0.1		±1.0		±0.1		±1.0	μA
I_{OZ}	3-State output off-state current	V_I = V_{IL} or V_{IH}, V_O = V_{CC} or GND		5.5		±0.5		±5.0		±0.5		±5.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC} or GND, I_O = 0		5.5		8.0		80		8.0		80	μA
ΔI_{CC}	Supply current, TTL inputs High[2]	One input at 3.4V, other inputs at V_{CC} or GND		5.5						0.9		1.0	mA

NOTES:

1. Not more than one output should be tested at a time, and the duration of the test should not exceed 10ms.
2. This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0V or V_{CC}.

74AC/ACT11824

9-Wide D-Type Flip-Flop with Reset and Enable; Positive-Edge Trigger; 3-State; INV

Objective Specification

FEATURES

- **High-speed parallel registers with positive edge-triggered D-type flip-flops**
- **Extra data width for wide address/ data paths or buses with parity**
- **Output capability: ±24mA**
- **CMOS (AC) and TTL (ACT) voltage level inputs**
- **50Ω incident wave switching**
- **Center-pin V_{CC} and ground configuration to minimize high-speed switching noise**
- **I_{CC} category: MSI**

DESCRIPTION

The 74AC/ACT11824 high-performance CMOS devices combine very high speed and high output drive comparable to the most advanced TTL families.

The AC/ACT11824 is a 9-bit wide buffered inverting register with Clock Enable and Master Reset which are ideal for parity bus interfacing in high-performance microprogrammed systems.

GENERAL INFORMATION

SYMBOL	PARAMETER	CONDITIONS T_A = 25°C; GND = 0V; V_{CC} = 5.0V		TYPICAL AC	TYPICAL ACT	UNIT
t_{PLH}/ t_{PHL}	Propagation delay CP to $\overline{Q}_n$	C_L = 50pF		6.0	8.5	ns
C_{PD}	Power dissipation capacitance per flip-flop[1]	f = 1MHz; C_L = 50pF	Enabled	75	100	pF
			Disabled	65	80	
C_{IN}	Input capacitance	V_I = 0V or V_{CC}		4.5	4.5	pF
C_{OUT}	Output capacitance	V_O = 0V or V_{CC}; Disabled		10	10	pF
I_{LATCH}	Latch-up current	Per Jedec JC40.2 Standard 17		500	500	mA
f_{MAX}	Maximum clock frequency; CP to $\overline{Q}_n$	C_L = 50pF		125	100	MHz

Note:

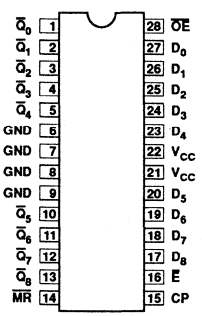
1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_I + \Sigma (C_L \times V_{CC}^2 \times f_O)$ where:
   f_I = input frequency in MHz, C_L = output load capacitance in pF,
   f_O = output frequency in MHz, V_{CC} = supply voltage in V,
   $\Sigma (C_L \times V_{CC}^2 \times f_O)$ = sum of outputs

ORDERING INFORMATION

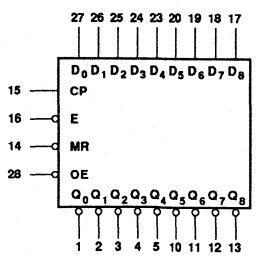
PACKAGES	TEMPERATURE RANGE	ORDER CODE
28-pin plastic DIP (300mil-wide)	-40°C to +85°C	74AC11824N 74ACT11824N
28-pin plastic SO (300mil-wide)	-40°C to +85°C	74AC11824D 74ACT11824D

PIN CONFIGURATION

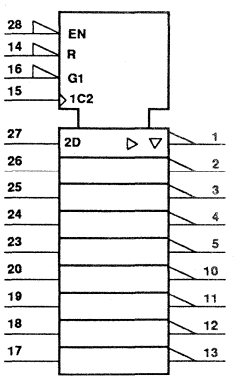
N and D Packages



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



PIN DESCRIPTION

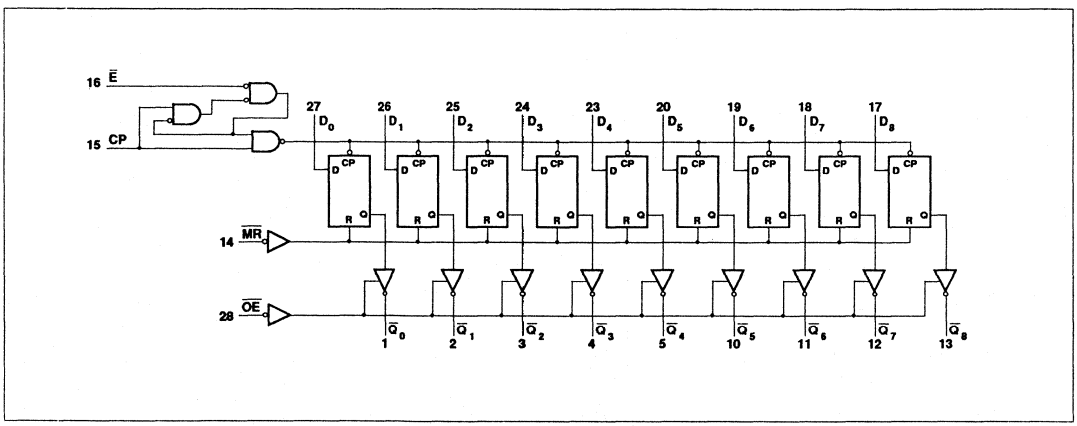
PIN NUMBER	SYMBOL	NAME AND FUNCTION
28	$\overline{OE}$	Output enable input (active-Low)
15	CP	Clock input
16	$\overline{E}$	Clock enable input (active-Low)
14	$\overline{MR}$	Master reset input (active-Low)
1, 2, 3, 4, 5, 10, 11, 12, 13	D_0 - D_8	Data inputs
27, 26, 25, 24, 23, 20, 19, 18, 17	$\overline{Q}_0$ - $\overline{Q}_8$	Data outputs
6, 7, 8, 9	GND	Ground (0V)
21, 22	V_{CC}	Positive supply voltage

FUNCTION TABLE

INPUTS					OUTPUTS
$\overline{OE}$	$\overline{MR}$	$\overline{E}$	CP	D_n	$\overline{Q}_n$
L	L	X	X	X	H
L	H	L	↑	l	H
L	H	L	↑	h	L
L	H	H	X	X	No change
H	X	X	X	X	Z

H = High voltage levle
h = High voltage level one setup time prior to the Low-to-High clock transition
L = Low voltage levels
l = Low voltage level one setup time prior to the Low-to-High clock transition
X = Don't Care
↑ = Low-to-High clock transition

LOGIC DIAGRAM



RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	74AC11824			74ACT11824			UNIT
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	DC supply voltage	3.0[1]	5.0	5.5	4.5	5.0	5.5	V
V_I	Input voltage	0		V_{CC}	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	0		V_{CC}	V
$\Delta t/\Delta v$	Input transition rise or fall rate	0		10	0		10	ns/V
T_A	Operating free-air temperature	-40		+85	-40		+85	°C

NOTE:

1. No electrical or switching characteristics are specified at V_{CC} < 3V. Operation between 2V and 3V is not recommended, but within that range, a device output will maintain a previously established logic state.

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	TEST CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 to+7.0	V
I_{IK} or V_I	DC input diode current[2]	$V_I < 0$	-20	mA
		$V_I > V_{CC}$	20	
	DC input voltage		-0.5 to V_{CC} +0.5	V
I_{OK} or V_O	DC output diode current[2]	$V_O < 0$	-50	mA
		$V_O > V_{CC}$	50	
	DC output voltage		-0.5 to V_{CC} +0.5	V
I_O	DC output source or sink current per output pin	V_O = 0 to V_{CC}	±50	mA
I_{CC} or I_{GND}	DC V_{CC} current		±225	mA
	DC ground current		±225	
T_{STG}	Storage temperature		-65 to 150	°C
P_{TOT}	Power dissipation per package Plastic DIP	Above 70°C:derate linearly by 8mW/K	500	mW
	Power dissipation per package Plastic surface mount (SO)	Above 70°C:derate linearly by 6mW/K	400	mW

NOTES:

1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		V_{CC}	74AC11824				74ACT11824				UNIT
					T_A = +25°C		T_A = -40°C to +85°C		T_A = +25°C		T_A = -40°C to +85°C		
				V	Min	Max	Min	Max	Min	Max	Min	Max	
V_{IH}	High-level input voltage			3.0	2.10		2.10						V
				4.5	3.15		3.15		2.0		2.0		
				5.5	3.85		3.85		2.0		2.0		
V_{IL}	Low-level input voltage			3.0		0.90		0.90					V
				4.5		1.35		1.35		0.8		0.8	
				5.5		1.65		1.65		0.8		0.8	
V_{OH}	High-level output voltage	V_I = V_{IL} or V_{IH}	I_{OH} = -50μA	3.0	2.9		2.9						V
				4.5	4.4		4.4		4.4		4.4		
				5.5	5.4		5.4		5.4		5.4		
			I_{OH} = -4mA	3.0	2.58		2.48						
			I_{OH} = -24mA	4.5	3.94		3.8		3.94		3.8		
				5.5	4.94		4.8		4.94		4.8		
			I_{OH} = -75mA[1]	5.5			3.85				3.85		
V_{OL}	Low-level output voltage	V_I = V_{IL} or V_{IH}	I_{OL} = 50μA	3.0		0.1		0.1					V
				4.5		0.1		0.1		0.1		0.1	
				5.5		0.1		0.1		0.1		0.1	
			I_{OL} = 12mA	3.0		0.36		0.44					
			I_{OL} = 24mA	4.5		0.36		0.44		0.36		0.44	
				5.5		0.36		0.44		0.36		0.44	
			I_{OL} = 75mA[1]	5.5				1.65				1.65	
I_I	Input leakage current	V_I = V_{CC} or GND		5.5		±0.1		±1.0		±0.1		±1.0	μA
I_{OZ}	3-State output off-state current	V_I = V_{IL} or V_{IH}, V_O = V_{CC} or GND		5.5		±0.5		±5.0		±0.5		±5.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC} or GND, I_O = 0		5.5		8.0		80		8.0		80	μA
ΔI_{CC}	Supply current, TTL inputs High[2]	One input at 3.4V, other inputs at V_{CC} or GND		5.5						0.9		1.0	mA

NOTES:
1. Not more than one output should be tested at a time, and the duration of the test should not exceed 10ms.
2. This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0V or V_{CC}.

74AC/ACT11825

Octal D-Type Flip-Flop with Reset and Enable; Positive-Edge Trigger; 3-State

Objective Specification

FEATURES

- **High-speed parallel registers with positive edge-triggered D-type flip-flops**
- **Output capability: ±24mA**
- **CMOS (AC) and TTL (ACT) voltage level inputs**
- **50Ω incident wave switching**
- **Center-pin V_{CC} and ground configuration to minimize high-speed switching noise**
- **I_{CC} category: MSI**

DESCRIPTION

The 74AC/ACT11825 high-performance CMOS devices combine very high speed and high output drive comparable to the most advanced TTL families.

The AC/ACT11825 is an 8-bit buffered register with Clock Enable, Master Reset, and multiple Enables ($\overline{OE}_0$, $\overline{OE}_1$, $\overline{OE}_2$) to allow multiuser control of the interface, e.g., CS, DMA, and RD/$\overline{WR}$.

GENERAL INFORMATION

SYMBOL	PARAMETER	CONDITIONS T_A = 25°C; GND = 0V; V_{CC} = 5.0V		TYPICAL AC	TYPICAL ACT	UNIT
t_{PLH}/t_{PHL}	Propagation delay CP to Q_n	C_L = 50pF		6.0	8.5	ns
C_{PD}	Power dissipation capacitance per flip-flop[1]	f = 1MHz; C_L = 50pF	Enabled	75	100	pF
			Disabled	65	80	
C_{IN}	Input capacitance	V_I = 0V or V_{CC}		4.5	4.5	pF
C_{OUT}	Output capacitance	V_O = 0V or V_{CC}; Disabled		10	10	pF
I_{LATCH}	Latch-up current	Per Jedec JC40.2 Standard 17		500	500	mA
f_{MAX}	Maximum clock frequency; CP to Q_n	C_L = 50pF		125	100	MHz

Note:

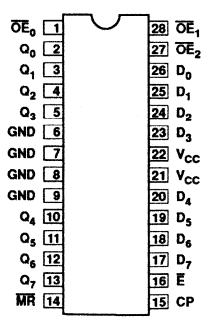
1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_I + \Sigma (C_L \times V_{CC}^2 \times f_O)$ where:
   f_I = input frequency in MHz, C_L = output load capacitance in pF,
   f_O = output frequency in MHz, V_{CC} = supply voltage in V,
   $\Sigma (C_L \times V_{CC}^2 \times f_O)$ = sum of outputs

ORDERING INFORMATION

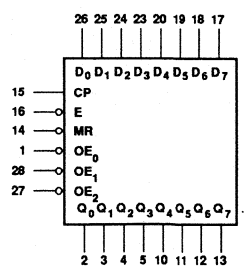
PACKAGES	TEMPERATURE RANGE	ORDER CODE
28-pin plastic DIP (300mil-wide)	-40°C to +85°C	74AC11825N 74ACT11825N
28-pin plastic SO (300mil-wide)	-40°C to +85°C	74AC11825D 74ACT11825D

PIN CONFIGURATION

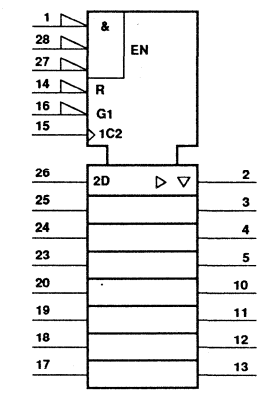
N and D Packages



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



PIN DESCRIPTION

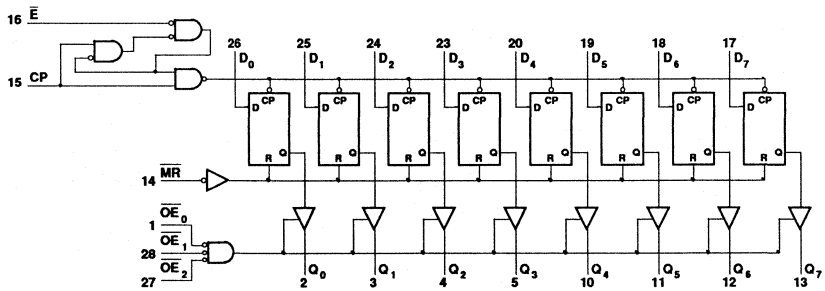
PIN NUMBER	SYMBOL	NAME AND FUNCTION
1, 28, 27	$\overline{OE}_0$, $\overline{OE}_1$, $\overline{OE}_2$	Output enable inputs (active-Low)
15	CP	Clock input
16	$\overline{E}$	Clock enable input (active-Low)
14	$\overline{MR}$	Master reset input (active-Low)
2, 3, 4, 5, 10, 11, 12, 13	D_0 - D_7	Data inputs
26, 25, 24, 23, 20, 19, 18, 17	Q_0 - Q_7	Data outputs
6, 7, 8, 9	GND	Ground (0V)
21, 22	V_{CC}	Positive supply voltage

FUNCTION TABLE

INPUTS					OUTPUTS
$\overline{OE}_n$	$\overline{MR}$	$\overline{E}$	CP	D_n	Q_n
L	L	X	X	X	L
L	H	L	↑	l	L
L	H	L	↑	h	H
L	H	H	X	X	No change
H	X	X	X	X	Z

H = High voltage levle
h = High voltage level one setup time prior to the Low-to-High clock transition
L = Low voltage levels
l = Low voltage level one setup time prior to the Low-to-High clock transition
X = Don't Care
↑ = Low-to-High clock transition

LOGIC DIAGRAM



RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	74AC11825			74ACT11825			UNIT
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	DC supply voltage	3.0[1]	5.0	5.5	4.5	5.0	5.5	V
V_I	Input voltage	0		V_{CC}	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	0		V_{CC}	V
$\Delta t/\Delta v$	Input transition rise or fall rate	0		10	0		10	ns/V
T_A	Operating free-air temperature	-40		+85	-40		+85	°C

NOTE:

1. No electrical or switching characteristics are specified at $V_{CC} < 3V$. Operation between 2V and 3V is not recommended, but within that range, a device output will maintain a previously established logic state.

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	TEST CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 to+7.0	V
I_{IK} or V_I	DC input diode current[2]	$V_I < 0$	-20	mA
		$V_I > V_{CC}$	20	
	DC input voltage		-0.5 to V_{CC} +0.5	V
I_{OK} or V_O	DC output diode current[2]	$V_O < 0$	-50	mA
		$V_O > V_{CC}$	50	
	DC output voltage		-0.5 to V_{CC} +0.5	V
I_O	DC output source or sink current per output pin	V_O = 0 to V_{CC}	±50	mA
I_{CC} or I_{GND}	DC V_{CC} current		±200	mA
	DC ground current		±200	
T_{STG}	Storage temperature		-65 to 150	°C
P_{TOT}	Power dissipation per package Plastic DIP	Above 70°C:derate linearly by 8mW/K	500	mW
	Power dissipation per package Plastic surface mount (SO)	Above 70°C:derate linearly by 6mW/K	400	mW

NOTES:

1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		V_{CC}	74AC11825				74ACT11825				UNIT
					T_A = +25°C		T_A = -40°C to +85°C		T_A = +25°C		T_A = -40°C to +85°C		
				V	Min	Max	Min	Max	Min	Max	Min	Max	
V_{IH}	High-level input voltage			3.0	2.10		2.10						V
				4.5	3.15		3.15		2.0		2.0		
				5.5	3.85		3.85		2.0		2.0		
V_{IL}	Low-level input voltage			3.0		0.90		0.90					V
				4.5		1.35		1.35		0.8		0.8	
				5.5		1.65		1.65		0.8		0.8	
V_{OH}	High-level output voltage	V_I = V_{IL} or V_{IH}	I_{OH} = -50μA	3.0	2.9		2.9						V
				4.5	4.4		4.4		4.4		4.4		
				5.5	5.4		5.4		5.4		5.4		
			I_{OH} = -4mA	3.0	2.58		2.48						
			I_{OH} = -24mA	4.5	3.94		3.8		3.94		3.8		
				5.5	4.94		4.8		4.94		4.8		
			I_{OH} = -75mA[1]	5.5			3.85				3.85		
V_{OL}	Low-level output voltage	V_I = V_{IL} or V_{IH}	I_{OL} = 50μA	3.0		0.1		0.1					V
				4.5		0.1		0.1		0.1		0.1	
				5.5		0.1		0.1		0.1		0.1	
			I_{OL} = 12mA	3.0		0.36		0.44					
			I_{OL} = 24mA	4.5		0.36		0.44		0.36		0.44	
				5.5		0.36		0.44		0.36		0.44	
			I_{OL} = 75mA[1]	5.5				1.65				1.65	
I_I	Input leakage current	V_I = V_{CC} or GND		5.5		±0.1		±1.0		±0.1		±1.0	μA
I_{OZ}	3-State output off-state current	V_I = V_{IL} or V_{IH}, V_O = V_{CC} or GND		5.5		±0.5		±5.0		±0.5		±5.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC} or GND, I_O = 0		5.5		8.0		80		8.0		80	μA
ΔI_{CC}	Supply current, TTL inputs High[2]	One input at 3.4V, other inputs at V_{CC} or GND		5.5						0.9		1.0	mA

NOTES:

1. Not more than one output should be tested at a time, and the duration of the test should not exceed 10ms.
2. This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0V or V_{CC}.

74AC/ACT11826

Octal D-Type Flip-Flop with Reset and Enable; Positive-Edge Trigger; 3-State; INV

Objective Specification

FEATURES

- **High-speed parallel registers with positive edge-triggered D-type flip-flops**
- **Output capability: ±24mA**
- **CMOS (AC) and TTL (ACT) voltage level inputs**
- **50Ω incident wave switching**
- **Center-pin V_{CC} and ground configuration to minimize high-speed switching noise**
- **I_{CC} category: MSI**

DESCRIPTION

The 74AC/ACT11826 high-performance CMOS devices combine very high speed and high output drive comparable to the most advanced TTL families.

The AC/ACT11826 is an 8-bit buffered inverting register with Clock Enable, Master Reset, and multiple Enables ($\overline{OE}_0$, $\overline{OE}_1$, $\overline{OE}_2$) to allow multiuser control of the interface, e.g., CS, DMA, and RD/$\overline{WR}$.

GENERAL INFORMATION

SYMBOL	PARAMETER	CONDITIONS T_A = 25°C; GND = 0V; V_{CC} = 5.0V		TYPICAL AC	TYPICAL ACT	UNIT
t_{PLH}/t_{PHL}	Propagation delay CP to $\overline{Q}_n$	C_L = 50pF		6.0	8.5	ns
C_{PD}	Power dissipation capacitance per flip-flop[1]	f = 1MHz; C_L = 50pF	Enabled	75	100	pF
			Disabled	65	80	
C_{IN}	Input capacitance	V_I = 0V or V_{CC}		4.5	4.5	pF
C_{OUT}	Output capacitance	V_O = 0V or V_{CC}; Disabled		10	10	pF
I_{LATCH}	Latch-up current	Per Jedec JC40.2 Standard 17		500	500	mA
f_{MAX}	Maximum clock frequency; CP to $\overline{Q}_n$	C_L = 50pF		125	100	MHz

Note:

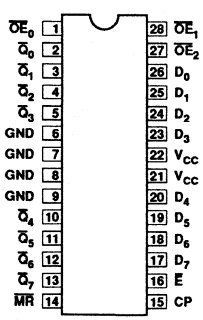
1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_I + \Sigma (C_L \times V_{CC}^2 \times f_O)$ where:
   f_I = input frequency in MHz, C_L = output load capacitance in pF,
   f_O = output frequency in MHz, V_{CC} = supply voltage in V,
   $\Sigma (C_L \times V_{CC}^2 \times f_O)$ = sum of outputs

ORDERING INFORMATION

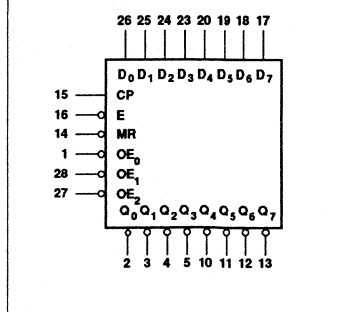
PACKAGES	TEMPERATURE RANGE	ORDER CODE
28-pin plastic DIP (300mil-wide)	-40°C to +85°C	74AC11826N 74ACT11826N
28-pin plastic SO (300mil-wide)	-40°C to +85°C	74AC11826D 74ACT11826D

PIN CONFIGURATION

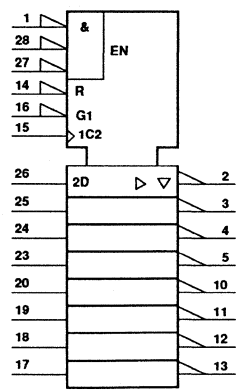
N and D Packages



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



Octal D-Type Flip-Flop with Reset and Enable; Positive-Edge Trigger; 3-State; INV

74AC/ACT11826

PIN DESCRIPTION

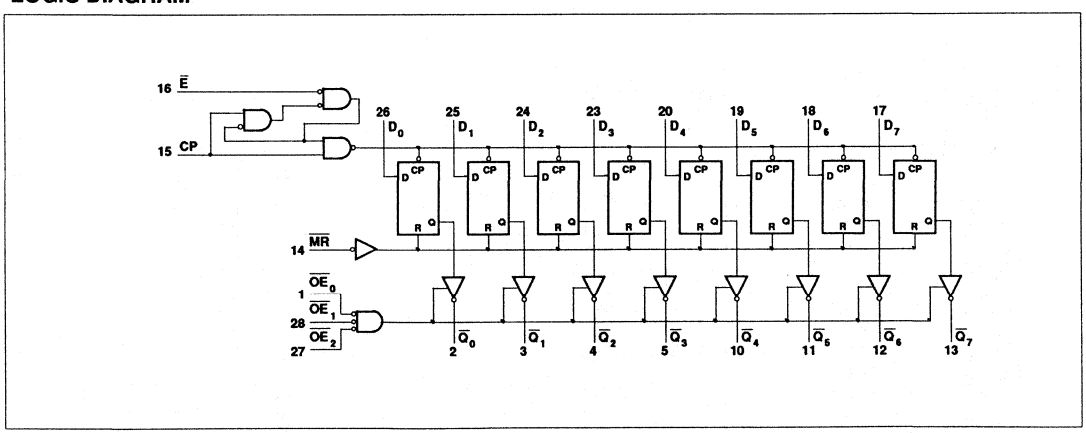
PIN NUMBER	SYMBOL	NAME AND FUNCTION
1, 28, 27	$\overline{OE}_0$, $\overline{OE}_1$, $\overline{OE}_2$	Output enable inputs (active-Low)
15	CP	Clock input
16	$\overline{E}$	Clock enable input (active-Low)
14	$\overline{MR}$	Master reset input (active-Low)
2, 3, 4, 5, 10, 11, 12, 13	D_0 - D_7	Data inputs
26, 25, 24, 23, 20, 19, 18, 17	$\overline{Q}_0$ - $\overline{Q}_7$	Data outputs
6, 7, 8, 9	GND	Ground (0V)
21, 22	V_{CC}	Positive supply voltage

FUNCTION TABLE

INPUTS					OUTPUTS
$\overline{OE}_n$	$\overline{MR}$	$\overline{E}$	CP	D_n	$\overline{Q}_n$
L	L	X	X	X	H
L	H	L	↑	l	H
L	H	L	↑	h	L
L	H	H	X	X	No change
H	X	X	X	X	Z

H = High voltage levle
h = High voltage level one setup time prior to the Low-to-High clock transition
L = Low voltage levels
l = Low voltage level one setup time prior to the Low-to-High clock transition
X = Don't Care
↑ = Low-to-High clock transition

LOGIC DIAGRAM



RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	74AC11826			74ACT11826			UNIT
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	DC supply voltage	3.0[1]	5.0	5.5	4.5	5.0	5.5	V
V_I	Input voltage	0		V_{CC}	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	0		V_{CC}	V
$\Delta t/\Delta v$	Input transition rise or fall rate	0		10	0		10	ns/V
T_A	Operating free-air temperature	-40		+85	-40		+85	°C

NOTE:
1. No electrical or switching characteristics are specified at V_{CC} < 3V. Operation between 2V and 3V is not recommended, but within that range, a device output will maintain a previously established logic state.

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	TEST CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 to+7.0	V
I_{IK} or V_I	DC input diode current[2]	$V_I < 0$	-20	mA
		$V_I > V_{CC}$	20	
	DC input voltage		-0.5 to V_{CC} +0.5	V
I_{OK} or V_O	DC output diode current[2]	$V_O < 0$	-50	mA
		$V_O > V_{CC}$	50	
	DC output voltage		-0.5 to V_{CC} +0.5	V
I_O	DC output source or sink current per output pin	V_O = 0 to V_{CC}	±50	mA
I_{CC} or I_{GND}	DC V_{CC} current		±200	mA
	DC ground current		±200	
T_{STG}	Storage temperature		-65 to 150	°C
P_{TOT}	Power dissipation per package Plastic DIP	Above 70°C:derate linearly by 8mW/K	500	mW
	Power dissipation per package Plastic surface mount (SO)	Above 70°C:derate linearly by 6mW/K	400	mW

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		V_{CC}	74AC11826				74ACT11826				UNIT
					T_A = +25°C		T_A = -40°C to +85°C		T_A = +25°C		T_A = -40°C to +85°C		
				V	Min	Max	Min	Max	Min	Max	Min	Max	
V_{IH}	High-level input voltage			3.0	2.10		2.10						V
				4.5	3.15		3.15		2.0		2.0		
				5.5	3.85		3.85		2.0		2.0		
V_{IL}	Low-level input voltage			3.0		0.90		0.90					V
				4.5		1.35		1.35		0.8		0.8	
				5.5		1.65		1.65		0.8		0.8	
V_{OH}	High-level output voltage	V_I = V_{IL} or V_{IH}	I_{OH} = -50μA	3.0	2.9		2.9						V
				4.5	4.4		4.4		4.4		4.4		
				5.5	5.4		5.4		5.4		5.4		
			I_{OH} = -4mA	3.0	2.58		2.48						
			I_{OH} = -24mA	4.5	3.94		3.8		3.94		3.8		
				5.5	4.94		4.8		4.94		4.8		
			I_{OH} = -75mA[1]	5.5			3.85				3.85		
V_{OL}	Low-level output voltage	V_I = V_{IL} or V_{IH}	I_{OL} = 50μA	3.0		0.1		0.1					V
				4.5		0.1		0.1		0.1		0.1	
				5.5		0.1		0.1		0.1		0.1	
			I_{OL} = 12mA	3.0		0.36		0.44					
			I_{OL} = 24mA	4.5		0.36		0.44		0.36		0.44	
				5.5		0.36		0.44		0.36		0.44	
			I_{OL} = 75mA[1]	5.5				1.65				1.65	
I_I	Input leakage current	V_I = V_{CC} or GND		5.5		±0.1		±1.0		±0.1		±1.0	μA
I_{OZ}	3-State output off-state current	V_I = V_{IL} or V_{IH}; V_O = V_{CC} or GND		5.5		±0.5		±5.0		±0.5		±5.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC} or GND, I_O = 0		5.5		8.0		80		8.0		80	μA
ΔI_{CC}	Supply current, TTL inputs High[2]	One input at 3.4V, other inputs at V_{CC} or GND		5.5						0.9		1.0	mA

NOTES:

1. Not more than one output should be tested at a time, and the duration of the test should not exceed 10ms.
2. This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0V or V_{CC}.

74AC/ACT11827

10-Wide Buffer/Line Driver; 3-State

Objective Specification

FEATURES

- **3-State buffers**
- **Output capability: ±24 mA**
- **CMOS (AC) and TTL (ACT) voltage level inputs**
- **50Ω incident wave switching**
- **Center-pin V_{CC} and ground configuration to minimize high-speed switching noise**
- **I_{CC} category: MSI**

DESCRIPTION

The 74AC/ACT11827 high-performance CMOS devices combine very high speed and high output drive comparable to the most advanced TTL families.

The 74AC/ACT11827 device is a 10-wide buffer/line driver and provides high performance bus interface buffering for wide data/address paths or busses carrying parity. It has NOR Output Enables ($\overline{OE}_0$, $\overline{OE}_1$) for maximum control flexibility.

GENERAL INFORMATION

SYMBOL	PARAMETER	CONDITIONS T_A = 25°C; GND = 0V; V_{CC} = 5.0V		TYPICAL AC	TYPICAL ACT	UNIT
t_{PLH}/t_{PHL}	Propagation delay A_n to Y_n	C_L = 50pF		5.3	6.6	ns
C_{PD}	Power dissipation capacitance per buffer[1]	f = 1MHz; C_L = 50pF	Enabled	38	39	pF
			Disabled	11	12	
C_{IN}	Input capacitance	V_I = 0V or V_{CC}		4.5	4.5	pF
C_{OUT}	Output capacitance	V_O = 0V or V_{CC}; Disabled		10	10	pF
I_{LATCH}	Latch-up current	Per Jedec JC40.2 Standard 17		500	500	mA

Note:

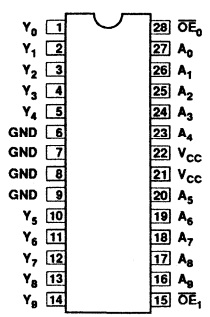
1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_I + \Sigma (C_L \times V_{CC}^2 \times f_O)$ where:
   f_I = input frequency in MHz, C_L = output load capacitance in pF,
   f_O = output frequency in MHz, V_{CC} = supply voltage in V,
   $\Sigma (C_L \times V_{CC}^2 \times f_O)$ = sum of outputs

ORDERING INFORMATION

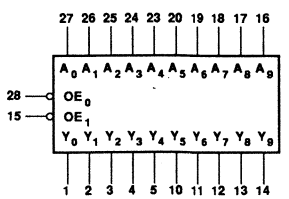
PACKAGES	TEMPERATURE RANGE	ORDER CODE
28-pin plastic DIP (300mil-wide)	-40°C to +85°C	74AC11827N 74ACT11827N
28-pin plastic SO (300mil-wide)	-40°C to +85°C	74AC11827D 74ACT11827D

PIN CONFIGURATION

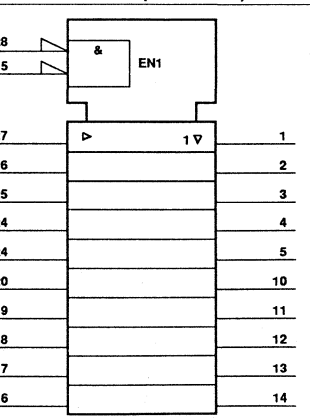
N and D Packages



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



PIN DESCRIPTION

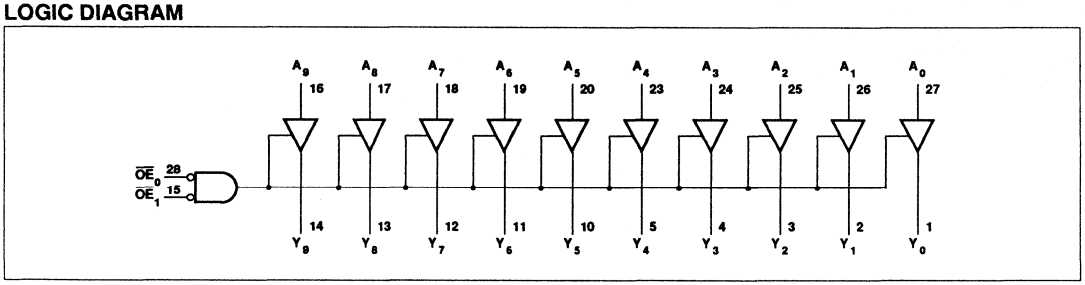
PIN NUMBER	SYMBOL	NAME AND FUNCTION
28, 15	$\overline{OE}_0$, $\overline{OE}_1$	Output enable input (active Low)
27, 26, 25, 24, 23, 20, 19, 18, 17, 16	A_0 - A_9	Data inputs
1, 2, 3, 4, 5, 10, 11, 12, 13, 14	Y_0 - Y_9	Data inputs
6, 7, 8, 9	GND	Ground (0V)
21, 22	V_{CC}	Positive supply voltage

FUNCTION TABLE

INPUTS		OUTPUTS
$\overline{OE}_n$	A_n	Y_n
L	L	L
L	H	H
H	X	Z

H = Highvoltage level
L = Low voltage level
X = Don't care
Z = High-impedance

LOGIC DIAGRAM



RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	74AC11827			74ACT11827			UNIT
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	DC supply voltage	3.0[1]	5.0	5.5	4.5	5.0	5.5	V
V_I	Input voltage	0		V_{CC}	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	0		V_{CC}	V
$\Delta t/\Delta v$	Input transition rise or fall rate	0		10	0		10	ns/V
T_A	Operating free-air temperature	-40		+85	-40		+85	°C

NOTE:

1. No electrical or switching characteristics are specified at V_{CC} < 3V. Operation between 2V and 3V is not recommended, but within that range, a device output will maintain a previously established logic state.

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	TEST CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 to+7.0	V
I_{IK} or V_I	DC input diode current[2]	$V_I < 0$	-20	mA
		$V_I > V_{CC}$	20	
	DC input voltage		-0.5 to V_{CC} +0.5	V
I_{OK} or V_O	DC output diode current[2]	$V_O < 0$	-50	mA
		$V_O > V_{CC}$	50	
	DC output voltage		-0.5 to V_{CC} +0.5	V
I_O	DC output source or sink current per output pin	V_O = 0 to V_{CC}	±50	mA
I_{CC} or I_{GND}	DC V_{CC} current		±250	mA
	DC ground current		±250	
T_{STG}	Storage temperature		-65 to 150	°C
P_{TOT}	Power dissipation per package Plastic DIP	Above 70°C:derate linearly by 8mW/K	500	mW
	Power dissipation per package Plastic surface mount (SO)	Above 70°C:derate linearly by 6mW/K	400	mW

NOTES:

1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		V_{CC}	74AC11827				74ACT11827				UNIT
					T_A = +25°C		T_A = -40°C to +85°C		T_A = +25°C		T_A = -40°C to +85°C		
				V	Min	Max	Min	Max	Min	Max	Min	Max	
V_{IH}	High-level input voltage			3.0	2.10		2.10						V
				4.5	3.15		3.15		2.0		2.0		
				5.5	3.85		3.85		2.0		2.0		
V_{IL}	Low-level input voltage			3.0		0.90		0.90					V
				4.5		1.35		1.35		0.8		0.8	
				5.5		1.65		1.65		0.8		0.8	
V_{OH}	High-level output voltage	V_I = V_{IL} or V_{IH}	I_{OH} = -50μA	3.0	2.9		2.9						V
				4.5	4.4		4.4		4.4		4.4		
				5.5	5.4		5.4		5.4		5.4		
			I_{OH} = -4mA	3.0	2.58		2.48						
			I_{OH} = -24mA	4.5	3.94		3.8		3.94		3.8		
				5.5	4.94		4.8		4.94		4.8		
			I_{OH} = -75mA[1]	5.5			3.85				3.85		
V_{OL}	Low-level output voltage	V_I = V_{IL} or V_{IH}	I_{OL} = 50μA	3.0		0.1		0.1					V
				4.5		0.1		0.1		0.1		0.1	
				5.5		0.1		0.1		0.1		0.1	
			I_{OL} = 12mA	3.0		0.36		0.44					
			I_{OL} = 24mA	4.5		0.36		0.44		0.36		0.44	
				5.5		0.36		0.44		0.36		0.44	
			I_{OL} = 75mA[1]	5.5				1.65				1.65	
I_I	Input leakage current	V_I = V_{CC} or GND		5.5		±0.1		±1.0		±0.1		±1.0	μA
I_{OZ}	3-State output off-state current	V_I = V_{IL} or V_{IH}; V_O = V_{CC} or GND		5.5		±0.5		±5.0		±0.5		±5.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC} or GND, I_O = 0		5.5		8.0		80		8.0		80	μA
ΔI_{CC}	Supply current, TTL inputs High[2]	One input at 3.4V, other inputs at V_{CC} or GND		5.5						0.9		1.0	mA

NOTES:
1. Not more than one output should be tested at a time, and the duration of the test should not exceed 10ms.
2. This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0V or V_{CC}.

74AC/ACT11828

10-Wide Buffer/Line Driver; 3-State; INV

Objective Specification

FEATURES

- **3-State buffers**
- **Output capability: ±24 mA**
- **CMOS (AC) and TTL (ACT) voltage level inputs**
- **50Ω incident wave switching**
- **Center-pin V_{CC} and ground configuration to minimize high-speed switching noise**
- **I_{CC} category: MSI**

DESCRIPTION

The 74AC/ACT11828 high-performance CMOS devices combine very high speed and high output drive comparable to the most advanced TTL families.

The 74AC/ACT11828 device is a 10-wide buffer/line driver and provides high performance bus interface buffering for wide data/address paths or busses carrying parity. It has NOR Output Enables ($\overline{OE}_0$, $\overline{OE}_1$) for maximum control flexibility.

GENERAL INFORMATION

SYMBOL	PARAMETER	CONDITIONS T_A = 25°C; GND = 0V; V_{CC} = 5.0V		TYPICAL AC	TYPICAL ACT	UNIT
t_{PLH}/t_{PHL}	Propagation delay A_n to $\overline{Y}_n$	C_L = 50pF		5.5	6.7	ns
C_{PD}	Power dissipation capacitance per buffer[1]	f = 1MHz; C_L = 50pF	Enabled	40	40	pF
			Disabled	14	13	
C_{IN}	Input capacitance	V_I = 0V or V_{CC}		4.5	4.5	pF
C_{OUT}	Output capacitance	V_O = 0V or V_{CC}; Disabled		10	10	pF
I_{LATCH}	Latch-up current	Per Jedec JC40.2 Standard 17		500	500	mA

Note:

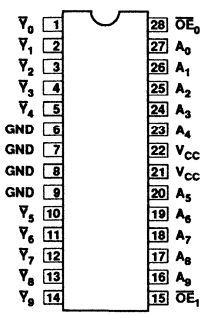
1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_I + \Sigma (C_L \times V_{CC}^2 \times f_O)$ where:
   f_I = input frequency in MHz, C_L = output load capacitance in pF,
   f_O = output frequency in MHz, V_{CC} = supply voltage in V,
   $\Sigma (C_L \times V_{CC}^2 \times f_O)$ = sum of outputs

ORDERING INFORMATION

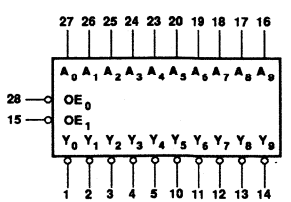
PACKAGES	TEMPERATURE RANGE	ORDER CODE
28-pin plastic DIP (300mil-wide)	-40°C to +85°C	74AC11828N 74ACT11828N
28-pin plastic SO (300mil-wide)	-40°C to +85°C	74AC11828D 74ACT11828D

PIN CONFIGURATION

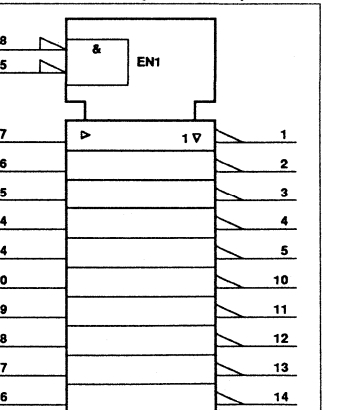
N and D Packages



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



PIN DESCRIPTION

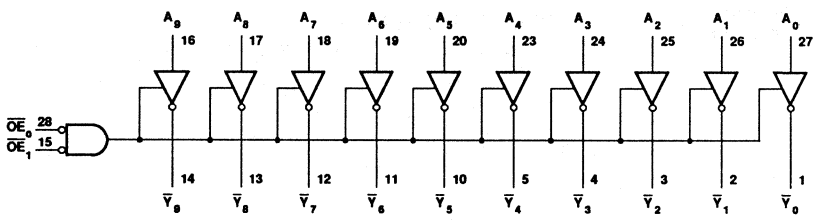
PIN NUMBER	SYMBOL	NAME AND FUNCTION
28, 15	$\overline{OE}_0$, $\overline{OE}_1$	Output enable input (active Low)
27, 26, 25, 24, 23, 20, 19, 18, 17, 16	A_0 - A_9	Data inputs
1, 2, 3, 4, 5, 10, 11, 12, 13, 14	$\overline{Y}_0$ - $\overline{Y}_9$	Data inputs
6, 7, 8, 9	GND	Ground (0V)
21, 22	V_{CC}	Positive supply voltage

FUNCTION TABLE

INPUTS		OUTPUTS
$\overline{OE}_n$	A_n	$\overline{Y}_n$
L	L	H
L	H	L
H	X	Z

H = Highvoltage level
L = Low voltage level
X = Don't care
Z = High-impedance

LOGIC DIAGRAM



RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	74AC11828			74ACT11828			UNIT
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	DC supply voltage	3.0[1]	5.0	5.5	4.5	5.0	5.5	V
V_I	Input voltage	0		V_{CC}	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	0		V_{CC}	V
$\Delta t/\Delta v$	Input transition rise or fall rate	0		10	0		10	ns/V
T_A	Operating free-air temperature	-40		+85	-40		+85	°C

NOTE:

1. No electrical or switching characteristics are specified at V_{CC} < 3V. Operation between 2V and 3V is not recommended, but within that range, a device output will maintain a previously established logic state.

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	TEST CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 to+7.0	V
I_{IK} or V_I	DC input diode current[2]	$V_I < 0$	-20	mA
		$V_I > V_{CC}$	20	
	DC input voltage		-0.5 to V_{CC} +0.5	V
I_{OK} or V_O	DC output diode current[2]	$V_O < 0$	-50	mA
		$V_O > V_{CC}$	50	
	DC output voltage		-0.5 to V_{CC} +0.5	V
I_O	DC output source or sink current per output pin	V_O = 0 to V_{CC}	±50	mA
I_{CC} or I_{GND}	DC V_{CC} current		±250	mA
	DC ground current		±250	
T_{STG}	Storage temperature		-65 to 150	°C
P_{TOT}	Power dissipation per package Plastic DIP	Above 70°C:derate linearly by 8mW/K	500	mW
	Power dissipation per package Plastic surface mount (SO)	Above 70°C:derate linearly by 6mW/K	400	mW

NOTES:

1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		V_{CC}	74AC11828				74ACT11828				UNIT
					T_A = +25°C		T_A = -40°C to +85°C		T_A = +25°C		T_A = -40°C to +85°C		
				V	Min	Max	Min	Max	Min	Max	Min	Max	
V_{IH}	High-level input voltage			3.0	2.10		2.10						V
				4.5	3.15		3.15		2.0		2.0		
				5.5	3.85		3.85		2.0		2.0		
V_{IL}	Low-level input voltage			3.0		0.90		0.90					V
				4.5		1.35		1.35		0.8		0.8	
				5.5		1.65		1.65		0.8		0.8	
V_{OH}	High-level output voltage	V_I = V_{IL} or V_{IH}	I_{OH} = -50μA	3.0	2.9		2.9						V
				4.5	4.4		4.4		4.4		4.4		
				5.5	5.4		5.4		5.4		5.4		
			I_{OH} = -4mA	3.0	2.58		2.48						
			I_{OH} = -24mA	4.5	3.94		3.8		3.94		3.8		
				5.5	4.94		4.8		4.94		4.8		
			I_{OH} = -75mA[1]	5.5			3.85				3.85		
V_{OL}	Low-level output voltage	V_I = V_{IL} or V_{IH}	I_{OL} = 50μA	3.0		0.1		0.1					V
				4.5		0.1		0.1		0.1		0.1	
				5.5		0.1		0.1		0.1		0.1	
			I_{OL} = 12mA	3.0		0.36		0.44					
			I_{OL} = 24mA	4.5		0.36		0.44		0.36		0.44	
				5.5		0.36		0.44		0.36		0.44	
			I_{OL} = 75mA[1]	5.5				1.65				1.65	
I_I	Input leakage current	V_I = V_{CC} or GND		5.5		±0.1		±1.0		±0.1		±1.0	μA
I_{OZ}	3-State output off-state current	V_I = V_{IL} or V_{IH}, V_O = V_{CC} or GND		5.5		±0.5		±5.0		±0.5		±5.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC} or GND, I_O = 0		5.5		8.0		80		8.0		80	μA
ΔI_{CC}	Supply current, TTL inputs High[2]	One input at 3.4V, other inputs at V_{CC} or GND		5.5						0.9		1.0	mA

NOTES:
1. Not more than one output should be tested at a time, and the duration of the test should not exceed 10ms.
2. This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0V or V_{CC}.

74AC/ACT11841

10-Wide D-Type Transparent Latch; 3-State

Objective Specification

FEATURES

- **High-speed parallel latches**
- **Extra data width for wide address/ data paths or buses with parity**
- **Output capability: ±24mA**
- **CMOS (AC) and TTL (ACT) voltage level inputs**
- **50Ω incident wave switching**
- **Center-pin V_{CC} and ground configuration to minimize high-speed switching noise**
- **I_{CC} category: MSI**

DESCRIPTION

The 74AC/ACT11841 high-performance CMOS devices combine very high speed and high output drive comparable to the most advanced TTL families.

The AC/ACT11841 consists of ten D-type latches with 3-State outputs. The flip-flops appear transparent to the data when Latch Enable (LE) is High. This allows asynchronous operation, as the output transition follows the data in transition. On the LE High-to-Low transition, the data that meets the setup and hold time is latched.

Data appears on the bus when the Output Enable ($\overline{OE}$) is Low. When $\overline{OE}$ is High the output is in the high-impedance state.

GENERAL INFORMATION

SYMBOL	PARAMETER	CONDITIONS T_A = 25°C; GND = 0V; V_{CC} = 5.0V		TYPICAL AC	TYPICAL ACT	UNIT
t_{PLH}/t_{PHL}	Propagation delay LE to Q_n	C_L = 50pF		8.5	10.4	ns
C_{PD}	Power dissipation capacitance per latch[1]	f = 1MHz; C_L = 50pF	Enabled	54	53	pF
			Disabled	32	30	
C_{IN}	Input capacitance	V_I = 0V or V_{CC}		4.5	4.5	pF
C_{OUT}	Output capacitance	V_O = 0V or V_{CC}; Disabled		10	10	pF
I_{LATCH}	Latch-up current	Per Jedec JC40.2 Standard 17		500	500	mA

Note:

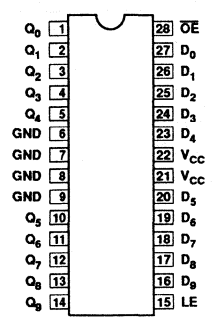
1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_I + \Sigma (C_L \times V_{CC}^2 \times f_O)$ where:
   f_I = input frequency in MHz, C_L = output load capacitance in pF,
   f_O = output frequency in MHz, V_{CC} = supply voltage in V,
   $\Sigma (C_L \times V_{CC}^2 \times f_O)$ = sum of outputs

ORDERING INFORMATION

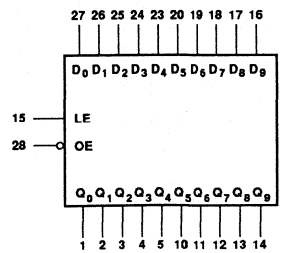
PACKAGES	TEMPERATURE RANGE	ORDER CODE
28-pin plastic DIP (300mil-wide)	-40°C to +85°C	74AC11841N 74ACT11841N
28-pin plastic SO (300mil-wide)	-40°C to +85°C	74AC11841D 74ACT11841D

PIN CONFIGURATION

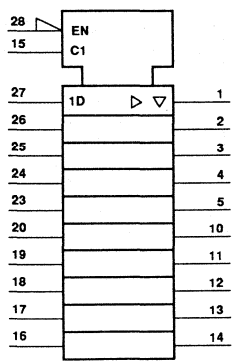
N and D Packages



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



PIN DESCRIPTION

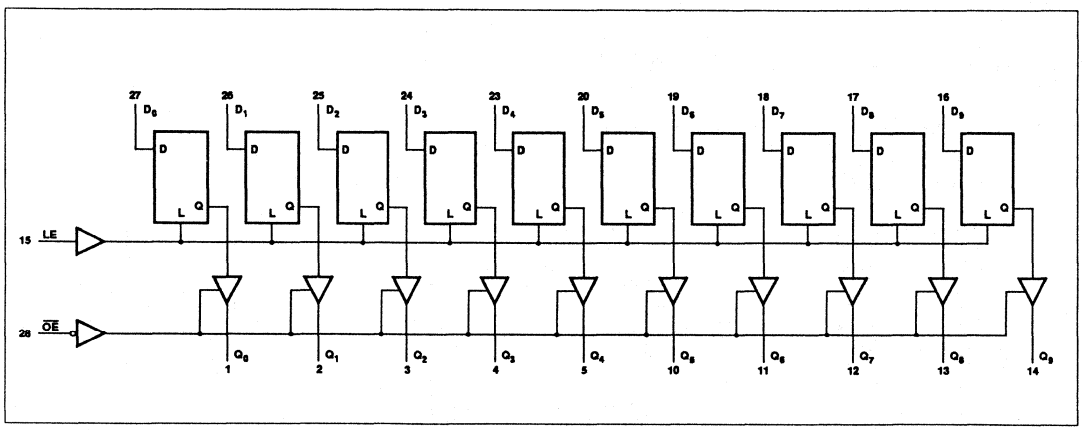
PIN NUMBER	SYMBOL	NAME AND FUNCTION
28	$\overline{OE}$	Output enable input (active-Low)
15	LE	Latch enable input
1, 2, 3, 4, 5, 10, 11, 12, 13, 14	D_0 - D_9	Data inputs
27, 26, 25, 24, 23, 20, 19, 18, 17, 16	Q_0 - Q_9	Data outputs
6, 7, 8, 9	GND	Ground (0V)
21, 22	V_{CC}	Positive supply voltage

FUNCTION TABLE

INPUTS			OUTPUTS	OPERATING MODE
$\overline{OE}$	LE	D_n	Q_n	
L L	H H	L H	L H	Transparent
L L	↓ ↓	l h	L H	Latched
H	X	X	Z	High-Z
L	L	X	NC	Hold

H = High voltage level
h = High voltage level one setup time prior to the High-to-Low transition of LE
L = Low voltage level
l = Low voltage level one setup time prior to the High-to-Low transition of LE
X = Don't Care
Z = High-impedance
↓ = High-to-Low transition
NC = No change

LOGIC DIAGRAM



RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	74AC11841			74ACT11841			UNIT
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	DC supply voltage	3.0[1]	5.0	5.5	4.5	5.0	5.5	V
V_I	Input voltage	0		V_{CC}	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	0		V_{CC}	V
$\Delta t/\Delta v$	Input transition rise or fall rate	0		10	0		10	ns/V
T_A	Operating free-air temperature	-40		+85	-40		+85	°C

NOTE:
1. No electrical or switching characteristics are specified at V_{CC} < 3V. Operation between 2V and 3V is not recommended, but within that range, a device output will maintain a previously established logic state.

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	TEST CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 to+7.0	V
I_{IK} or V_I	DC input diode current[2]	$V_I < 0$	-20	mA
		$V_I > V_{CC}$	20	
	DC input voltage		-0.5 to V_{CC} +0.5	V
I_{OK} or V_O	DC output diode current[2]	$V_O < 0$	-50	mA
		$V_O > V_{CC}$	50	
	DC output voltage		-0.5 to V_{CC} +0.5	V
I_O	DC output source or sink current per output pin	V_O = 0 to V_{CC}	±50	mA
I_{CC} or I_{GND}	DC V_{CC} current		±250	mA
	DC ground current		±250	
T_{STG}	Storage temperature		-65 to 150	°C
P_{TOT}	Power dissipation per package Plastic DIP	Above 70°C:derate linearly by 8mW/K	500	mW
	Power dissipation per package Plastic surface mount (SO)	Above 70°C:derate linearly by 6mW/K	400	mW

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		V_{CC}	74AC11841				74ACT11841				UNIT
					T_A = +25°C		T_A = -40°C to +85°C		T_A = +25°C		T_A = -40°C to +85°C		
				V	Min	Max	Min	Max	Min	Max	Min	Max	
V_{IH}	High-level input voltage			3.0	2.10		2.10						V
				4.5	3.15		3.15		2.0		2.0		
				5.5	3.85		3.85		2.0		2.0		
V_{IL}	Low-level input voltage			3.0		0.90		0.90					V
				4.5		1.35		1.35		0.8		0.8	
				5.5		1.65		1.65		0.8		0.8	
V_{OH}	High-level output voltage	V_I = V_{IL} or V_{IH}	I_{OH} = -50μA	3.0	2.9		2.9						V
				4.5	4.4		4.4		4.4		4.4		
				5.5	5.4		5.4		5.4		5.4		
			I_{OH} = -4mA	3.0	2.58		2.48						
			I_{OH} = -24mA	4.5	3.94		3.8		3.94		3.8		
				5.5	4.94		4.8		4.94		4.8		
			I_{OH} = -75mA[1]	5.5			3.85				3.85		
V_{OL}	Low-level output voltage	V_I = V_{IL} or V_{IH}	I_{OL} = 50μA	3.0		0.1		0.1					V
				4.5		0.1		0.1		0.1		0.1	
				5.5		0.1		0.1		0.1		0.1	
			I_{OL} = 12mA	3.0		0.36		0.44					
			I_{OL} = 24mA	4.5		0.36		0.44		0.36		0.44	
				5.5		0.36		0.44		0.36		0.44	
			I_{OL} = 75mA[1]	5.5				1.65				1.65	
I_I	Input leakage current	V_I = V_{CC} or GND		5.5		±0.1		±1.0		±0.1		±1.0	μA
I_{OZ}	3-State output off-state current	V_I = V_{IL} or V_{IH}, V_O = V_{CC} or GND		5.5		±0.5		±5.0		±0.5		±5.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC} or GND, I_O = 0		5.5		8.0		80		8.0		80	μA
ΔI_{CC}	Supply current, TTL inputs High[2]	One input at 3.4V, other inputs at V_{CC} or GND		5.5						0.9		1.0	mA

NOTES:
1. Not more than one output should be tested at a time, and the duration of the test should not exceed 10ms.
2. This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0V or V_{CC}.

74AC/ACT11842

10-Wide D-Type Transparent Latch; 3-State; INV

Objective Specification

FEATURES

- **High-speed parallel latches**
- **Extra data width for wide address/ data paths or buses with parity**
- **Output capability: ±24mA**
- **CMOS (AC) and TTL (ACT) voltage level inputs**
- **50Ω incident wave switching**
- **Center-pin V_{CC} and ground configuration to minimize high-speed switching noise**
- **I_{CC} category: MSI**

DESCRIPTION

The 74AC/ACT11842 high-performance CMOS devices combine very high speed and high output drive comparable to the most advanced TTL families.

The AC/ACT11842 consists of ten D-type latches with 3-State inverting outputs. The flip-flops appear transparent to the data when Latch Enable (LE) is High. This allows asynchronous operation, as the output transition follows the data in transition. On the LE High-to-Low transition, the data that meets the setup and hold time is latched.

Data appears on the bus when the Output Enable ($\overline{OE}$) is Low. When $\overline{OE}$ is High the output is in the high-impedance state.

GENERAL INFORMATION

SYMBOL	PARAMETER	CONDITIONS T_A = 25°C; GND = 0V; V_{CC} = 5.0V		TYPICAL AC	TYPICAL ACT	UNIT
t_{PLH}/t_{PHL}	Propagation delay LE to $\overline{O}_n$	C_L = 50pF		8.5	10.4	ns
C_{PD}	Power dissipation capacitance per latch[1]	f = 1MHz; C_L = 50pF	Enabled	54	54	pF
			Disabled	32	32	
C_{IN}	Input capacitance	V_I = 0V or V_{CC}		4.5	4.5	pF
C_{OUT}	Output capacitance	V_O = 0V or V_{CC}; Disabled		10	10	pF
I_{LATCH}	Latch-up current	Per Jedec JC40.2 Standard 17		500	500	mA

Note:

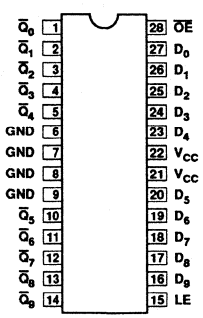
1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_I + \Sigma (C_L \times V_{CC}^2 \times f_O)$ where:
   f_I = input frequency in MHz, C_L = output load capacitance in pF,
   f_O = output frequency in MHz, V_{CC} = supply voltage in V,
   $\Sigma (C_L \times V_{CC}^2 \times f_O)$ = sum of outputs

ORDERING INFORMATION

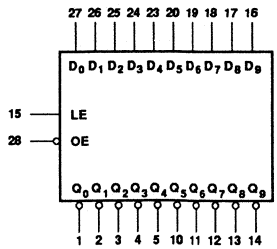
PACKAGES	TEMPERATURE RANGE	ORDER CODE
28-pin plastic DIP (300mil-wide)	-40°C to +85°C	74AC11842N 74ACT11842N
28-pin plastic SO (300mil-wide)	-40°C to +85°C	74AC11842D 74ACT11842D

PIN CONFIGURATION

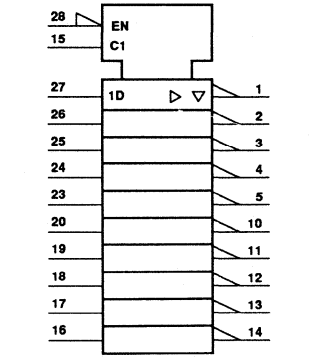
N and D Packages



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



PIN DESCRIPTION

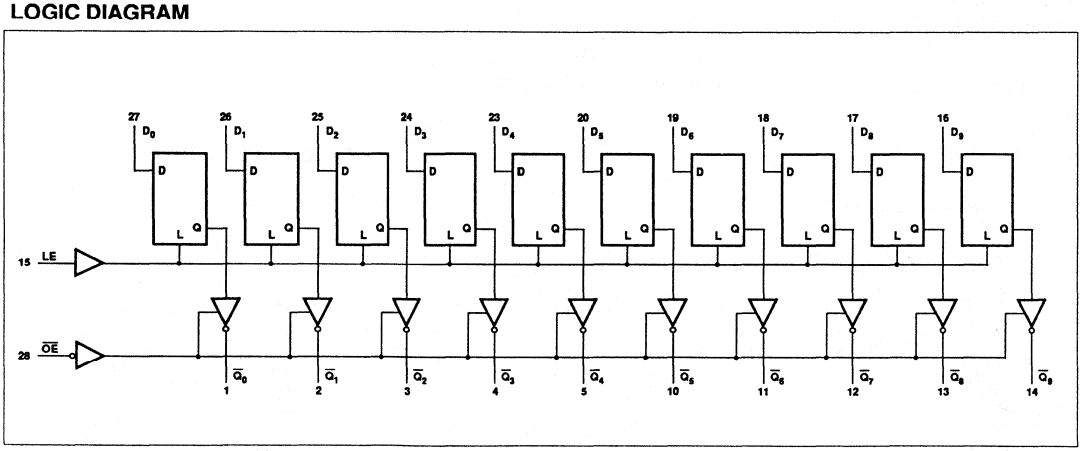
PIN NUMBER	SYMBOL	NAME AND FUNCTION
28	$\overline{OE}$	Output enable input (active-Low)
15	LE	Latch enable input
1, 2, 3, 4, 5, 10, 11, 12, 13, 14	D_0 - D_9	Data inputs
27, 26, 25, 24, 23, 20, 19, 18, 17, 16	$\overline{Q}_0$ - $\overline{Q}_9$	Data outputs
6, 7, 8, 9	GND	Ground (0V)
21, 22	V_{CC}	Positive supply voltage

FUNCTION TABLE

INPUTS			OUTPUTS	OPERATING MODE
$\overline{OE}$	LE	D_n	$\overline{Q}_n$	
L	H	L	H	Transparent
L	H	H	L	
L	↓	l	H	Latched
L	↓	h	L	
H	X	X	Z	High-Z
L	L	X	NC	Hold

H = High voltage level
h = High voltage level one setup time prior to the High-to-Low transition of LE
L = Low voltage level
l = Low voltage level one setup time prior to the High-to-Low transition of LE
X = Don't Care
Z = High-impedance
↓ = High-to-Low transition
NC = No change

LOGIC DIAGRAM



RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	74AC11842			74ACT11842			UNIT
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	DC supply voltage	3.0[1]	5.0	5.5	4.5	5.0	5.5	V
V_I	Input voltage	0		V_{CC}	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	0		V_{CC}	V
$\Delta t/\Delta v$	Input transition rise or fall rate	0		10	0		10	ns/V
T_A	Operating free-air temperature	-40		+85	-40		+85	°C

NOTE:
1. No electrical or switching characteristics are specified at V_{CC} < 3V. Operation between 2V and 3V is not recommended, but within that range, a device output will maintain a previously established logic state.

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	TEST CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 to+7.0	V
I_{IK} or V_I	DC input diode current[2]	$V_I < 0$	-20	mA
		$V_I > V_{CC}$	20	
	DC input voltage		-0.5 to V_{CC} +0.5	V
I_{OK} or V_O	DC output diode current[2]	$V_O < 0$	-50	mA
		$V_O > V_{CC}$	50	
	DC output voltage		-0.5 to V_{CC} +0.5	V
I_O	DC output source or sink current per output pin	V_O = 0 to V_{CC}	±50	mA
I_{CC} or I_{GND}	DC V_{CC} current		±250	mA
	DC ground current		±250	
T_{STG}	Storage temperature		-65 to 150	°C
P_{TOT}	Power dissipation per package Plastic DIP	Above 70°C:derate linearly by 8mW/K	500	mW
	Power dissipation per package Plastic surface mount (SO)	Above 70°C:derate linearly by 6mW/K	400	mW

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		V_{CC}	74AC11842				74ACT11842				UNIT
					T_A = +25°C		T_A = -40°C to +85°C		T_A = +25°C		T_A = -40°C to +85°C		
				V	Min	Max	Min	Max	Min	Max	Min	Max	
V_{IH}	High-level input voltage			3.0	2.10		2.10						V
				4.5	3.15		3.15		2.0		2.0		
				5.5	3.85		3.85		2.0		2.0		
V_{IL}	Low-level input voltage			3.0		0.90		0.90					V
				4.5		1.35		1.35		0.8		0.8	
				5.5		1.65		1.65		0.8		0.8	
V_{OH}	High-level output voltage	V_I = V_{IL} or V_{IH}	I_{OH} = -50μA	3.0	2.9		2.9						V
				4.5	4.4		4.4		4.4		4.4		
				5.5	5.4		5.4		5.4		5.4		
			I_{OH} = -4mA	3.0	2.58		2.48						
			I_{OH} = -24mA	4.5	3.94		3.8		3.94		3.8		
				5.5	4.94		4.8		4.94		4.8		
			I_{OH} = -75mA[1]	5.5			3.85				3.85		
V_{OL}	Low-level output voltage	V_I = V_{IL} or V_{IH}	I_{OL} = 50μA	3.0		0.1		0.1					V
				4.5		0.1		0.1		0.1		0.1	
				5.5		0.1		0.1		0.1		0.1	
			I_{OL} = 12mA	3.0		0.36		0.44					
			I_{OL} = 24mA	4.5		0.36		0.44		0.36		0.44	
				5.5		0.36		0.44		0.36		0.44	
			I_{OL} = 75mA[1]	5.5				1.65				1.65	
I_I	Input leakage current	V_I = V_{CC} or GND		5.5		±0.1		±1.0		±0.1		±1.0	μA
I_{OZ}	3-State output off-state current	V_I = V_{IL} or V_{IH}, V_O = V_{CC} or GND		5.5		±0.5		±5.0		±0.5		±5.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC} or GND, I_O = 0		5.5		8.0		80		8.0		80	μA
ΔI_{CC}	Supply current, TTL inputs High[2]	One input at 3.4V, other inputs at V_{CC} or GND		5.5						0.9		1.0	mA

NOTES:
1. Not more than one output should be tested at a time, and the duration of the test should not exceed 10ms.
2. This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0V or V_{CC}.

74AC/ACT11843

9-Wide D-Type Transparent Latch with Set and Reset; 3-State

Objective Specification

FEATURES

- **High-speed parallel latches**
- **Extra data width for wide address/ data paths or buses with parity**
- **Output capability: ±24mA**
- **CMOS (AC) and TTL (ACT) voltage level inputs**
- **50Ω incident wave switching**
- **Center-pin V_{CC} and ground configuration to minimize high-speed switching noise**
- **I_{CC} category: MSI**

DESCRIPTION

The 74AC/ACT11843 high-performance CMOS devices combine very high speed and high output drive comparable to the most advanced TTL families.

The AC/ACT11843 consists of nine D-type latches with 3-State outputs. The flip-flops appear transparent to the data when Latch Enable (LE) is High. This aliows asynchronous operation, as the output transition follows the data in transition. On the LE High-to-Low transition, the data that meets the setup and hold time is latched.

Data appears on the bus when the Output

GENERAL INFORMATION

SYMBOL	PARAMETER	CONDITIONS T_A = 25°C; GND = 0V; V_{CC} = 5.0V		TYPICAL AC	TYPICAL ACT	UNIT
t_{PLH}/ t_{PHL}	Propagation delay LE to Q_n	C_L = 50pF		8.7	10.5	ns
C_{PD}	Power dissipation capacitance per latch[1]	f = 1MHz;	Enabled	55	55	pF
		C_L = 50pF	Disabled	33	32	pF
C_{IN}	Input capacitance	V_I = 0V or V_{CC}		4.5	4.5	pF
C_{OUT}	Output capacitance	V_O = 0V or V_{CC}; Disabled		10	10	pF
I_{LATCH}	Latch-up current	Per Jedec JC40.2 Standard 17		500	500	mA

Note:

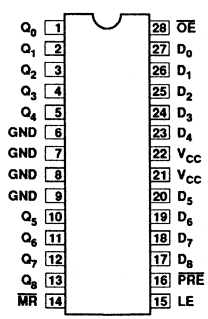
1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_I + \Sigma (C_L \times V_{CC}^2 \times f_O)$ where:
   f_I = input frequency in MHz, C_L = output load capacitance in pF,
   f_O = output frequency in MHz, V_{CC} = supply voltage in V,
   $\Sigma (C_L \times V_{CC}^2 \times f_O)$ = sum of outputs

ORDERING INFORMATION

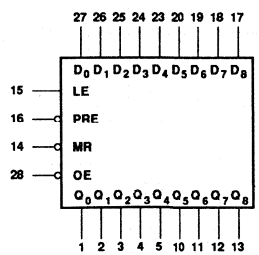
PACKAGES	TEMPERATURE RANGE	ORDER CODE
28-pin plastic DIP (300mil-wide)	-40°C to +85°C	74AC11843N 74ACT11843N
28-pin plastic SO (300mil-wide)	-40°C to +85°C	74AC11843D 74ACT11843D

PIN CONFIGURATION

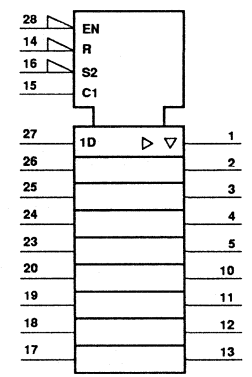
N and D Packages



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



9-Wide D-Type Transparent Latch with Set and Reset; 3-State

74AC/ACT11843

PIN DESCRIPTION

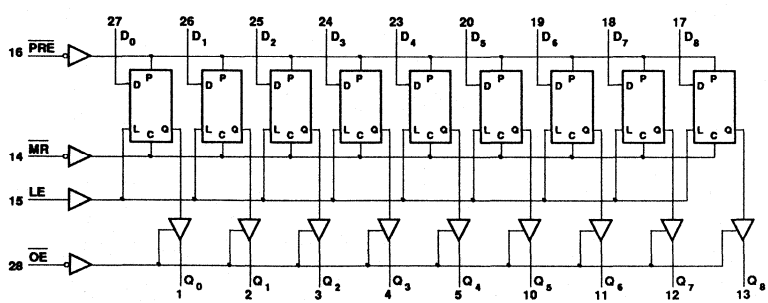
PIN NUMBER	SYMBOL	NAME AND FUNCTION
28	$\overline{OE}$	Output enable input (active-Low)
15	LE	Latch enable input
16	$\overline{PRE}$	Preset input (active-Low)
14	$\overline{MR}$	Master reset input (active-Low)
1, 2, 3, 4, 5, 10, 11, 12, 13	D_0 - D_8	Data inputs
27, 26, 25, 24, 23, 20, 19, 18, 17	Q_0 - Q_8	Data outputs
6, 7, 8, 9	GND	Ground (0V)
21, 22	V_{CC}	Positive supply voltage

FUNCTION TABLE

INPUTS					OUTPUTS	OPERATING MODE
$\overline{OE}$	$\overline{PRE}$	$\overline{MR}$	LE	D_n	Q_n	
H	X	X	X	X	Z	High-Z
L	L	X	X	X	H	Preset
L	H	L	X	X	L	Clear
L L	H H	H H	H H	L H	L H	Transparent
L L	H H	H H	↓ ↓	l h	L H	Latched
L	H	H	L	X	NC	Hold

H = High voltage level
h = High voltage level one setup time prior to the High-to-Low transition of LE
L = Low voltage level
l = Low voltage level one setup time prior to the High-to-Low transition of LE
X = Don't Care
Z = High-impedance
↓ = High-to-Low transition
NC = No change

LOGIC DIAGRAM



Enable ($\overline{OE}$) is Low. When $\overline{OE}$ is High the output is in the high-impedance state.

The AC/ACT11843 also features a Master Rest ($\overline{MR}$) pin and a Preset ($\overline{PRE}$) pin. These pins are ideal for parity bus interfacing in high perfance systems. When $\overline{MR}$ is Low, the outputs are Low if $\overline{OE}$ is Low. When $\overline{MR}$ is High, data can be entered into the latch. When $\overline{PRE}$ is Low, the outputs are High if $\overline{OE}$ is Low. $\overline{PRE}$ overrides $\overline{MR}$.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	74AC11843			74ACT11843			UNIT
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	DC supply voltage	3.0[1]	5.0	5.5	4.5	5.0	5.5	V
V_I	Input voltage	0		V_{CC}	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	0		V_{CC}	V
$\Delta t/\Delta v$	Input transition rise or fall rate	0		10	0		10	ns/V
T_A	Operating free-air temperature	-40		+85	-40		+85	°C

NOTE:

1. No electrical or switching characteristics are specified at $V_{CC} < 3V$. Operation between 2V and 3V is not recommended, but within that range, a device output will maintain a previously established logic state.

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	TEST CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 to+7.0	V
I_{IK} or V_I	DC input diode current[2]	$V_I < 0$	-20	mA
		$V_I > V_{CC}$	20	
	DC input voltage		-0.5 to V_{CC} +0.5	V
I_{OK} or V_O	DC output diode current[2]	$V_O < 0$	-50	mA
		$V_O > V_{CC}$	50	
	DC output voltage		-0.5 to V_{CC} +0.5	V
I_O	DC output source or sink current per output pin	V_O = 0 to V_{CC}	±50	mA
I_{CC} or I_{GND}	DC V_{CC} current		±225	mA
	DC ground current		±225	
T_{STG}	Storage temperature		-65 to 150	°C
P_{TOT}	Power dissipation per package Plastic DIP	Above 70°C:derate linearly by 8mW/K	500	mW
	Power dissipation per package Plastic surface mount (SO)	Above 70°C:derate linearly by 6mW/K	400	mW

NOTES:

1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		V_{CC}	74AC11843				74ACT11843				UNIT
					T_A = +25°C		T_A = -40°C to +85°C		T_A = +25°C		T_A = -40°C to +85°C		
				V	Min	Max	Min	Max	Min	Max	Min	Max	
V_{IH}	High-level input voltage			3.0	2.10		2.10						V
				4.5	3.15		3.15		2.0		2.0		
				5.5	3.85		3.85		2.0		2.0		
V_{IL}	Low-level input voltage			3.0		0.90		0.90					V
				4.5		1.35		1.35		0.8		0.8	
				5.5		1.65		1.65		0.8		0.8	
V_{OH}	High-level output voltage	V_I = V_{IL} or V_{IH}	I_{OH} = -50μA	3.0	2.9		2.9						V
				4.5	4.4		4.4		4.4		4.4		
				5.5	5.4		5.4		5.4		5.4		
			I_{OH} = -4mA	3.0	2.58		2.48						
			I_{OH} = -24mA	4.5	3.94		3.8		3.94		3.8		
				5.5	4.94		4.8		4.94		4.8		
			I_{OH} = -75mA[1]	5.5			3.85				3.85		
V_{OL}	Low-level output voltage	V_I = V_{IL} or V_{IH}	I_{OL} = 50μA	3.0		0.1		0.1					V
				4.5		0.1		0.1		0.1		0.1	
				5.5		0.1		0.1		0.1		0.1	
			I_{OL} = 12mA	3.0		0.36		0.44					
			I_{OL} = 24mA	4.5		0.36		0.44		0.36		0.44	
				5.5		0.36		0.44		0.36		0.44	
			I_{OL} = 75mA[1]	5.5				1.65				1.65	
I_I	Input leakage current	V_I = V_{CC} or GND		5.5		±0.1		±1.0		±0.1		±1.0	μA
I_{OZ}	3-State output off-state current	V_I = V_{IL} or V_{IH}, V_O = V_{CC} or GND		5.5		±0.5		±5.0		±0.5		±5.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC} or GND, I_O = 0		5.5		8.0		80		8.0		80	μA
ΔI_{CC}	Supply current, TTL inputs High[2]	One input at 3.4V, other inputs at V_{CC} or GND		5.5						0.9		1.0	mA

NOTES:
1. Not more than one output should be tested at a time, and the duration of the test should not exceed 10ms.
2. This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0V or V_{CC}.

74AC/ACT11844

9-Wide D-Type Transparent Latch with Set and Reset; 3-State; INV

Objective Specification

FEATURES

- **High-speed parallel latches**
- **Extra data width for wide address/ data paths or buses with parity**
- **Output capability: ±24mA**
- **CMOS (AC) and TTL (ACT) voltage level inputs**
- **50Ω incident wave switching**
- **Center-pin V_{CC} and ground configuration to minimize high-speed switching noise**
- **I_{CC} category: MSI**

DESCRIPTION

The 74AC/ACT11844 high-performance CMOS devices combine very high speed and high output drive comparable to the most advanced TTL families.

The AC/ACT11844 consists of nine D-type latches with inverting 3-State outputs. The flip-flops appear transparent to the data when Latch Enable (LE) is High. This allows asynchronous operation, as the output transition follows the data in transition. On the LE High-to-Low transition, the data that meets the setup and hold time is latched.

Data appears on the bus when the Output

GENERAL INFORMATION

SYMBOL	PARAMETER	CONDITIONS T_A = 25°C; GND = 0V; V_{CC} = 5.0V		TYPICAL AC	TYPICAL ACT	UNIT
t_{PLH}/t_{PHL}	Propagation delay LE to $\overline{Q}_n$	C_L = 50pF		8.7	10.5	ns
C_{PD}	Power dissipation capacitance per latch[1]	f = 1MHz; C_L = 50pF	Enabled	55	55	pF
			Disabled	33	32	
C_{IN}	Input capacitance	V_I = 0V or V_{CC}		4.5	4.5	pF
C_{OUT}	Output capacitance	V_O = 0V or V_{CC}; Disabled		10	10	pF
I_{LATCH}	Latch-up current	Per Jedec JC40.2 Standard 17		500	500	mA

Note:

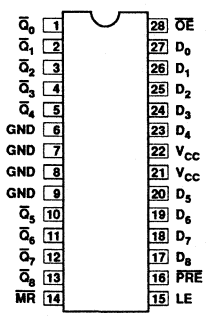
1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_I + \Sigma (C_L \times V_{CC}^2 \times f_O)$ where:
   f_I = input frequency in MHz, C_L = output load capacitance in pF,
   f_O = output frequency in MHz, V_{CC} = supply voltage in V,
   $\Sigma (C_L \times V_{CC}^2 \times f_O)$ = sum of outputs

ORDERING INFORMATION

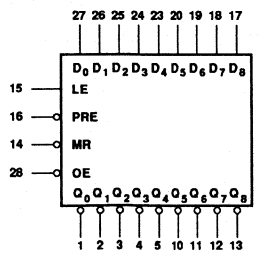
PACKAGES	TEMPERATURE RANGE	ORDER CODE
28-pin plastic DIP (300mil-wide)	-40°C to +85°C	74AC11844N 74ACT11844N
28-pin plastic SO (300mil-wide)	-40°C to +85°C	74AC11844D 74ACT11844D

PIN CONFIGURATION

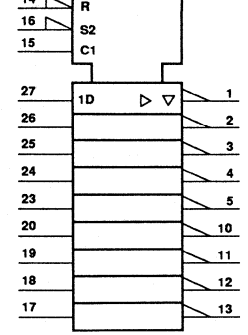
N and D Packages



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



9-Wide D-Type Transparent Latch with Set and Reset; 3-State; INV

74AC/ACT11844

PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
28	$\overline{OE}$	Output enable input (active-Low)
15	LE	Latch enable input
16	$\overline{PRE}$	Preset input (active-Low)
14	$\overline{MR}$	Master reset input (active-Low)
1, 2, 3, 4, 5, 10, 11, 12, 13	D_0 - D_8	Data inputs
27, 26, 25, 24, 23, 20, 19, 18, 17	$\overline{Q}_0$ - $\overline{Q}_8$	Data outputs
6, 7, 8, 9	GND	Ground (0V)
21, 22	V_{CC}	Positive supply voltage

FUNCTION TABLE

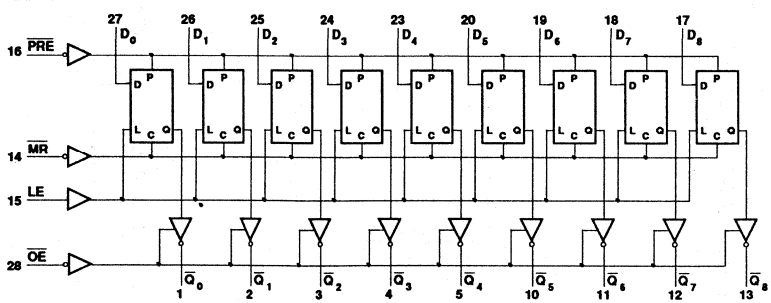
INPUTS					OUTPUTS	OPERATING MODE
$\overline{OE}$	$\overline{PRE}$	$\overline{MR}$	LE	D_n	$\overline{Q}_n$	
H	X	X	X	X	Z	High-Z
L	L	X	X	X	L	Preset
L	H	L	X	X	H	Clear
L L	H H	H H	H H	L H	H L	Transparent
L L	H H	H H	↓ ↓	l h	H L	Latched
L	H	H	L	X	NC	Hold

H = High voltage level
h = High voltage level one setup time prior to the High-to-Low transition of LE
L = Low voltage level
l = Low voltage level one setup time prior to the High-to-Low transition of LE
X = Don't Care
Z = High-impedance
↓ = High-to-Low transition
NC = No change

Enable ($\overline{OE}$) is Low. When $\overline{OE}$ is High the output is in the high-impedance state.

The AC/ACT11844 also features a Master Rest ($\overline{MR}$) pin and a Preset ($\overline{PRE}$) pin. These pins are ideal for parity bus interfacing in high perfance systems. When $\overline{MR}$ is Low, the outputs are High if $\overline{OE}$ is Low. When $\overline{MR}$ is High, data can be entered into the latch. When $\overline{PRE}$ is Low, the outputs are Low if $\overline{OE}$ is Low. $\overline{PRE}$ overrides $\overline{MR}$.

LOGIC DIAGRAM



RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	74AC11844			74ACT11844			UNIT
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	DC supply voltage	3.0[1]	5.0	5.5	4.5	5.0	5.5	V
V_I	Input voltage	0		V_{CC}	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	0		V_{CC}	V
$\Delta t/\Delta v$	Input transition rise or fall rate	0		10	0		10	ns/V
T_A	Operating free-air temperature	-40		+85	-40		+85	°C

NOTE:

1. No electrical or switching characteristics are specified at V_{CC} < 3V. Operation between 2V and 3V is not recommended, but within that range, a device output will maintain a previously established logic state.

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	TEST CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 to+7.0	V
I_{IK} or V_I	DC input diode current[2]	$V_I < 0$	-20	mA
		$V_I > V_{CC}$	20	
	DC input voltage		-0.5 to V_{CC} +0.5	V
I_{OK} or V_O	DC output diode current[2]	$V_O < 0$	-50	mA
		$V_O > V_{CC}$	50	
	DC output voltage		-0.5 to V_{CC} +0.5	V
I_O	DC output source or sink current per output pin	V_O = 0 to V_{CC}	±50	mA
I_{CC} or I_{GND}	DC V_{CC} current		±225	mA
	DC ground current		±225	
T_{STG}	Storage temperature		-65 to 150	°C
P_{TOT}	Power dissipation per package Plastic DIP	Above 70°C:derate linearly by 8mW/K	500	mW
	Power dissipation per package Plastic surface mount (SO)	Above 70°C:derate linearly by 6mW/K	400	mW

NOTES:

1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		V_{CC}	74AC11844				74ACT11844				UNIT
					T_A = +25°C		T_A = -40°C to +85°C		T_A = +25°C		T_A = -40°C to +85°C		
				V	Min	Max	Min	Max	Min	Max	Min	Max	
V_{IH}	High-level input voltage			3.0	2.10		2.10						V
				4.5	3.15		3.15		2.0		2.0		
				5.5	3.85		3.85		2.0		2.0		
V_{IL}	Low-level input voltage			3.0		0.90		0.90					V
				4.5		1.35		1.35		0.8		0.8	
				5.5		1.65		1.65		0.8		0.8	
V_{OH}	High-level output voltage	V_I = V_{IL} or V_{IH}	I_{OH} = -50μA	3.0	2.9		2.9						V
				4.5	4.4		4.4		4.4		4.4		
				5.5	5.4		5.4		5.4		5.4		
			I_{OH} = -4mA	3.0	2.58		2.48						
			I_{OH} = -24mA	4.5	3.94		3.8		3.94		3.8		
				5.5	4.94		4.8		4.94		4.8		
			I_{OH} = -75mA[1]	5.5			3.85				3.85		
V_{OL}	Low-level output voltage	V_I = V_{IL} or V_{IH}	I_{OL} = 50μA	3.0		0.1		0.1					V
				4.5		0.1		0.1		0.1		0.1	
				5.5		0.1		0.1		0.1		0.1	
			I_{OL} = 12mA	3.0		0.36		0.44					
			I_{OL} = 24mA	4.5		0.36		0.44		0.36		0.44	
				5.5		0.36		0.44		0.36		0.44	
			I_{OL} = 75mA[1]	5.5				1.65				1.65	
I_I	Input leakage current	V_I = V_{CC} or GND		5.5		±0.1		±1.0		±0.1		±1.0	μA
I_{OZ}	3-State output off-state current	V_I = V_{IL} or V_{IH}; V_O = V_{CC} or GND		5.5		±0.5		±5.0		±0.5		±5.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC} or GND, I_O = 0		5.5		8.0		80		8.0		80	μA
ΔI_{CC}	Supply current, TTL inputs High[2]	One input at 3.4V, other inputs at V_{CC} or GND		5.5						0.9		1.0	mA

NOTES:

1. Not more than one output should be tested at a time, and the duration of the test should not exceed 10ms.
2. This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0V or V_{CC}.

74AC/ACT11845

Octal D-Type Transparent Latch with Set and Reset; 3-State

Objective Specification

FEATURES

- **High-speed parallel registers with positive edge-triggered D-type flip-flops**
- **Output capability: ±24mA**
- **CMOS (AC) and TTL (ACT) voltage level inputs**
- **50Ω incident wave switching**
- **Center-pin V_{CC} and ground configuration to minimize high-speed switching noise**
- **I_{CC} category: MSI**

DESCRIPTION

The 74AC/ACT11845 high-performance CMOS devices combine very high speed and high output drive comparable to the most advanced TTL families.

The AC/ACT11845 consists of eight D-type latches with 3-State outputs. The flip-flops appear transparent to the data when Latch Enable (LE) is High. This allows asynchronous operation, as the output transition follows the data in transition. On the LE High-to-Low transition, the data that meets the setup and hold time is latched.

Data appears on the bus when the three

GENERAL INFORMATION

SYMBOL	PARAMETER	CONDITIONS T_A = 25°C; GND = 0V; V_{CC} = 5.0V		TYPICAL AC	TYPICAL ACT	UNIT
t_{PLH}/t_{PHL}	Propagation delay LE to Q_n	C_L = 50pF		8.7	10.5	ns
C_{PD}	Power dissipation capacitance per latch[1]	f = 1MHz; C_L = 50pF	Enabled	54	54	pF
			Disabled	32	32	
C_{IN}	Input capacitance	V_I = 0V or V_{CC}		4.5	4.5	pF
C_{OUT}	Output capacitance	V_O = 0V or V_{CC}; Disabled		10	10	pF
I_{LATCH}	Latch-up current	Per Jedec JC40.2 Standard 17		500	500	mA

Note:

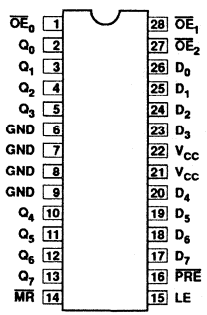
1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_I + \Sigma (C_L \times V_{CC}^2 \times f_O)$ where:
   f_I = input frequency in MHz, C_L = output load capacitance in pF,
   f_O = output frequency in MHz, V_{CC} = supply voltage in V,
   $\Sigma (C_L \times V_{CC}^2 \times f_O)$ = sum of outputs

ORDERING INFORMATION

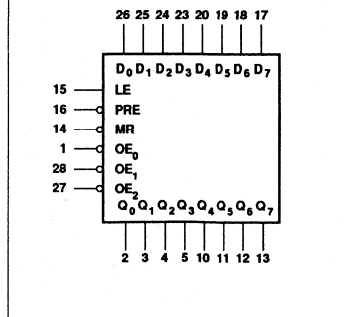
PACKAGES	TEMPERATURE RANGE	ORDER CODE
28-pin plastic DIP (300mil-wide)	-40°C to +85°C	74AC11845N 74ACT11845N
28-pin plastic SO (300mil-wide)	-40°C to +85°C	74AC11845D 74ACT11845D

PIN CONFIGURATION

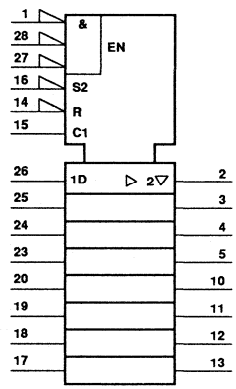
N and D Packages



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



Octal D-Type Transparent Latch with Set and Reset; 3-State

74AC/ACT11845

PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
1, 28, 27	$\overline{OE}_0$, $\overline{OE}_1$, $\overline{OE}_2$	Output enable inputs (active-Low)
15	LE	Latch enable input
16	$\overline{PRE}$	Preset input (active-Low)
14	$\overline{MR}$	Master reset input (active-Low)
2, 3, 4, 5, 10, 11, 12, 13	D_0 - D_7	Data inputs
26, 25, 24, 23, 20, 19, 18, 17	Q_0 - Q_7	Data outputs
6, 7, 8, 9	GND	Ground (0V)
21, 22	V_{CC}	Positive supply voltage

Output Enable pins ($\overline{OE}_0$, $\overline{OE}_1$, $\overline{OE}_2$) are Low. When any $\overline{OE}_n$ is High the output is in the high-impedance state.

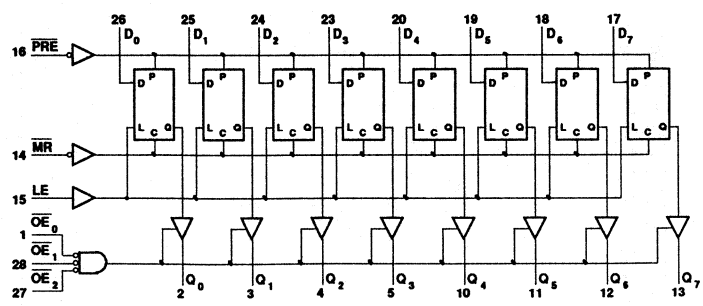
The AC/ACT11845 also features a Master Rest ($\overline{MR}$) pin and a Preset ($\overline{PRE}$) pin. These pins are ideal for parity bus interfacing in high perfance systems. When $\overline{MR}$ is Low, the outputs are Low if all $\overline{OE}$ pins are Low. When $\overline{MR}$ is High, data can be entered into the latch. When $\overline{PRE}$ is Low, the outputs are High if all $\overline{OE}$ pins are Low. $\overline{PRE}$ overrides $\overline{MR}$.

FUNCTION TABLE

INPUTS					OUTPUTS	OPERATING MODE
$\overline{OE}_n$	$\overline{PRE}$	$\overline{MR}$	LE	D_n	Q_n	
H	X	X	X	X	Z	High-Z
L	L	X	X	X	H	Preset
L	H	L	X	X	L	Clear
L L	H H	H H	H H	L H	L H	Transparent
L L	H H	H H	↓ ↓	l h	L H	Latched
L	H	H	L	X	NC	Hold

H = High voltage level
h = High voltage level one setup time prior to the High-to-Low transition of LE
L = Low voltage level
l = Low voltage level one setup time prior to the High-to-Low transition of LE
X = Don't Care
Z = High-impedance
↓ = High-to-Low transition
NC = No change

LOGIC DIAGRAM



RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	74AC11845			74ACT11845			UNIT
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	DC supply voltage	3.0[1]	5.0	5.5	4.5	5.0	5.5	V
V_I	Input voltage	0		V_{CC}	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	0		V_{CC}	V
$\Delta t/\Delta v$	Input transition rise or fall rate	0		10	0		10	ns/V
T_A	Operating free-air temperature	-40		+85	-40		+85	°C

NOTE:

1. No electrical or switching characteristics are specified at $V_{CC} < 3V$. Operation between 2V and 3V is not recommended, but within that range, a device output will maintain a previously established logic state.

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	TEST CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 to+7.0	V
I_{IK} or V_I	DC input diode current[2]	$V_I < 0$	-20	mA
		$V_I > V_{CC}$	20	
	DC input voltage		-0.5 to V_{CC} +0.5	V
I_{OK} or V_O	DC output diode current[2]	$V_O < 0$	-50	mA
		$V_O > V_{CC}$	50	
	DC output voltage		-0.5 to V_{CC} +0.5	V
I_O	DC output source or sink current per output pin	V_O = 0 to V_{CC}	±50	mA
I_{CC} or I_{GND}	DC V_{CC} current		±200	mA
	DC ground current		±200	
T_{STG}	Storage temperature		-65 to 150	°C
P_{TOT}	Power dissipation per package Plastic DIP	Above 70°C:derate linearly by 8mW/K	500	mW
	Power dissipation per package Plastic surface mount (SO)	Above 70°C:derate linearly by 6mW/K	400	mW

NOTES:

1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		V_{CC}	74AC11845				74ACT11845				UNIT
					T_A = +25°C		T_A = -40°C to +85°C		T_A = +25°C		T_A = -40°C to +85°C		
				V	Min	Max	Min	Max	Min	Max	Min	Max	
V_{IH}	High-level input voltage			3.0	2.10		2.10						V
				4.5	3.15		3.15		2.0		2.0		
				5.5	3.85		3.85		2.0		2.0		
V_{IL}	Low-level input voltage			3.0		0.90		0.90					V
				4.5		1.35		1.35		0.8		0.8	
				5.5		1.65		1.65		0.8		0.8	
V_{OH}	High-level output voltage	V_I = V_{IL} or V_{IH}	I_{OH} = -50μA	3.0	2.9		2.9						V
				4.5	4.4		4.4		4.4		4.4		
				5.5	5.4		5.4		5.4		5.4		
			I_{OH} = -4mA	3.0	2.58		2.48						
			I_{OH} = -24mA	4.5	3.94		3.8		3.94		3.8		
				5.5	4.94		4.8		4.94		4.8		
			I_{OH} = -75mA[1]	5.5			3.85				3.85		
V_{OL}	Low-level output voltage	V_I = V_{IL} or V_{IH}	I_{OL} = 50μA	3.0		0.1		0.1					V
				4.5		0.1		0.1		0.1		0.1	
				5.5		0.1		0.1		0.1		0.1	
			I_{OL} = 12mA	3.0		0.36		0.44					
			I_{OL} = 24mA	4.5		0.36		0.44		0.36		0.44	
				5.5		0.36		0.44		0.36		0.44	
			I_{OL} = 75mA[1]	5.5				1.65				1.65	
I_I	Input leakage current	V_I = V_{CC} or GND		5.5		±0.1		±1.0		±0.1		±1.0	μA
I_{OZ}	3-State output off-state current	V_I = V_{IL} or V_{IH}; V_O = V_{CC} or GND		5.5		±0.5		±5.0		±0.5		±5.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC} or GND, I_O = 0		5.5		8.0		80		8.0		80	μA
ΔI_{CC}	Supply current, TTL inputs High[2]	One input at 3.4V, other inputs at V_{CC} or GND		5.5						0.9		1.0	mA

NOTES:

1. Not more than one output should be tested at a time, and the duration of the test should not exceed 10ms.
2. This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0V or V_{CC}.

74AC/ACT11846

Octal D-Type Transparent Latch with Set and Reset; 3-State; INV

Objective Specification

FEATURES

- **High-speed parallel registers with positive edge-triggered D-type flip-flops**
- **Output capability: ±24mA**
- **CMOS (AC) and TTL (ACT) voltage level inputs**
- **50Ω incident wave switching**
- **Center-pin V_{CC} and ground configuration to minimize high-speed switching noise**
- **I_{CC} category: MSI**

DESCRIPTION

The 74AC/ACT11846 high-performance CMOS devices combine very high speed and high output drive comparable to the most advanced TTL families.

The AC/ACT11846 consists of eight D-type latches with 3-State outputs. The flip-flops appear transparent to the data when Latch Enable (LE) is High. This allows asynchronous operation, as the output transition follows the data in transition. On the LE High-to-Low transition, the data that meets the setup and hold time is latched.

Data appears on the bus when the three

GENERAL INFORMATION

SYMBOL	PARAMETER	CONDITIONS T_A = 25°C; GND = 0V; V_{CC} = 5.0V		TYPICAL AC	TYPICAL ACT	UNIT
t_{PLH}/t_{PHL}	Propagation delay LE to $\overline{Q}_n$	C_L = 50pF		8.7	10.5	ns
C_{PD}	Power dissipation capacitance per latch[1]	f = 1MHz;	Enabled	54	54	pF
		C_L = 50pF	Disabled	32	32	
C_{IN}	Input capacitance	V_I = 0V or V_{CC}		4.5	4.5	pF
C_{OUT}	Output capacitance	V_O = 0V or V_{CC}; Disabled		10	10	pF
I_{LATCH}	Latch-up current	Per Jedec JC40.2 Standard 17		500	500	mA

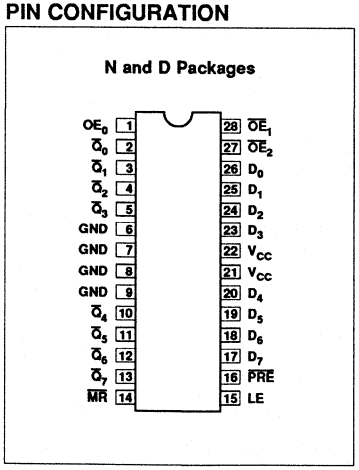
Note:

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_I + \Sigma (C_L \times V_{CC}^2 \times f_O)$ where:
   f_I = input frequency in MHz, C_L = output load capacitance in pF,
   f_O = output frequency in MHz, V_{CC} = supply voltage in V,
   $\Sigma (C_L \times V_{CC}^2 \times f_O)$ = sum of outputs

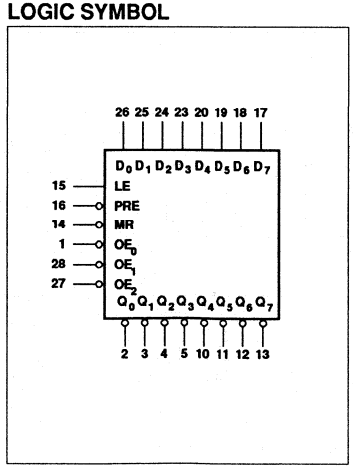
ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE
28-pin plastic DIP (300mil-wide)	-40°C to +85°C	74AC11846N 74ACT11846N
28-pin plastic SO (300mil-wide)	-40°C to +85°C	74AC11846D 74ACT11846D

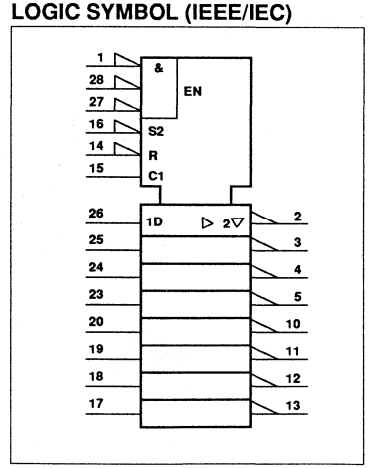
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



Octal D-Type Transparent Latch with Set and Reset; 3-State; INV

74AC/ACT11846

PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
1, 28, 27	$\overline{OE}_0$, $\overline{OE}_1$, $\overline{OE}_2$	Output enable inputs (active-Low)
15	LE	Latch enable input
16	$\overline{PRE}$	Preset input (active-Low)
14	$\overline{MR}$	Master reset input (active-Low)
2, 3, 4, 5, 10, 11, 12, 13	D_0 - D_7	Data inputs
26, 25, 24, 23, 20, 19, 18, 17	$\overline{Q}_0$ - $\overline{Q}_7$	Data outputs
6, 7, 8, 9	GND	Ground (0V)
21, 22	V_{CC}	Positive supply voltage

Output Enable pins ($\overline{OE}_0$, $\overline{OE}_1$, $\overline{OE}_2$) are Low. When any $\overline{OE}_n$ is High the output is in the high-impedance state.

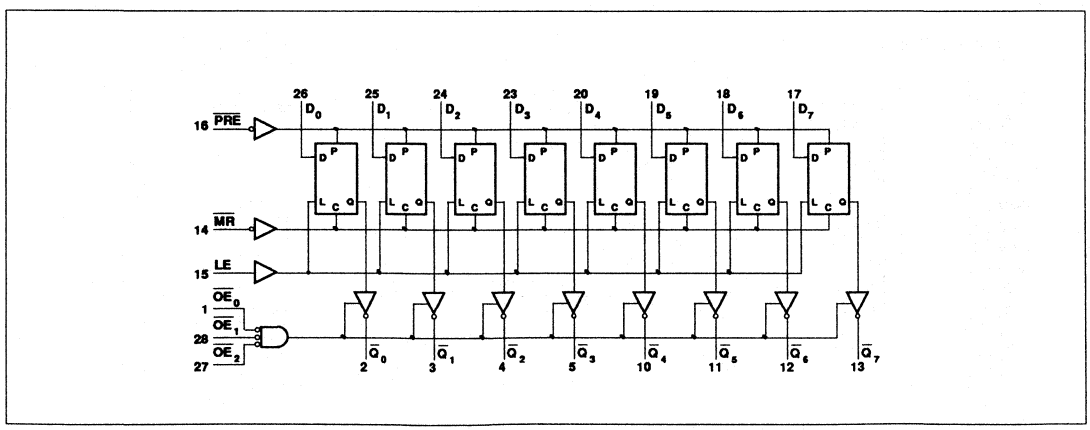
The AC/ACT11846 also features a Master Rest ($\overline{MR}$) pin and a Preset ($\overline{PRE}$) pin. These pins are ideal for parity bus interfacing in high perfance systems. When $\overline{MR}$ is Low, the outputs are High if all $\overline{OE}$ pins are Low. When $\overline{MR}$ is High, data can be entered into the latch. When $\overline{PRE}$ is Low, the outputs are Low if all $\overline{OE}$ pins are Low. $\overline{PRE}$ overrides $\overline{MR}$.

FUNCTION TABLE

INPUTS					OUTPUTS	OPERATING MODE
$\overline{OE}_n$	$\overline{PRE}$	$\overline{MR}$	LE	D_n	$\overline{Q}_n$	
H	X	X	X	X	Z	High-Z
L	L	X	X	X	L	Preset
L	H	L	X	X	H	Clear
L L	H H	H H	H H	L H	H L	Transparent
L L	H H	H H	↓ ↓	l h	H L	Latched
L	H	H	L	X	NC	Hold

H = High voltage level
h = High voltage level one setup time prior to the High-to-Low transition of LE
L = Low voltage level
l = Low voltage level one setup time prior to the High-to-Low transition of LE
X = Don't Care
Z = High-impedance
↓ = High-to-Low transition
NC = No change

LOGIC DIAGRAM



RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	74AC11846			74ACT11846			UNIT
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	DC supply voltage	3.0[1]	5.0	5.5	4.5	5.0	5.5	V
V_I	Input voltage	0		V_{CC}	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	0		V_{CC}	V
$\Delta t/\Delta v$	Input transition rise or fall rate	0		10	0		10	ns/V
T_A	Operating free-air temperature	-40		+85	-40		+85	°C

NOTE:

1. No electrical or switching characteristics are specified at V_{CC} < 3V. Operation between 2V and 3V is not recommended, but within that range, a device output will maintain a previously established logic state.

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	TEST CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 to+7.0	V
I_{IK} or V_I	DC input diode current[2]	$V_I < 0$	-20	mA
		$V_I > V_{CC}$	20	
	DC input voltage		-0.5 to V_{CC} +0.5	V
I_{OK} or V_O	DC output diode current[2]	$V_O < 0$	-50	mA
		$V_O > V_{CC}$	50	
	DC output voltage		-0.5 to V_{CC} +0.5	V
I_O	DC output source or sink current per output pin	V_O = 0 to V_{CC}	±50	mA
I_{CC} or I_{GND}	DC V_{CC} current		±200	mA
	DC ground current		±200	
T_{STG}	Storage temperature		-65 to 150	°C
P_{TOT}	Power dissipation per package Plastic DIP	Above 70°C:derate linearly by 8mW/K	500	mW
	Power dissipation per package Plastic surface mount (SO)	Above 70°C:derate linearly by 6mW/K	400	mW

NOTES:

1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		V_{CC}	74AC11846				74ACT11846				UNIT
					T_A = +25°C		T_A = -40°C to +85°C		T_A = +25°C		T_A = -40°C to +85°C		
				V	Min	Max	Min	Max	Min	Max	Min	Max	
V_{IH}	High-level input voltage			3.0	2.10		2.10						V
				4.5	3.15		3.15		2.0		2.0		
				5.5	3.85		3.85		2.0		2.0		
V_{IL}	Low-level input voltage			3.0		0.90		0.90					V
				4.5		1.35		1.35		0.8		0.8	
				5.5		1.65		1.65		0.8		0.8	
V_{OH}	High-level output voltage	V_I = V_{IL} or V_{IH}	I_{OH} = -50μA	3.0	2.9		2.9						V
				4.5	4.4		4.4		4.4		4.4		
				5.5	5.4		5.4		5.4		5.4		
			I_{OH} = -4mA	3.0	2.58		2.48						
			I_{OH} = -24mA	4.5	3.94		3.8		3.94		3.8		
				5.5	4.94		4.8		4.94		4.8		
			I_{OH} = -75mA[1]	5.5			3.85				3.85		
V_{OL}	Low-level output voltage	V_I = V_{IL} or V_{IH}	I_{OL} = 50μA	3.0		0.1		0.1					V
				4.5		0.1		0.1		0.1		0.1	
				5.5		0.1		0.1		0.1		0.1	
			I_{OL} = 12mA	3.0		0.36		0.44					
			I_{OL} = 24mA	4.5		0.36		0.44		0.36		0.44	
				5.5		0.36		0.44		0.36		0.44	
			I_{OL} = 75mA[1]	5.5				1.65				1.65	
I_I	Input leakage current	V_I = V_{CC} or GND		5.5		±0.1		±1.0		±0.1		±1.0	μA
I_{OZ}	3-State output off-state current	V_I = V_{IL} or V_{IH}, V_O = V_{CC} or GND		5.5		±0.5		±5.0		±0.5		±5.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC} or GND, I_O = 0		5.5		8.0		80		8.0		80	μA
ΔI_{CC}	Supply current, TTL inputs High[2]	One input at 3.4V, other inputs at V_{CC} or GND		5.5						0.9		1.0	mA

NOTES:

1. Not more than one output should be tested at a time, and the duration of the test should not exceed 10ms.
2. This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0V or V_{CC}.

74AC/ACT11861

10-Wide Transceiver; 3-State

Objective Specification

FEATURES

- **High-speed bus interface buffering for wide address/data paths or buses carrying parity**
- **Output capability: ±24mA**
- **CMOS (AC) and TTL (ACT) voltage level inputs**
- **50Ω incident wave switching**
- **Center-pin V_{CC} and ground configuration to minimize high-speed switching noise**
- **I_{CC} category: MSI**

DESCRIPTION

The 74AC/ACT11861 high-performance CMOS devices combine very high speed and high output drive comparable to the most advanced TTL families.

The AC/ACT11861 Bus Interface Register provides extra data width (10-wide) for wider address/data paths or buses carrying parity.

GENERAL INFORMATION

SYMBOL	PARAMETER	CONDITIONS T_A = 25°C; GND = 0V; V_{CC} = 5.0V		TYPICAL AC	TYPICAL ACT	UNIT
t_{PLH}/t_{PHL}	Propagation delay A_n to B_n or B_n to A_n	C_L = 50pF		6.6	7.7	ns
C_{PD}	Power dissipation capacitance per transceiver[1]	f = 1MHz;	Enabled	46	40	pF
		C_L = 50pF	Disabled	10	8	pF
C_{IN}	Input capacitance	V_I = 0V or V_{CC}		4.5	4.5	pF
$C_{I/O}$	I/O capacitance	$V_{I/O}$ = 0V or V_{CC}; Disabled		12	12	pF
I_{LATCH}	Latch-up current	Per Jedec JC40.2 Standard 17		500	500	mA

Note:

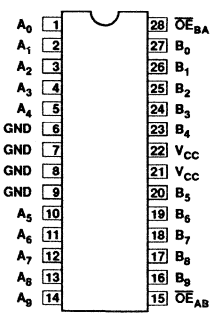
1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_I + \Sigma (C_L \times V_{CC}^2 \times f_O)$ where:
   f_I = input frequency in MHz, C_L = output load capacitance in pF,
   f_O = output frequency in MHz, V_{CC} = supply voltage in V,
   $\Sigma (C_L \times V_{CC}^2 \times f_O)$ = sum of outputs

ORDERING INFORMATION

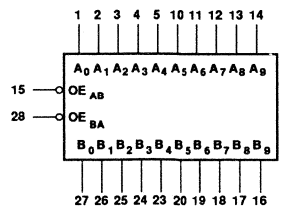
PACKAGES	TEMPERATURE RANGE	ORDER CODE
28-pin plastic DIP (300mil-wide)	-40°C to +85°C	74AC11861N 74ACT11861N
28-pin plastic SO (300mil-wide)	-40°C to +85°C	74AC11861D 74ACT11861D

PIN CONFIGURATION

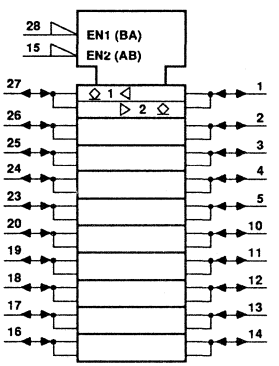
N and D Packages



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



PIN DESCRIPTION

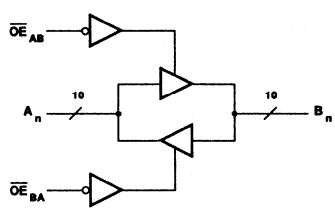
PIN NUMBER	SYMBOL	NAME AND FUNCTION
15	$\overline{OE}_{AB}$	A-to-B output enable input (active Low)
28	$\overline{OE}_{BA}$	B-to-A output enable input (active Low)
1, 2, 3, 4, 5, 10, 11, 12, 13, 14	A_0 - A_9	Data inputs/outputs (A side)
27, 26, 25, 24, 23, 20, 19, 18, 17	B_0 - B_9	Data inputs/outputs (B side)
6, 7, 8, 9	GND	Ground (0V)
21, 22	V_{CC}	Positive supply voltage

FUNCTION TABLE

INPUTS		MODE OF OPERATION
$\overline{OE}_{AB}$	$\overline{OE}_{BA}$	
L	H	A data to B bus
H	L	B data to A bus
H	H	Z

H = High voltage level
L = Low volatge level
Z = High-impedance (OFF) state

LOGIC DIAGRAM



RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	74AC11861			74ACT11861			UNIT
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	DC supply voltage	3.0[1]	5.0	5.5	4.5	5.0	5.5	V
V_I	Input voltage	0		V_{CC}	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	0		V_{CC}	V
$\Delta t/\Delta v$	Input transition rise or fall rate	0		10	0		10	ns/V
T_A	Operating free-air temperature	-40		+85	-40		+85	°C

NOTE:
1. No electrical or switching characteristics are specified at V_{CC} < 3V. Operation between 2V and 3V is not recommended, but within that range, a device output will maintain a previously established logic state.

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	TEST CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 to+7.0	V
I_{IK} or V_I	DC input diode current[2]	$V_I < 0$	-20	mA
		$V_I > V_{CC}$	20	
	DC input voltage		-0.5 to V_{CC} +0.5	V
I_{OK} or V_O	DC output diode current[2]	$V_O < 0$	-50	mA
		$V_O > V_{CC}$	50	
	DC output voltage		-0.5 to V_{CC} +0.5	V
I_O	DC output source or sink current per output pin	V_O = 0 to V_{CC}	±50	mA
I_{CC} or I_{GND}	DC V_{CC} current		±250	mA
	DC ground current		±250	
T_{STG}	Storage temperature		-65 to 150	°C
P_{TOT}	Power dissipation per package Plastic DIP	Above 70°C:derate linearly by 8mW/K	500	mW
	Power dissipation per package Plastic surface mount (SO)	Above 70°C:derate linearly by 6mW/K	400	mW

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		V_{CC}	74AC11861				74ACT11861				UNIT
					T_A = +25°C		T_A = -40°C to +85°C		T_A = +25°C		T_A = -40°C to +85°C		
				V	Min	Max	Min	Max	Min	Max	Min	Max	
V_{IH}	High-level input voltage			3.0	2.10		2.10						V
				4.5	3.15		3.15		2.0		2.0		
				5.5	3.85		3.85		2.0		2.0		
V_{IL}	Low-level input voltage			3.0		0.90		0.90					V
				4.5		1.35		1.35		0.8		0.8	
				5.5		1.65		1.65		0.8		0.8	
V_{OH}	High-level output voltage	V_I = V_{IL} or V_{IH}	I_{OH} = -50μA	3.0	2.9		2.9						V
				4.5	4.4		4.4		4.4		4.4		
				5.5	5.4		5.4		5.4		5.4		
			I_{OH} = -4mA	3.0	2.58		2.48						
			I_{OH} = -24mA	4.5	3.94		3.8		3.94		3.8		
				5.5	4.94		4.8		4.94		4.8		
			I_{OH} = -75mA[1]	5.5			3.85				3.85		
V_{OL}	Low-level output voltage	V_I = V_{IL} or V_{IH}	I_{OL} = 50μA	3.0		0.1		0.1					V
				4.5		0.1		0.1		0.1		0.1	
				5.5		0.1		0.1		0.1		0.1	
			I_{OL} = 12mA	3.0		0.36		0.44					
			I_{OL} = 24mA	4.5		0.36		0.44		0.36		0.44	
				5.5		0.36		0.44		0.36		0.44	
			I_{OL} = 75mA[1]	5.5				1.65				1.65	
I_I	Input leakage current	V_I = V_{CC} or GND		5.5		±0.1		±1.0		±0.1		±1.0	μA
I_{OZ}	3-State output off-state current	V_I = V_{IL} or V_{IH}, V_O = V_{CC} or GND		5.5		±0.5		±5.0		±0.5		±5.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC} or GND, I_O = 0		5.5		8.0		80		8.0		80	μA
ΔI_{CC}	Supply current, TTL inputs High[2]	One input at 3.4V, other inputs at V_{CC} or GND		5.5						0.9		1.0	mA

NOTES:
1. Not more than one output should be tested at a time, and the duration of the test should not exceed 10ms.
2. This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0V or V_{CC}.

74AC/ACT11862

10-Wide Transceiver; 3-State; INV

Objective Specification

FEATURES

- **High-speed bus interface buffering for wide address/data paths or buses carrying parity**
- **Output capability: ±24mA**
- **CMOS (AC) and TTL (ACT) voltage level inputs**
- **50Ω incident wave switching**
- **Center-pin V_{CC} and ground configuration to minimize high-speed switching noise**
- **I_{CC} category: MSI**

DESCRIPTION

The 74AC/ACT11862 high-performance CMOS devices combine very high speed and high output drive comparable to the most advanced TTL families.

The AC/ACT11862 inverting Bus Interface Register provides extra data width (10-wide) for wider address/data paths or buses carrying parity.

GENERAL INFORMATION

SYMBOL	PARAMETER	CONDITIONS T_A = 25°C; GND = 0V; V_{CC} = 5.0V		TYPICAL AC	TYPICAL ACT	UNIT
t_{PLH}/t_{PHL}	Propagation delay A_n to $\overline{B}_n$ or B_n to $\overline{A}_n$	C_L = 50pF		6.4	7.9	ns
C_{PD}	Power dissipation capacitance per transceiver[1]	f = 1MHz; C_L = 50pF	Enabled	40	45	pF
			Disabled	8	11	
C_{IN}	Input capacitance	V_I = 0V or V_{CC}		4.5	4.5	pF
$C_{I/O}$	I/O capacitance	$V_{I/O}$ = 0V or V_{CC}; Disabled		12	12	pF
I_{LATCH}	Latch-up current	Per Jedec JC40.2 Standard 17		500	500	mA

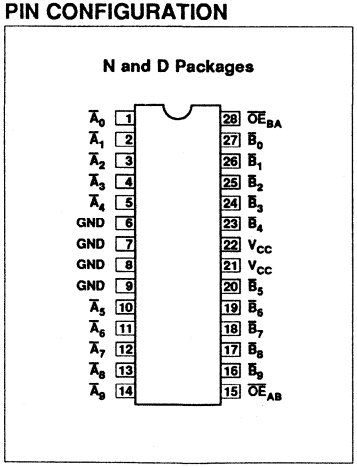
Note:

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_I + \Sigma (C_L \times V_{CC}^2 \times f_O)$ where:
   f_I = input frequency in MHz, C_L = output load capacitance in pF,
   f_O = output frequency in MHz, V_{CC} = supply voltage in V,
   $\Sigma (C_L \times V_{CC}^2 \times f_O)$ = sum of outputs

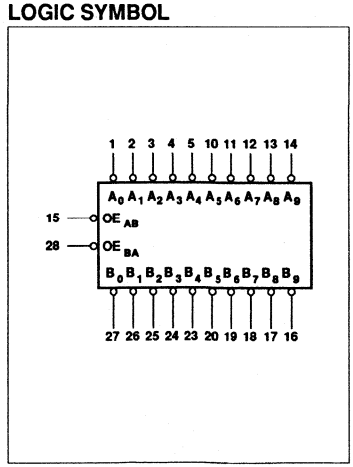
ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE
28-pin plastic DIP (300mil-wide)	-40°C to +85°C	74AC11862N 74ACT11862N
28-pin plastic SO (300mil-wide)	-40°C to +85°C	74AC11862D 74ACT11862D

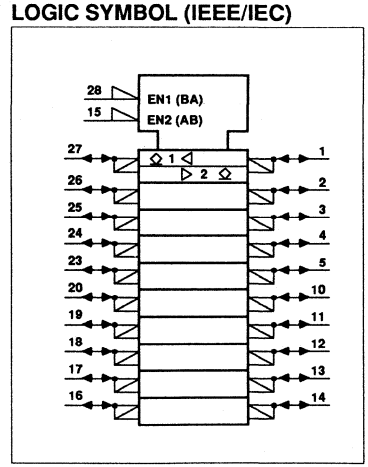
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



PIN DESCRIPTION

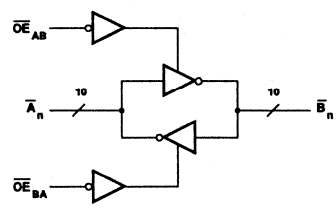
PIN NUMBER	SYMBOL	NAME AND FUNCTION
15	$\overline{OE}_{AB}$	A-to-B output enable input (active Low)
28	$\overline{OE}_{BA}$	B-to-A output enable input (active Low)
1, 2, 3, 4, 5, 10, 11, 12, 13, 14	$\overline{A}_0$ - $\overline{A}_9$	Data inputs/outputs (A side)
27, 26, 25, 24, 23, 20, 19, 18, 17	$\overline{B}_0$ - $\overline{B}_9$	Data inputs/outputs (B side)
6, 7, 8, 9	GND	Ground (0V)
21, 22	V_{CC}	Positive supply voltage

FUNCTION TABLE

INPUTS		MODE OF OPERATION
$\overline{OE}_{AB}$	$\overline{OE}_{BA}$	
L	H	$\overline{A}$ data to B bus
H	L	$\overline{B}$ data to A bus
H	H	Z

H = High voltage level
L = Low volatge level
Z = High-impedance (OFF) state

LOGIC DIAGRAM



RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	74AC11862			74ACT11862			UNIT
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	DC supply voltage	3.0[1]	5.0	5.5	4.5	5.0	5.5	V
V_I	Input voltage	0		V_{CC}	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	0		V_{CC}	V
$\Delta t/\Delta v$	Input transition rise or fall rate	0		10	0		10	ns/V
T_A	Operating free-air temperature	-40		+85	-40		+85	°C

NOTE:
1. No electrical or switching characteristics are specified at $V_{CC} < 3V$. Operation between 2V and 3V is not recommended, but within that range, a device output will maintain a previously established logic state.

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	TEST CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 to+7.0	V
I_{IK} or V_I	DC input diode current[2]	$V_I < 0$	-20	mA
		$V_I > V_{CC}$	20	
	DC input voltage		-0.5 to V_{CC} +0.5	V
I_{OK} or V_O	DC output diode current[2]	$V_O < 0$	-50	mA
		$V_O > V_{CC}$	50	
	DC output voltage		-0.5 to V_{CC} +0.5	V
I_O	DC output source or sink current per output pin	V_O = 0 to V_{CC}	±50	mA
I_{CC} or I_{GND}	DC V_{CC} current		±250	mA
	DC ground current		±250	
T_{STG}	Storage temperature		-65 to 150	°C
P_{TOT}	Power dissipation per package Plastic DIP	Above 70°C:derate linearly by 8mW/K	500	mW
	Power dissipation per package Plastic surface mount (SO)	Above 70°C:derate linearly by 6mW/K	400	mW

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		V_{CC}	74AC11862				74ACT11862				UNIT
					T_A = +25°C		T_A = -40°C to +85°C		T_A = +25°C		T_A = -40°C to +85°C		
				V	Min	Max	Min	Max	Min	Max	Min	Max	
V_{IH}	High-level input voltage			3.0	2.10		2.10						V
				4.5	3.15		3.15		2.0		2.0		
				5.5	3.85		3.85		2.0		2.0		
V_{IL}	Low-level input voltage			3.0		0.90		0.90					V
				4.5		1.35		1.35		0.8		0.8	
				5.5		1.65		1.65		0.8		0.8	
V_{OH}	High-level output voltage	V_I = V_{IL} or V_{IH}	I_{OH} = -50µA	3.0	2.9		2.9						V
				4.5	4.4		4.4		4.4		4.4		
				5.5	5.4		5.4		5.4		5.4		
			I_{OH} = -4mA	3.0	2.58		2.48						
			I_{OH} = -24mA	4.5	3.94		3.8		3.94		3.8		
				5.5	4.94		4.8		4.94		4.8		
			I_{OH} = -75mA[1]	5.5			3.85				3.85		
V_{OL}	Low-level output voltage	V_I = V_{IL} or V_{IH}	I_{OL} = 50µA	3.0		0.1		0.1					V
				4.5		0.1		0.1		0.1		0.1	
				5.5		0.1		0.1		0.1		0.1	
			I_{OL} = 12mA	3.0		0.36		0.44					
			I_{OL} = 24mA	4.5		0.36		0.44		0.36		0.44	
				5.5		0.36		0.44		0.36		0.44	
			I_{OL} = 75mA[1]	5.5				1.65				1.65	
I_I	Input leakage current	V_I = V_{CC} or GND		5.5		±0.1		±1.0		±0.1		±1.0	µA
I_{OZ}	3-State output off-state current	V_I = V_{IL} or V_{IH}, V_O = V_{CC} or GND		5.5		±0.5		±5.0		±0.5		±5.0	µA
I_{CC}	Quiescent supply current	V_I = V_{CC} or GND, I_O = 0		5.5		8.0		80		8.0		80	µA
ΔI_{CC}	Supply current, TTL inputs High[2]	One input at 3.4V, other inputs at V_{CC} or GND		5.5						0.9		1.0	mA

NOTES:
1. Not more than one output should be tested at a time, and the duration of the test should not exceed 10ms.
2. This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0V or V_{CC}.

74AC/ACT11863

9-Wide Transceiver; 3-State

Objective Specification

FEATURES

- **High-speed bus interface buffering for wide address/data paths or buses carrying parity**
- **Output capability: ±24mA**
- **CMOS (AC) and TTL (ACT) voltage level inputs**
- **50Ω incident wave switching**
- **Center-pin V_{CC} and ground configuration to minimize high-speed switching noise**
- **I_{CC} category: MSI**

DESCRIPTION

The 74AC/ACT11863 high-performance CMOS devices combine very high speed and high output drive comparable to the most advanced TTL families.

The AC/ACT11863 Bus Interface Register provides extra data width (9-wide) for wider address/data paths or buses carrying parity. It has NORed Transmit and Receive Output Enables for maximum control flexibility.

GENERAL INFORMATION

SYMBOL	PARAMETER	CONDITIONS T_A = 25°C; GND = 0V; V_{CC} = 5.0V		TYPICAL AC	TYPICAL ACT	UNIT
t_{PLH}/t_{PHL}	Propagation delay A_n to B_n or B_n to A_n	C_L = 50pF		6.6	7.7	ns
C_{PD}	Power dissipation capacitance per transceiver[1]	f = 1MHz;	Enabled	46	40	pF
		C_L = 50pF	Disabled	10	8	pF
C_{IN}	Input capacitance	V_I = 0V or V_{CC}		4.5	4.5	pF
$C_{I/O}$	I/O capacitance	$V_{I/O}$ = 0V or V_{CC}; Disabled		12	12	pF
I_{LATCH}	Latch-up current	Per Jedec JC40.2 Standard 17		500	500	mA

Note:

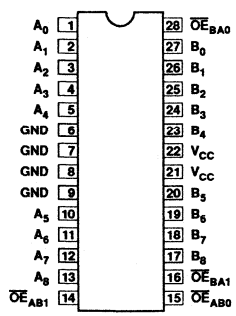
1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_I + \Sigma (C_L \times V_{CC}^2 \times f_O)$ where:
   f_I = input frequency in MHz, C_L = output load capacitance in pF,
   f_O = output frequency in MHz, V_{CC} = supply voltage in V,
   $\Sigma (C_L \times V_{CC}^2 \times f_O)$ = sum of outputs

ORDERING INFORMATION

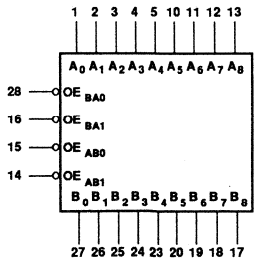
PACKAGES	TEMPERATURE RANGE	ORDER CODE
28-pin plastic DIP (300mil-wide)	-40°C to +85°C	74AC11863N 74ACT11863N
28-pin plastic SO (300mil-wide)	-40°C to +85°C	74AC11863D 74ACT11863D

PIN CONFIGURATION

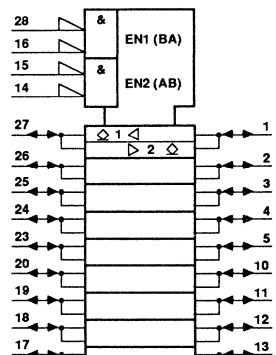
N and D Packages



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



PIN DESCRIPTION

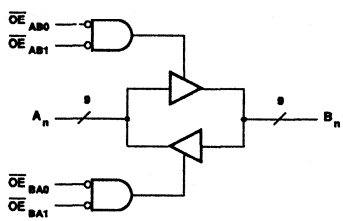
PIN NUMBER	SYMBOL	NAME AND FUNCTION
15, 14	$\overline{OE}_{AB0}$, $\overline{OE}_{AB1}$	A-to-B output enable inputs (active Low)
28, 16	$\overline{OE}_{BA0}$, $\overline{OE}_{BA1}$	B-to-A output enable inputs (active Low)
1, 2, 3, 4, 5, 10, 11, 12, 13	A_0 - A_8	Data inputs/outputs (A side)
27, 26, 25, 24, 23, 20, 19, 18, 17	B_0 - B_8	Data inputs/outputs (B side)
6, 7, 8, 9	GND	Ground (0V)
21, 22	V_{CC}	Positive supply voltage

FUNCTION TABLE

INPUTS				MODE OF OPERATION
$\overline{OE}_{AB0}$	$\overline{OE}_{AB1}$	$\overline{OE}_{BA0}$	$\overline{OE}_{BA1}$	
L	L	H	X	A data to B bus
L	L	X	H	
H	X	L	L	B data to A bus
X	H	L	L	
H	H	H	H	Z

H = High voltage level
L = Low voltage level
X = Don't care
Z = High-impedance state

LOGIC DIAGRAM



RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	74AC11863			74ACT11863			UNIT
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	DC supply voltage	3.0[1]	5.0	5.5	4.5	5.0	5.5	V
V_I	Input voltage	0		V_{CC}	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	0		V_{CC}	V
$\Delta t/\Delta v$	Input transition rise or fall rate	0		10	0		10	ns/V
T_A	Operating free-air temperature	-40		+85	-40		+85	°C

NOTE:

1. No electrical or switching characteristics are specified at V_{CC} < 3V. Operation between 2V and 3V is not recommended, but within that range, a device output will maintain a previously established logic state.

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	TEST CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 to+7.0	V
I_{IK} or V_I	DC input diode current[2]	V_I < 0	-20	mA
		V_I > V_{CC}	20	
	DC input voltage		-0.5 to V_{CC} +0.5	V
I_{OK} or V_O	DC output diode current[2]	V_O < 0	-50	mA
		V_O > V_{CC}	50	
	DC output voltage		-0.5 to V_{CC} +0.5	V
I_O	DC output source or sink current per output pin	V_O = 0 to V_{CC}	±50	mA
I_{CC} or I_{GND}	DC V_{CC} current		±225	mA
	DC ground current		±225	
T_{STG}	Storage temperature		-65 to 150	°C
P_{TOT}	Power dissipation per package Plastic DIP	Above 70°C:derate linearly by 8mW/K	500	mW
	Power dissipation per package Plastic surface mount (SO)	Above 70°C:derate linearly by 6mW/K	400	mW

NOTES:

1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		V_{CC}	74AC11863				74ACT11863				UNIT
					T_A = +25°C		T_A = -40°C to +85°C		T_A = +25°C		T_A = -40°C to +85°C		
				V	Min	Max	Min	Max	Min	Max	Min	Max	
V_{IH}	High-level input voltage			3.0	2.10		2.10						V
				4.5	3.15		3.15		2.0		2.0		
				5.5	3.85		3.85		2.0		2.0		
V_{IL}	Low-level input voltage			3.0		0.90		0.90					V
				4.5		1.35		1.35		0.8		0.8	
				5.5		1.65		1.65		0.8		0.8	
V_{OH}	High-level output voltage	V_I = V_{IL} or V_{IH}	I_{OH} = -50μA	3.0	2.9		2.9						V
				4.5	4.4		4.4		4.4		4.4		
				5.5	5.4		5.4		5.4		5.4		
			I_{OH} = -4mA	3.0	2.58		2.48						
			I_{OH} = -24mA	4.5	3.94		3.8		3.94		3.8		
				5.5	4.94		4.8		4.94		4.8		
			I_{OH} = -75mA[1]	5.5			3.85				3.85		
V_{OL}	Low-level output voltage	V_I = V_{IL} or V_{IH}	I_{OL} = 50μA	3.0		0.1		0.1					V
				4.5		0.1		0.1		0.1		0.1	
				5.5		0.1		0.1		0.1		0.1	
			I_{OL} = 12mA	3.0		0.36		0.44					
			I_{OL} = 24mA	4.5		0.36		0.44		0.36		0.44	
				5.5		0.36		0.44		0.36		0.44	
			I_{OL} = 75mA[1]	5.5				1.65				1.65	
I_I	Input leakage current	V_I = V_{CC} or GND		5.5		±0.1		±1.0		±0.1		±1.0	μA
I_{OZ}	3-State output off-state current	V_I = V_{IL} or V_{IH}; V_O = V_{CC} or GND		5.5		±0.5		±5.0		±0.5		±5.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC} or GND, I_O = 0		5.5		8.0		80		8.0		80	μA
ΔI_{CC}	Supply current, TTL inputs High[2]	One input at 3.4V, other inputs at V_{CC} or GND		5.5						0.9		1.0	mA

NOTES:
1. Not more than one output should be tested at a time, and the duration of the test should not exceed 10ms.
2. This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0V or V_{CC}.

74AC/ACT11864

9-Wide Transceiver; 3-State; INV

Objective Specification

FEATURES

- **High-speed bus interface buffering for wide address/data paths or buses carrying parity**
- **Output capability: ±24mA**
- **CMOS (AC) and TTL (ACT) voltage level inputs**
- **50Ω incident wave switching**
- **Center-pin V_{CC} and ground configuration to minimize high-speed switching noise**
- **I_{CC} category: MSI**

DESCRIPTION

The 74AC/ACT11864 high-performance CMOS devices combine very high speed and high output drive comparable to the most advanced TTL families.

The AC/ACT11864 inverting Bus Interface Register provides extra data width (9-wide) for wider address/data paths or buses carrying parity. It has NORed Transmit and Receive Output Enables for maximum control flexibility.

GENERAL INFORMATION

SYMBOL	PARAMETER	CONDITIONS T_A = 25°C; GND = 0V; V_{CC} = 5.0V		TYPICAL AC	TYPICAL ACT	UNIT
t_{PLH}/t_{PHL}	Propagation delay A_n to $\overline{B}_n$ or B_n to $\overline{A}_n$	C_L = 50pF		6.4	7.9	ns
C_{PD}	Power dissipation capacitance per transceiver[1]	f = 1MHz; C_L = 50pF	Enabled	40	45	pF
			Disabled	8	11	
C_{IN}	Input capacitance	V_I = 0V or V_{CC}		4.5	4.5	pF
$C_{I/O}$	I/O capacitance	$V_{I/O}$ = 0V or V_{CC}; Disabled		12	12	pF
I_{LATCH}	Latch-up current	Per Jedec JC40.2 Standard 17		500	500	mA

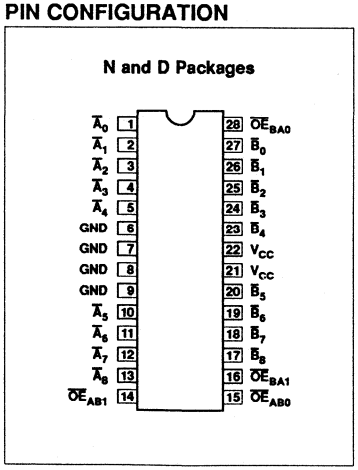
Note:

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_I + \Sigma (C_L \times V_{CC}^2 \times f_O)$ where:
   f_I = input frequency in MHz, C_L = output load capacitance in pF,
   f_O = output frequency in MHz, V_{CC} = supply voltage in V,
   $\Sigma (C_L \times V_{CC}^2 \times f_O)$ = sum of outputs

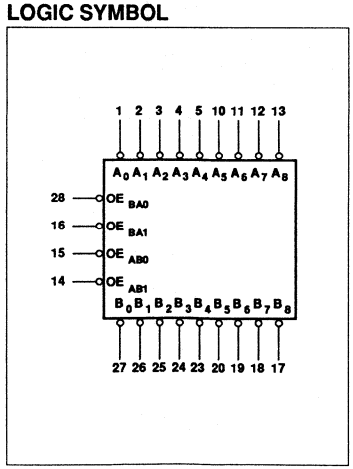
ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE
28-pin plastic DIP (300mil-wide)	-40°C to +85°C	74AC11864N 74ACT11864N
28-pin plastic SO (300mil-wide)	-40°C to +85°C	74AC11864D 74ACT11864D

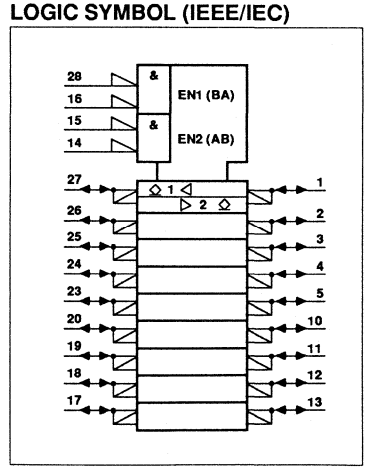
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



PIN DESCRIPTION

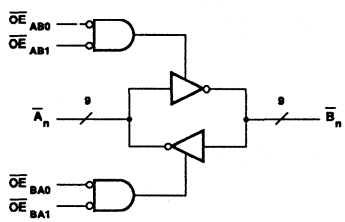
PIN NUMBER	SYMBOL	NAME AND FUNCTION
15, 14	$\overline{OE}_{AB0}$, $\overline{OE}_{AB1}$	A-to-B output enable inputs (active Low)
28, 16	$\overline{OE}_{BA0}$, $\overline{OE}_{BA1}$	B-to-A output enable inputs (active Low)
1, 2, 3, 4, 5, 10, 11, 12, 13	$\overline{A}_0$ - $\overline{A}_8$	Data inputs/outputs (A side)
27, 26, 25, 24, 23, 20, 19, 18, 17	$\overline{B}_0$ - $\overline{B}_8$	Data inputs/outputs (B side)
6, 7, 8, 9	GND	Ground (0V)
21, 22	V_{CC}	Positive supply voltage

FUNCTION TABLE

INPUTS				MODE OF OPERATION
$\overline{OE}_{AB0}$	$\overline{OE}_{AB1}$	$\overline{OE}_{BA0}$	$\overline{OE}_{BA1}$	
L	L	H	X	$\overline{A}$ data to B bus
L	L	X	H	
H	X	L	L	$\overline{B}$ data to A bus
X	H	L	L	
H	H	H	H	Z

H = High voltage level
L = Low voltage level
X = Don't care
Z = High-impedance state

LOGIC DIAGRAM



RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	74AC11864			74ACT11864			UNIT
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	DC supply voltage	3.0[1]	5.0	5.5	4.5	5.0	5.5	V
V_I	Input voltage	0		V_{CC}	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	0		V_{CC}	V
$\Delta t/\Delta v$	Input transition rise or fall rate	0		10	0		10	ns/V
T_A	Operating free-air temperature	-40		+85	-40		+85	°C

NOTE:

1. No electrical or switching characteristics are specified at V_{CC} < 3V. Operation between 2V and 3V is not recommended, but within that range, a device output will maintain a previously established logic state.

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	TEST CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 to+7.0	V
I_{IK} or V_I	DC input diode current[2]	$V_I < 0$	-20	mA
		$V_I > V_{CC}$	20	
	DC input voltage		-0.5 to V_{CC} +0.5	V
I_{OK} or V_O	DC output diode current[2]	$V_O < 0$	-50	mA
		$V_O > V_{CC}$	50	
	DC output voltage		-0.5 to V_{CC} +0.5	V
I_O	DC output source or sink current per output pin	V_O = 0 to V_{CC}	±50	mA
I_{CC} or I_{GND}	DC V_{CC} current		±225	mA
	DC ground current		±225	
T_{STG}	Storage temperature		-65 to 150	°C
P_{TOT}	Power dissipation per package Plastic DIP	Above 70°C:derate linearly by 8mW/K	500	mW
	Power dissipation per package Plastic surface mount (SO)	Above 70°C:derate linearly by 6mW/K	400	mW

NOTES:

1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		V_{CC}	74AC11864				74ACT11864				UNIT
					T_A = +25°C		T_A = -40°C to +85°C		T_A = +25°C		T_A = -40°C to +85°C		
				V	Min	Max	Min	Max	Min	Max	Min	Max	
V_{IH}	High-level input voltage			3.0	2.10		2.10						V
				4.5	3.15		3.15		2.0		2.0		
				5.5	3.85		3.85		2.0		2.0		
V_{IL}	Low-level input voltage			3.0		0.90		0.90					V
				4.5		1.35		1.35		0.8		0.8	
				5.5		1.65		1.65		0.8		0.8	
V_{OH}	High-level output voltage	V_I = V_{IL} or V_{IH}	I_{OH} = -50μA	3.0	2.9		2.9						V
				4.5	4.4		4.4		4.4		4.4		
				5.5	5.4		5.4		5.4		5.4		
			I_{OH} = -4mA	3.0	2.58		2.48						
			I_{OH} = -24mA	4.5	3.94		3.8		3.94		3.8		
				5.5	4.94		4.8		4.94		4.8		
			I_{OH} = -75mA[1]	5.5			3.85				3.85		
V_{OL}	Low-level output voltage	V_I = V_{IL} or V_{IH}	I_{OL} = 50μA	3.0		0.1		0.1					V
				4.5		0.1		0.1		0.1		0.1	
				5.5		0.1		0.1		0.1		0.1	
			I_{OL} = 12mA	3.0		0.36		0.44					
			I_{OL} = 24mA	4.5		0.36		0.44		0.36		0.44	
				5.5		0.36		0.44		0.36		0.44	
			I_{OL} = 75mA[1]	5.5				1.65				1.65	
I_I	Input leakage current	V_I = V_{CC} or GND		5.5		±0.1		±1.0		±0.1		±1.0	μA
I_{OZ}	3-State output off-state current	V_I = V_{IL} or V_{IH}, V_O = V_{CC} or GND		5.5		±0.5		±5.0		±0.5		±5.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC} or GND, I_O = 0		5.5		8.0		80		8.0		80	μA
ΔI_{CC}	Supply current, TTL inputs High[2]	One input at 3.4V, other inputs at V_{CC} or GND		5.5						0.9		1.0	mA

NOTES:
1. Not more than one output should be tested at a time, and the duration of the test should not exceed 10ms.
2. This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0V or V_{CC}.

74AC/ACT11898

10-Bit Serial-In Parallel-Out Shift Register

Preliminary Specification

FEATURES

- **Gated serial data inputs**
- **Fully buffered clock and data inputs**
- **Fully synchronous data transfers**
- **Typical shift frequency of 100MHz**
- **Asynchronous master reset**
- **Output capability: ±24mA**
- **CMOS (AC) and TTL (ACT) voltage level inputs**
- **50Ω incident wave switching**
- **Center-pin V_{CC} and ground configuration to minimize high-speed switching noise**
- **I_{CC} category: MSI**

DESCRIPTION

The 74AC/ACT11898 high-performance CMOS devices combine very high speed and high output drive comparable to the most advanced TTL families.

The 74AC/ACT11898 10-bit Serial-In Parallel-Out Shift Register is an edge-triggered shift register with serial data entry and an output from each of the 10 stages. Data is entered serially through one of two inputs (A • B); either input can be used as an active-High enable for data entry through the other input. Otherwise

GENERAL INFORMATION

SYMBOL	PARAMETER	CONDITIONS T_A = 25°C; GND = 0V; V_{CC} = 5.0V	TYPICAL		UNIT
			AC	ACT	
t_{PLH}/t_{PHL}	Propagation delay CP to Q_n ($\overline{MR}$ = High)	C_L = 50pF	6.6	7.6	ns
C_{PD}	Power dissipation capacitance[1]	f = 1MHz; C_L = 50pF	122	117	pF
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	4.0	4.0	pF
I_{LATCH}	Latch-up current	Per Jedec JC40.2 Standard 17	500	500	mA
f_{MAX}	Maximum clock frequency	C_L = 50pF	100	90	MHz

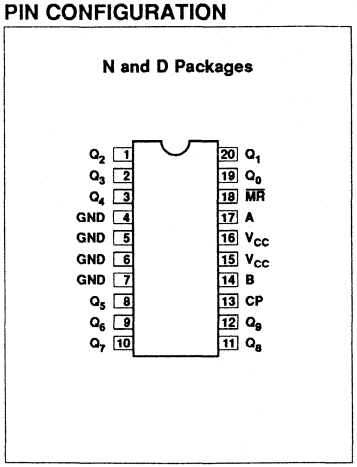
Note:

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_I + \Sigma (C_L \times V_{CC}^2 \times f_O)$ where:
   f_I = input frequency in MHz, C_L = output load capacitance in pF,
   f_O = output frequency in MHz, V_{CC} = supply voltage in V,
   $\Sigma (C_L \times V_{CC}^2 \times f_O)$ = sum of outputs

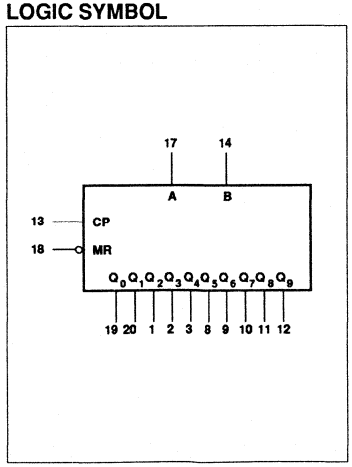
ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE
20-pin plastic DIP (300mil-wide)	-40°C to +85°C	74AC11898N 74ACT11898N
20-pin plastic SO (300mil-wide)	-40°C to +85°C	74AC11898D 74ACT11898D

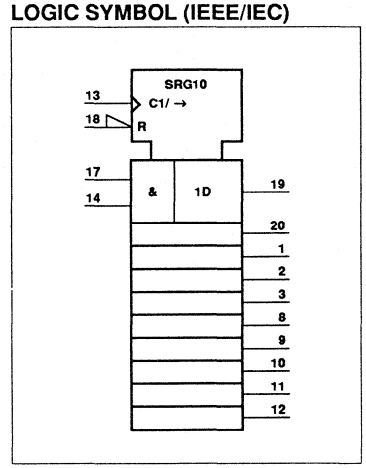
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



both inputs must be connected to the input data or an unused input must be tied High.

Data shifts one place to the right on each Low-to-High transition of the Clock (CP) input and enters the logical AND of the two inputs (A • B) that existed one setup time before the rising clock edge into Q_0.

A Low level on the Master Reset ($\overline{MR}$) input overrides all other inputs and clears the register asynchronously, forcing all outputs Low.

PIN DESCRIPTION

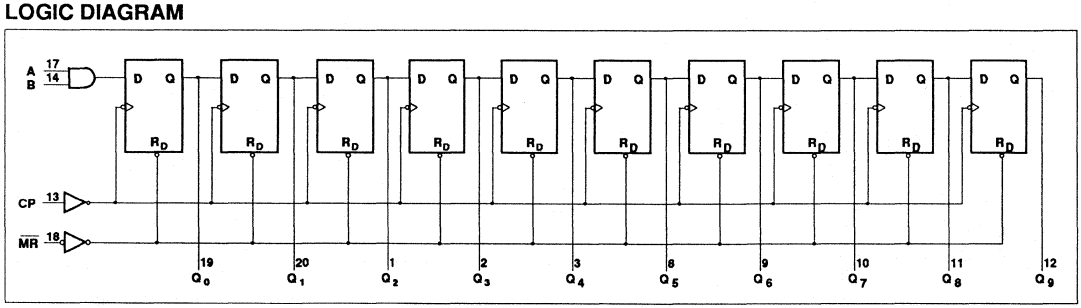
PIN NUMBER	SYMBOL	NAME AND FUNCTION
18	$\overline{MR}$	Asynchronous master reset (active Low)
13	CP	Clock input (Low-to-High, edge-triggered)
17, 14	A, B	Data inputs
19, 20, 1, 2, 3, 8, 9, 10, 11, 12	Q_0 - Q_9	Parallel outputs outputs
4, 5, 6, 7	GND	Ground (0V)
15, 16	V_{CC}	Positive supply voltage

FUNCTION TABLE

OPERATING MODE	INPUTS				OUTPUTS			
	$\overline{MR}$	CP	A	B	Q_0	Q_1	—	Q_9
Reset (clear)	L	X	X	X	L	L	—	L
Shift	H	↑	l	l	L	q_0	—	q_9
	H	↑	l	h	L	q_0	—	q_9
	H	↑	h	l	L	q_0	—	q_9
	H	↑	h	h	H	q_0	—	q_9

H = High voltage level
L = Low voltage level
h = High voltage level one setup time prior to the Low-to High clock transition
l = Low voltage level one setup time prior to the Low-to High clock transition
X = Don't care
q_n = State of the referenced input (or output) one setup time prior to the Low-to-High clock transition
↑ = Low-to-High clock transition

LOGIC DIAGRAM



RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	74AC11898			74ACT11898			UNIT
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	DC supply voltage	3.0[1]	5.0	5.5	4.5	5.0	5.5	V
V_I	Input voltage	0		V_{CC}	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	0		V_{CC}	V
$\Delta t/\Delta v$	Input transition rise or fall rate	0		10	0		10	ns/V
T_A	Operating free-air temperature	-40		+85	-40		+85	°C

NOTE:
1. No electrical or switching characteristics are specified at $V_{CC} < 3V$. Operation between 2V and 3V is not recommended, but within that range, a device output will maintain a previously established logic state.

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	TEST CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 to+7.0	V
I_{IK} or V_I	DC input diode current[2]	$V_I < 0$	-20	mA
		$V_I > V_{CC}$	20	
	DC input voltage		-0.5 to V_{CC} +0.5	V
I_{OK} or V_O	DC output diode current[2]	$V_O < 0$	-50	mA
		$V_O > V_{CC}$	50	
	DC output voltage		-0.5 to V_{CC} +0.5	V
I_O	DC output source or sink current per output pin	V_O = 0 to V_{CC}	±50	mA
I_{CC} or I_{GND}	DC V_{CC} current		±250	mA
	DC ground current		±250	
T_{STG}	Storage temperature		-65 to 150	°C
P_{TOT}	Power dissipation per package Plastic DIP	Above 70°C:derate linearly by 8mW/K	500	mW
	Power dissipation per package Plastic surface mount (SO)	Above 70°C:derate linearly by 6mW/K	400	mW

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		V_{CC}	74AC11898				74ACT11898				UNIT
					T_A = +25°C		T_A = -40°C to +85°C		T_A = +25°C		T_A = -40°C to +85°C		
				V	Min	Max	Min	Max	Min	Max	Min	Max	
V_{IH}	High-level input voltage			3.0	2.10		2.10						V
				4.5	3.15		3.15		2.0		2.0		
				5.5	3.85		3.85		2.0		2.0		
V_{IL}	Low-level input voltage			3.0		0.90		0.90					V
				4.5		1.35		1.35		0.8		0.8	
				5.5		1.65		1.65		0.8		0.8	
V_{OH}	High-level output voltage	V_I = V_{IL} or V_{IH}	I_{OH} = -50μA	3.0	2.9		2.9						V
				4.5	4.4		4.4		4.4		4.4		
				5.5	5.4		5.4		5.4		5.4		
			I_{OH} = -4mA	3.0	2.58		2.48						
			I_{OH} = -24mA	4.5	3.94		3.8		3.94		3.8		
				5.5	4.94		4.8		4.94		4.8		
			I_{OH} = -75mA[1]	5.5			3.85				3.85		
V_{OL}	Low-level output voltage	V_I = V_{IL} or V_{IH}	I_{OL} = 50μA	3.0		0.1		0.1					V
				4.5		0.1		0.1		0.1		0.1	
				5.5		0.1		0.1		0.1		0.1	
			I_{OL} = 12mA	3.0		0.36		0.44					
			I_{OL} = 24mA	4.5		0.36		0.44		0.36		0.44	
				5.5		0.36		0.44		0.36		0.44	
			I_{OL} = 75mA[1]	5.5				1.65				1.65	
I_I	Input leakage current	V_I = V_{CC} or GND		5.5		±0.1		±1.0		±0.1		±1.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC} or GND, I_O = 0		5.5		8.0		80		8.0		80	μA
ΔI_{CC}	Supply current, TTL inputs High[2]	One input at 3.4V, other inputs at V_{CC} or GND		5.5						0.9		1.0	mA

NOTES:
1. Not more than one output should be tested at a time, and the duration of the test should not exceed 10ms.
2. This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0V or V_{CC}.

AC ELECTRICAL CHARACTERISTICS AT 3.3V ±0.3V

SYMBOL	PARAMETER	WAVEFORM	74AC11898					UNIT
			T_A = +25°C			T_A = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	1	50	70		50		MHz
t_{PLH} t_{PHL}	Propagation delay CP to Q_n	1	1.5 1.5	8.9 8.8	10.8 10.7	1.5 1.5	11.8 11.6	ns
t_{PHL}	Propagation delay $\overline{MR}$ to Q_n	2	1.5	9.6	11.5	1.5	12.6	ns
t_S	Setup time, High or Low A, B to CP	3	13.5			13.5		ns
t_H	Hold time, High or Low A, B to CP	3	0.0			0.0		ns
t_W	Clock pulse width (shift) High or Low	1	10.0			10.0		ns
t_W	$\overline{MR}$ pulse width, Low	2	3.0			3.0		ns
t_{REC}	Recovery time $\overline{MR}$ to CP	2	1.5			1.5		ns

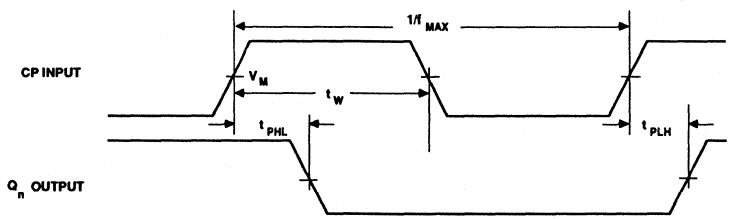
AC ELECTRICAL CHARACTERISTICS AT 5.0V ±0.5V

SYMBOL	PARAMETER	WAVEFORM	74AC11898					UNIT
			T_A = +25°C			T_A = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	1	80	100		80		MHz
t_{PLH} t_{PHL}	Propagation delay CP to Q_n	1	1.5 1.5	6.4 6.8	8.0 8.4	1.5 1.5	8.8 9.2	ns
t_{PHL}	Propagation delay $\overline{MR}$ to Q_n	2	1.5	7.2	8.9	1.5	9.6	ns
t_S	Setup time, High or Low A, B to CP	3	8.5			8.5		ns
t_H	Hold time, High or Low A, B to CP	3	0.0			0.0		ns
t_W	Clock pulse width (shift) High or Low	1	6.3			6.3		ns
t_W	$\overline{MR}$ pulse width, Low	2	2.5			2.5		ns
t_{REC}	Recovery time $\overline{MR}$ to CP	2	1.5			1.5		ns

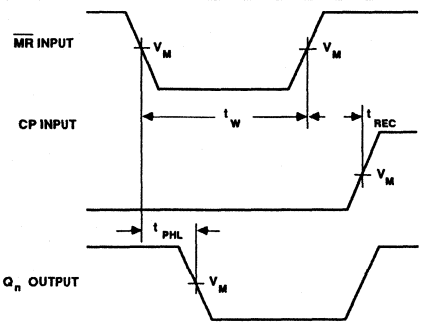
AC ELECTRICAL CHARACTERISTICS AT 5.0V ±0.5V

SYMBOL	PARAMETER	WAVEFORM	74ACT11898					UNIT
			T_A = +25°C			T_A = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	1	70	90		70		MHz
t_{PLH} t_{PHL}	Propagation delay CP to Q_n	1	1.5 1.5	7.5 7.7	9.0 9.1	1.5 1.5	9.8 10.0	ns
t_{PHL}	Propagation delay $\overline{MR}$ to Q_n	2	1.5	9.5	11.0	1.5	11.9	ns
t_S	Setup time, High or Low A, B to CP	3	9.5			9.5		ns
t_H	Hold time, High or Low A, B to CP	3	0.0			0.0		ns
t_W	Clock pulse width (shift) High or Low	1	7.1			7.1		ns
t_W	$\overline{MR}$ pulse width, Low	2	4.0			4.0		ns
t_{REC}	Recovery time $\overline{MR}$ to CP	2	1.5			1.5		ns

AC WAVEFORMS

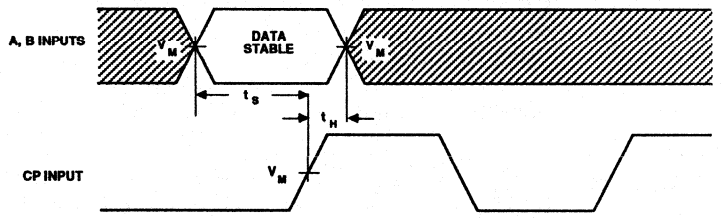


Waveform 1. Waveforms Showing Clock to Outputs Propagation Delays and Clock Pulse Width



Waveform 2. Waveforms Showing the Master Reset ($\overline{MR}$) Pulse Width, the Master Reset to Output (Q_n) Propagation Delays, and the Master Reset to Clock (CP) Recovery Time

AC WAVEFORMS (Continued)

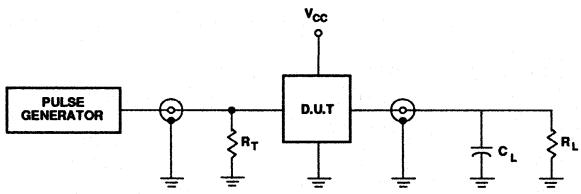


Waveform 3. Waveforms Showing the Data Set-up and Hold Times for the InputS (A,B)

WAVEFORM CONDITIONS

	INPUTS	OUTPUTS
AC	V_{IN} = GND to V_{CC}, V_M = 50% V_{CC}	V_{OUT} = V_{OL} to V_{OH}
ACT	V_{IN} = GND to 3.0V, V_M = 1.5V	V_M = 50% V_{CC}

TEST CIRCUIT



Test Circuit

DEFINITIONS

C_L = Load capacitance, 50pF; includes jig and probe capacitance

R_L = Load resistor, 500Ω

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators

Input pulses: PRR ≤ 10MHz

$t_r = t_f$ = 3ns

74AC/ACT11979

8-Bit Multiplexed I/O Read-Back Register

Objective Specification

FEATURES

- **Octal bus interface**
- **3-State buffers**
- **Output capability: ±24 mA**
- **CMOS (AC) and TTL (ACT) voltage level inputs**
- **50Ω incident wave switching**
- **Center-pin V_{CC} and ground configuration to minimize high-speed switching noise**
- **I_{CC} category: MSI**

DESCRIPTION

The 74AC/ACT11979 high-performance CMOS devices combine very high speed and high output drive comparable to the most advanced TTL families.

The 74AC/ACT11979 device is an 8-bit multiplexed I/O read-back register. When the Output Enable ($\overline{OE}$) input is held High, it loads data on the rising edge of the Clock (CP). When the Clock is held High or Low, the data is held in the registers. When the Output Enable is Low, the data held in the register is visible on the I/O pins (I/O_n).

GENERAL INFORMATION

SYMBOL	PARAMETER	CONDITIONS T_A = 25°C; GND = 0V V_{CC} = 5.0V		TYPICAL AC	TYPICAL ACT	UNIT
t_{PZH}/ t_{PZL}	Propagation delay $\overline{OE}$ to I/O_n	C_L = 50pF		5.3	5.6	ns
C_{PD}	Power dissipation capacitance[1]	f = 1MHz; C_L = 50pF	Enabled	135	135	pF
			Disabled	40	40	
C_{IN}	Input capacitance	V_I = 0V or V_{CC}		3.5	3.5	pF
$C_{I/O}$	I/O capacitance	$V_{I/O}$ = 0V or V_{CC}; Disabled		8.5	8.5	pF
I_{LATCH}	Latch-up current	Per Jedec JC40.2 Standard 17		500	500	mA

Note:

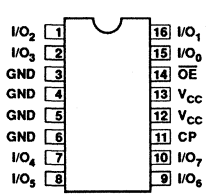
1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_I + \Sigma (C_L \times V_{CC}^2 \times f_O)$ where:
   f_I = input frequency in MHz, C_L = output load capacitance in pF,
   f_O = output frequency in MHz, V_{CC} = supply voltage in V,
   $\Sigma (C_L \times V_{CC}^2 \times f_O)$ = sum of outputs

ORDERING INFORMATION

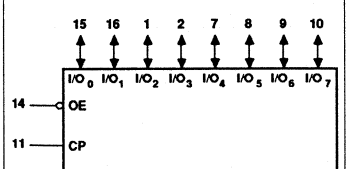
PACKAGES	TEMPERATURE RANGE	ORDER CODE
16-pin plastic DIP (300mil-wide)	-40°C to +85°C	74AC11979N 74ACT11979N
16-pin plastic SO (150mil-wide)	-40°C to +85°C	74AC11979D 74ACT11979D

PIN CONFIGURATION

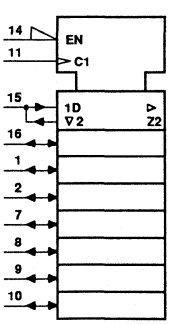
N and D Packages



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



PIN DESCRIPTION

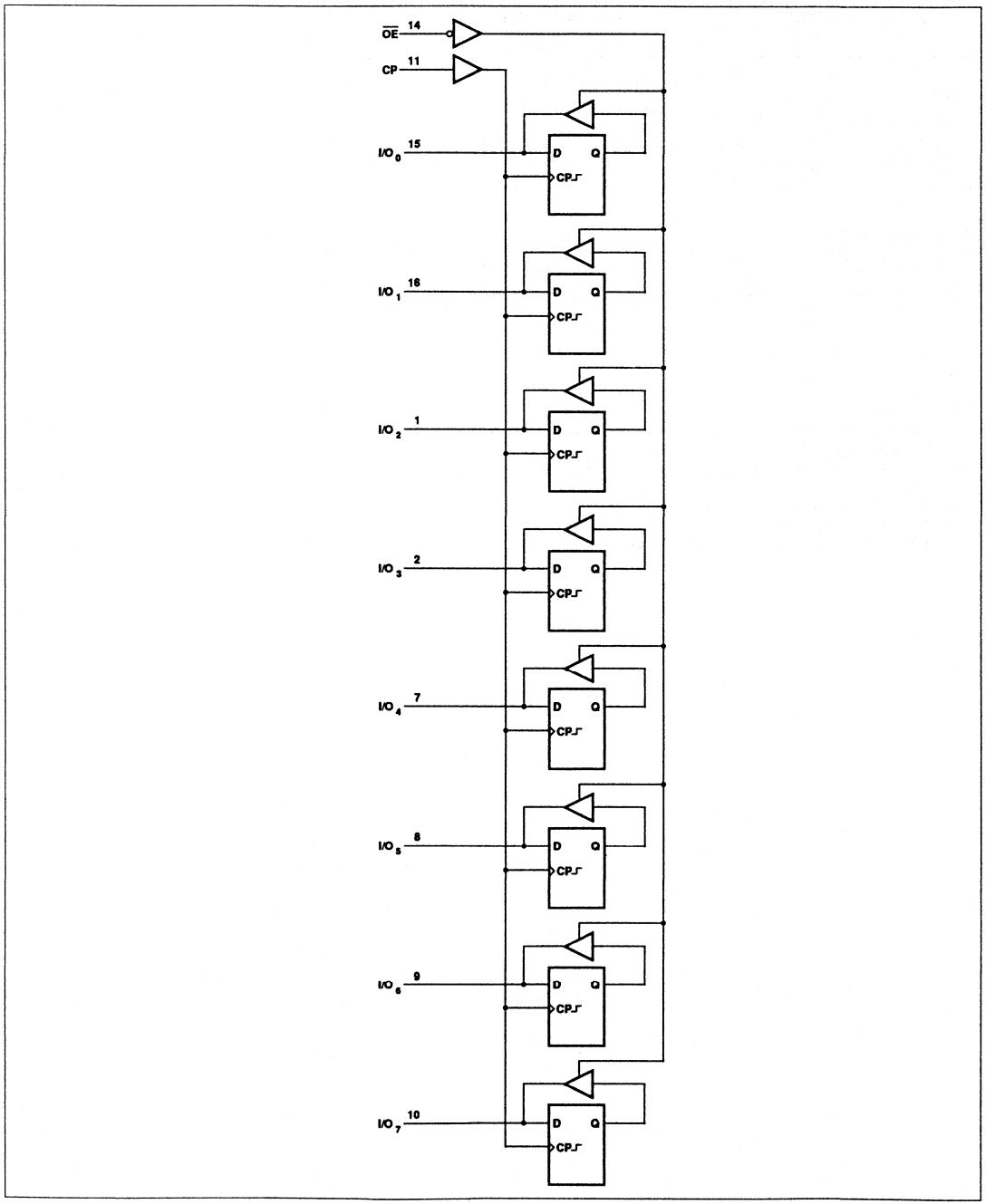
PIN NUMBER	SYMBOL	NAME AND FUNCTION
14	$\overline{OE}$	Output enable input (active Low)
11	CP	Clock input
15, 16, 1, 2 7, 8, 9, 10	I/O_0 - I/O_7	Data inputs/outputs (3-state)
3, 4, 5, 6	GND	Ground (0V)
12, 13	V_{CC}	Positive supply voltage

FUNCTION TABLE

$\overline{OE}$	CP	I/O_n	OPERATION
L	X*	Data out	Output data
H	↑	l h	Load data
H	H L	Z	Hold data

H = High voltage level
h = High voltage level one set-up time prior to the Low-to-High clock transition
L = Low volatge level
l = Low voltage level one set-up time prior to the Low-to-High clock transition
X = Don't care
↑ = Low-to-High clock transition
Z = High-impedance (OFF) state
* The register is loaded on any Low-to-High transition

LOGIC DIAGRAM



RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	74AC11979			74ACT11979			UNIT
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	DC supply voltage	3.0[1]	5.0	5.5	4.5	5.0	5.5	V
V_I	Input voltage	0		V_{CC}	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	0		V_{CC}	V
$\Delta t/\Delta v$	Input transition rise or fall rate	0		10	0		10	ns/V
T_A	Operating free-air temperature	-40		+85	-40		+85	°C

NOTE:
1. No electrical or switching characteristics are specified at $V_{CC} < 3V$. Operation between 2V and 3V is not recommended, but within that range, a device output will maintain a previously established logic state.

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	TEST CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 to+7.0	V
I_{IK} or V_I	DC input diode current[2]	$V_I < 0$	-20	mA
		$V_I > V_{CC}$	20	
	DC input voltage		-0.5 to V_{CC} +0.5	V
I_{OK} or V_O	DC output diode current[2]	$V_O < 0$	-50	mA
		$V_O > V_{CC}$	50	
	DC output voltage		-0.5 to V_{CC} +0.5	V
I_O	DC output source or sink current per output pin	V_O = 0 to V_{CC}	±50	mA
I_{CC} or I_{GND}	DC V_{CC} current		±200	mA
	DC ground current		±200	
T_{STG}	Storage temperature		-65 to 150	°C
P_{TOT}	Power dissipation per package Plastic DIP	Above 70°C:derate linearly by 8mW/K	500	mW
	Power dissipation per package Plastic surface mount (SO)	Above 70°C:derate linearly by 6mW/K	400	mW

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		V_{CC}	74AC11979				74ACT11979				UNIT
					T_A = +25°C		T_A = -40°C to +85°C		T_A = +25°C		T_A = -40°C to +85°C		
				V	Min	Max	Min	Max	Min	Max	Min	Max	
V_{IH}	High-level input voltage			3.0	2.10		2.10						V
				4.5	3.15		3.15		2.0		2.0		
				5.5	3.85		3.85		2.0		2.0		
V_{IL}	Low-level input voltage			3.0		0.90		0.90					V
				4.5		1.35		1.35		0.8		0.8	
				5.5		1.65		1.65		0.8		0.8	
V_{OH}	High-level output voltage	V_I = V_{IL} or V_{IH}	I_{OH} = -50μA	3.0	2.9		2.9						V
				4.5	4.4		4.4		4.4		4.4		
				5.5	5.4		5.4		5.4		5.4		
			I_{OH} = -4mA	3.0	2.58		2.48						
			I_{OH} = -24mA	4.5	3.94		3.8		3.94		3.8		
				5.5	4.94		4.8		4.94		4.8		
			I_{OH} = -75mA[1]	5.5			3.85				3.85		
V_{OL}	Low-level output voltage	V_I = V_{IL} or V_{IH}	I_{OL} = 50μA	3.0		0.1		0.1					V
				4.5		0.1		0.1		0.1		0.1	
				5.5		0.1		0.1		0.1		0.1	
			I_{OL} = 12mA	3.0		0.36		0.44					
			I_{OL} = 24mA	4.5		0.36		0.44		0.36		0.44	
				5.5		0.36		0.44		0.36		0.44	
			I_{OL} = 75mA[1]	5.5				1.65				1.65	
I_I	Input leakage current	V_I = V_{CC} or GND		5.5		±0.1		±1.0		±0.1		±1.0	μA
I_{OZ}	3-State output off-state current	V_I = V_{IL} or V_{IH}; V_O = V_{CC} or GND		5.5		±0.5		±5.0		±0.5		±5.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC} or GND, I_O = 0		5.5		8.0		80		8.0		80	μA
ΔI_{CC}	Supply current, TTL inputs High[2]	One input at 3.4V, other inputs at V_{CC} or GND		5.5						0.9		1.0	mA

NOTES:
1. Not more than one output should be tested at a time, and the duration of the test should not exceed 10ms.
2. This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0V or V_{CC}.

Section 6
Application Notes

INDEX

AN600
Handling Precautions

Application Note

ELECTROSTATIC CHARGES

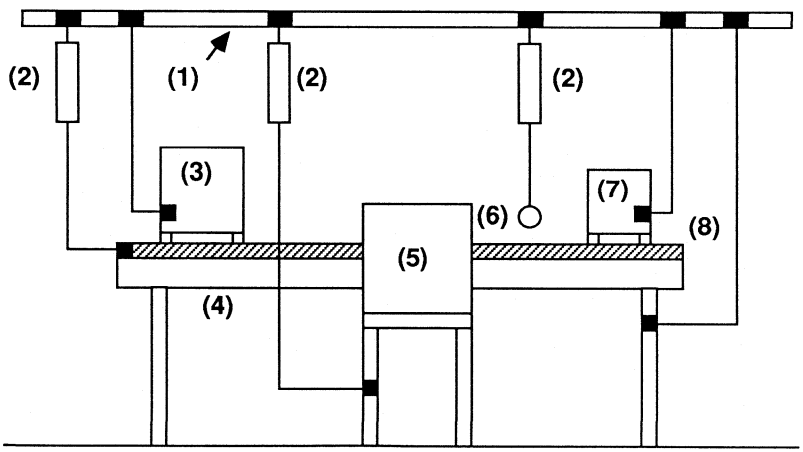
Electrostatic charges can be stored in many things; for example, man-made fiber clothing, moving machinery, objects with air blowing across them, plastic storage bins, sheets of paper stored in plastic envelopes, paper from electrostatic copying machines, and people. The charges are caused by friction between two surfaces, at least one of which is non-conductive. The magnitude and polarity of the charges depends on the different affinities for electrons of the two materials rubbing together, the friction force and the humidity of the surrounding air.

Electrostatic discharge is the transfer of an electrostatic charge between bodies at different potentials and occurs with direct contact or when induced by an electrostatic field. All of our CMOS ICs are internally protected against electrostatic discharge, but they can be damaged if the following precautions are not taken.

WORK STATION

Figure 1 shows a working area suitable for safety handling electrostatic sensitive devices. It has a work bench, the surface of which is conductive or covered by an antistatic sheet. Typical resistivity for the bench surface is 1kΩ to 0.5MΩ per cm^2. The floor should also be covered with antistatic material. The following precautions should be observed:

- Persons at a work-bench should be grounded via a wrist strap and a resistor.
- All electrical equipment should be connected to the mains via a ground-leakage switch and the equipment cases should be grounded.
- Relative humidity should be maintained between 50% and 65%.
- An ionizer should be used to neutralize objects with immobile static charges.



NOTES:
1. Grounding rail
2. Resistor (500kΩ ±10%, 0.5W)
3. Ionizer
4. Work bench
5. Chair
6. Wrist strap
7. Electrical equipment
8. Conductive surface/antistatic sheet

Figure 1. Protected Work Station

Handling Precautions

RECEIPT AND STORAGE

CMOS ICs are packed for dispatch in antistatic/conductive boxes, rails or blister tape. The fact that the ICs are sensitive to electrostatic discharge is shown by warning labels on both primary and secondary packing.

The ICs should be kept in their original packing while in storage. If a bulk container is partially unpacked, the tasks should be performed at a protected work station. Any CMOS ICs that are temporarily stored should be packed in conductive or antistatic packing or carriers.

ASSEMBLY

CMOS ICs must be removed from their protective packing with grounded component-pincers or short-circuit clips. Short-circuit clips must remain in place during mounting, soldering and cleansing/drying processes. Do not remove more ICs from the storage packing than are needed at any one time. Production/assembly documents should state that the product contains electrostatic sensitive devices and that special precautions need to be taken.

During assembly, ensure that the CMOS ICs are the last of the components to be mounted and that this is done at a protected work station.

All tools used during assembly, including soldering tools and solder baths, must be grounded. All hand-tools should be of conductive or antistatic material and, where possible, not insulated.

Measuring and testing of completed circuit boards must be done at a protected work station. Place the soldered side of the circuit board on conductive or antistatic foam and remove the short-circuit clips. Remove the circuit board from the foam, holding the board only at the edges. Make sure the circuit board does not touch the conductive surface of the work bench. After testing, replace the circuit board on the conductive foam to await packing.

Handle assembled circuit boards containing CMOS ICs in the same way as unmounted CMOS ICs. They should also carry warning labels and be packed in conductive or antistatic packing.

AN601
Simultaneous Switching Evaluation of Advanced CMOS Logic

Application Note

Introduction

The purpose of this paper is to define what Simultaneous Switching Evaluation (SSE) is, why it is tested, and how it is tested for the Advanced CMOS Logic (ACL) family of integrated circuits.

Why Should SSE be Performed

The purpose of SSE is to evaluate what effect switching more than one output simultaneously has on the performance of the circuit. SSE becomes important in any high-performance line of circuits because the propagation delays and output edge rates are very fast.

Fast edge rates can team up with parasitic inductances to produce unwanted side effects such as output disturbances and/or performance degradations. Output disturbances can manifest themselves in the form of glitches or bumps from solid low levels near or above the low threshold of a subsequent device, or from solid highs down near or below the high threshold of a subsequent device. Degradations take the form of slowed propagation delays, abnormally slow or distorted output edges, or lost data in devices containing memory. Any and all of these unwanted side effects will cause a system to perform unpredictably and unreliably. Output disturbances especially can be the cause of a multitude of system performance abnormalities.

Since ACL is considered to be a high-performance family of circuits, SSE is necessary in order to insure that the circuits will perform as specified under any switching condition. To guarantee that ACL will perform satisfactorily under multiple output switching conditions, comprehensive SSE is performed prior to product release. Tests are done to evaluate the magnitude of output disturbances, the integrity of stored data, and the propagation delays and output transition times under conditions of multiple outputs switching.

Each of these evaluations will now be explained and a very general procedure for measuring each will be given. For a specific step-by-step procedure for measuring each, including fixturing and equipment requirements, refer to Appendix 1.

Output Disturbance Tests

The purpose of these tests is to determine the magnitude of disturbances on the High and Low level of the outputs when multiple outputs are switching. The terms V_{OHV} and V_{OLP} are used to describe the level of these disturbances. V_{OHV} refers to the minimum 'valley' High level output voltage and V_{OLP} refers to the maximum 'peak' Low level output voltage. Figure 1 shows a typical example of what the output disturbances look like and also defines the points where V_{OLP} and V_{OHV} are measured.

For circuits with a single output or a single complementary output, the circuit is setup so that the pin under test is switching and the disturbance levels are then measured at the points on the waveform as shown in Figure 1. For all other circuits, the circuit is set up so that the pin under test is not switching while the other outputs are

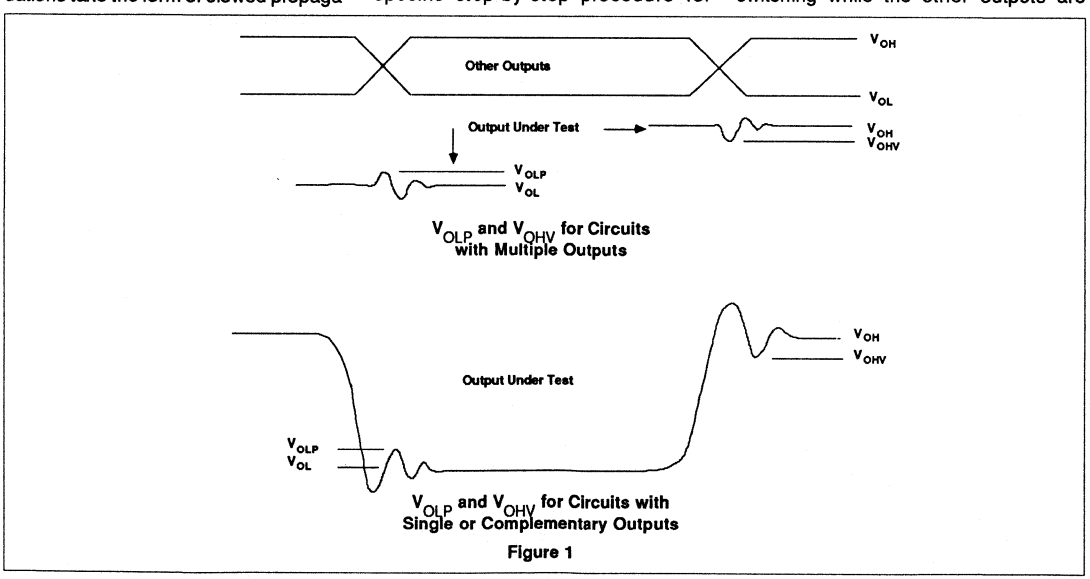


Figure 1

switching and the disturbance levels are then measured as shown in Figure 1.

3.2 Output High Disturbance

- For circuits with a single output or a single complimentary output, set the input conditions so the output(s) under test is switching. For all other circuits, set the input conditions so the output under test is high with as many other outputs as possible switching.
- Examine the waveform and record the level of V_{OHV} with respect to V_{CC} as defined by Figure 1.

3.3 Output Low Disturbance

- For circuits with a single output or a single complementary output, set the input conditions so the output under test is switching. For all other circuits, set the input conditions so the output under test is Low with as many other outputs as possible switching.
- Examine the waveform and record the level of V_{OLP} with respect to Ground as defined by Figure 1.

Stored Data Integrity

The purpose of this test is to determine what effect, if any, switching multiple outputs simultaneously has on integrity of data storage for circuits with internal storage elements. This test is necessary to insure that the contents of internal storage elements are never corrupted by voltage transients which appear not only on outputs, but also on internal chip supply lines. To perform this test:

- Store a logic 1 in an internal storage element.
- Switch all remaining outputs or, if possible, all outputs.
- Discontinue switching and set input conditions so that the contents of the internal storage elements can be observed.
- Verify that the internal storage element has not changed state.
- Store a logic 0 in an internal storage element and repeat the previous three steps.

Simultaneous Switching Influence on AC Parameters

The purpose of these tests is to determine what effect switching multiple outputs simultaneously has on the propagation delays and output transition times of a circuit. This test is necessary to insure that the propagation delays and output transition times are not significantly degraded by switching multiple outputs simultaneously. To perform these tests:

- Set the input conditions so that the output under test will be switching in the manner required for measurement of the desired propagation delay or output transit on time.
- Switch as many other outputs as possible.
- Measure the propagation delay or output transition time on the output under test using any accurate method.

Summary

The user of ACL circuits should be aware of any potential disturbances or performance degradations that can occur under conditions of multiple output switching and should understand the terms used to describe and measure these. This paper is an attempt to standardize a procedure to which all ACL circuits should be subjected. This method, when followed, will give a user a clear indication of actual device performance.

Simultaneous Switching Evaluation of Advanced CMOS Logic

AN601

Appendix 1 -
A Step-by-Step Procedure for Evaluating SSE in the Laboratory

1.0 PURPOSE AND SCOPE OF DOCUMENT

1.1 This document gives the steps and procedures needed for completing SSE for ACL devices. Testing is done to determine the effects that switching more than one output simultaneously has on output disturbances, stored data integrity, propagation delays, and output transition times.

2.0 EQUIPMENT REQUIREMENTS

2.1 Hardware

Device	Options
Bench Controller	HP9836C or equivalent
Programmable Oscilloscope	TEK7854 or equivalent
Programmable Pulse Generator	HP8161A or EH2000
Temperature Controller	TP412 or equivalent
Power Supply Programmer	ICS4871 or equivalent
Test Fixture	Acceptable high frequency PC board fixture
Plotter	HP7475A or equivalent
Printer	HP2673A or equivalent
Dice System (An optional data generator/analyzer)	HP8180A, HP8182A, and HP15414A

3.0 GENERAL

3.1.1 When applicable, plots should be taken on at least one part and data values should be taken on three parts. The one part used for plots should have typical characteristics for the sample as a whole.

3.1.2 The test fixture will be the same one used for standard AC testing. This is a high-frequency PC board fixture featuring adequate grounding and V_{CC} decoupling as well as 50Ω micro strip line for all signal paths and close proximity loading. The test fixture should have V_{CC} decoupling of at least 100µF, 0.1µF, 0.01µF, and 100pF. For a complete discussion of fixturing requirements including grounding, bypassing, and general high-frequency testing requirements refer to the Application Note entitled "Testing and Specifying ACL Logic."

3.1.3 Pulse Generator Setup

For 74AC11XXX $V_{IH} = (.8\ V_{CC})$, $V_{IL} = (.2\ V_{CC})$
For 74ACT11XXX $V_{IH} = 2.5V$, $V_{IL} = 0.5V$
t_R/t_F = 3.0ns (10 to 90%)
f = 5MHz
Duty Cycle = 50%

The input signal should be terminated with 50Ω and then branched out equally to all inputs needing the input signal. ("Simultaneous" is defined as the input pins Simultaneous Logic of the device seeing a given signal at the same moment in time). Line lengths from the termination to the device pin should be kept as short as possible. The dice system can be used if more flexibility of input programming is necessary. If the dice system is used, interchannel delay between the various channels must be nulled out at the pins of the device. If a gang type configuration is used to tie the input signal to more than one input, input edge rates should be as close as possible to the 3.0ns times.

3.1.4 All outputs should be loaded with the standard 50pF, 500Ω AC load.

3.1.5 The output to be evaluated should be the one farthest away from the V_{CC} pins. If there are two equidistant outputs, record data on both outputs and plot only the worst-case output. Also, if more than one mode/path exists, all should be checked, but only the worst case tested.

3.2 Output High Disturbance - Measure the V_{OHV} level on an output held High during simultaneous switching.

3.2.1 V_{CC} = -5.5V, Temp. = 55°C and V_{CC} =5.0V, Temp. = 25°C

3.2.2 Number of devices = 3. Plots should be taken on one part.

3.2.3 Input conditions should be set so that the output under test is High.

3.2.4 Switch the remaining outputs simultaneously from Low to High and record V_{OHV}.

3.2.5 Plot waveforms of a switching input, the High output, and a switching output.

3.2.6 Repeat steps 3.2.4 through 3.2.5 for the following other transitions:

High to Low
3-State to Low (if possible)
Low to 3-State "
High to 3-State "
3-State to High "

3.3 Output Low Disturbance Testing - Measure the V_{OLP} level on an output held Low during simultaneous switching.

3.3.1 V_{CC} = 5.5V, Temp. = -55°C and V_{CC} = 5.0V, Temp. = 25°C

3.3.2 Number of devices = 3. Plots should be taken on one part.

3.3.3 Input conditions should be set so that the output under test is Low.

3.3.4 Switch the remaining outputs simultaneously from High to Low and record V_{OLP}.

3.3.5 Plot waveforms of a switching input, the Low output, and a switching output.

3.3.6 Repeat steps 3.3.4 through 3.3.5 for the following other transitions:

Low to High	
3-State to Low	(if possible)
Low to 3-State	"
High to 3-State	"
3-State to High	"

3.4 **Stored Data Integrity** - For devices with internal storage elements, perform tests to insure that internal storage elements are not corrupted by simultaneous switching of outputs.

3.4.1 V_{CC} = 5.5V, Temp. = -55°C and V_{CC} = 5.0V, Temp. = 25°C

3.4.2 Number of devices = 3.

3.4.3 Store data (both High and Low) in an internal storage element. This can be the same element of the output tested in 3.2 and 3.3.

3.4.4 Switch the remaining outputs simultaneously as was done in 3.2. and 3.3 (including 3-States if possible). Check to see that data is not corrupted with any of the switching.

3.4.5 When possible, the dice system should be utilized to functionally check out various combinations of switching with respect to the above procedures.

3.5 **Input Waveform Phase Effects** - Check phase effects and measure the delay offset that causes the largest magnitude of output disturbances (when possible).

3.5.1 V_{CC} = 5.5V

3.5.2 Temp. = 25°C and -55°C

3.5.3 Number of devices = 3. Plots should be taken on one part.

3.5.4 Testing is completed by switching half of the outputs 180° out-of-phase from the other half of the outputs.

3.5.5 Adjust the delay on half of the outputs (with respect to the other half) until the worst-case output disturbance is obtained.

3.5.6 Record the edge offset and disturbance magnitudes for three parts.

3.5.7 Plot waveforms (one part) of a switching input from one half and another from the other half with outputs from both halves.

3.5.8 Repeat steps 3.5.5 through 3.5.7 for in-phase effects as well.

4.0 Tpd vs. Simultaneous Switching

- Measure propagation delays and output transition times under conditions of multiple outputs switching.

4.1.1 Number of devices = 3

4.1.2 V_{CC} = 5.0V, Temp. = 25°C

4.1.3 Number of outputs tested = 1

4.1.4 Number of outputs switching = 1 to N (when possible)

4.1.5 The test output should be tested for all possible propagation delays (t_{PLH}, t_{PHL}, t_{PZL}, t_{PLZ}, t_{PLH}, and t_{PHZ}) and also transition times (t_{TLH} and t_{THL}) for all conditions of outputs simultaneously switching (1 to n).

4.1.6 All tests should be made with other outputs switching in phase and then out of phase.

AN602
Printed Circuit Board Test Fixtures for High-Speed Logic

Application Note

INTRODUCTION

The Signetics Standard Products Group (SPG) operates a Characterization Laboratory in Orem, Utah. This Lab maintains the capability of testing the 11 logic product families the Division supports. These include: AuTTL–74XXX, Schottky-74SXXX, Low-Power Schottky-74LSXXX, FAST–74FXXX, ALS-74ALSXXX, High-Speed CMOS-74HCXXX, High-Speed CMOS/TTL-74HCTXXX, Advanced CMOS/TTL (ACL)-74ACT11XXX, Advanced CMOS (ACL)-74AC11XXX, and both 10K and 100K ECL.

In the past Signetics SPG Characterization has designed and built a series of bench test AC fixtures that provide the ability to have one fixture that addresses many product types across families. It allowed the use of a smaller fixture inventory to perform well over the majority of the devices. With the advent of the 74AC11xxx series, 1 micron CMOS logic family, the existing fixtures were no longer adequate. The largest problem with the older fixtures is the method of bypassing switching noise from V_{CC} to GND. They use bus bars running down the top and bottom sides of the PC board from the end of the device to the point of connection to the DUT V_{CC}/GND pins. Connection was then made using a copper braid to the DUT pin. While adequate for earlier logic families there is too much inductance in the power supply path to allow switching the faster transitions and higher currents of the ACL family without causing severe aberrations in output waveforms. This family of devices is also the first "TTL" type to specify operation over the entire V_{CC}/GND extremes in a simultaneous switching condition.

THEORY OF OPERATION

There are several key points in testing the ACL logic family. They are:

- Low inductance/high frequency power supply by-passing.
- Large ground and V_{CC} planes (covering virtually the entire board area).
- 50Ω signal lines for uniform impedance, high bandwidth and easy interface to test gear.
- Output AC load capacitance close to the DUT.
- Measurement point close to the DUT.

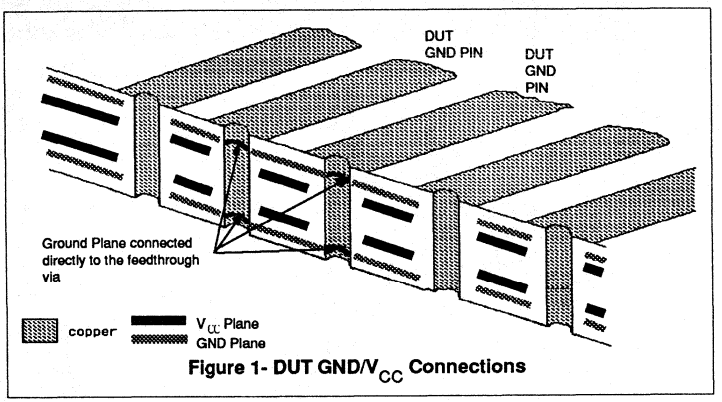


Figure 1- DUT GND/V_{CC} Connections

POWER SUPPLY AND GROUND

The largest difference between these fixtures and the earlier series is the inclusion of dedicated GND and other power supply planes internal to the PC board. The GND layers are used for impedance control of the signal traces and internal to the GND planes are V_{CC} and other power supply planes. In order to provide the lowest possible impedance in the power and GND connections the planes are connected directly to the DUT power/GND pad vias (See Figure #1). This feature reduces the V_{CC}/GND path inductances to a minimum and provides the highest possible frequency response under simultaneous switching conditions. This series of boards has a ring frequency of approximately500 MHz between the power supply pins. This ensures that the output waveforms seen on the test equipment are due to the device and package, not the fixture. The trade-off for these features is that the boards must be purchased for a particular V_{CC}/GND pin combination. Signetics has designated an extension to the DUT board PC board numbers to allow calling out the separate internal layers needed for the various GND/power supply combinations. See Appendix I for the GND/V_{CC} combinations.

DEVICE SOCKETS

These boards do not use a DUT socket. All surface mount packages in this series of PC boards use a conductive polymer from Shin-Etsu for signal transmission (See Figure #3). This polymer, type MAF, only conducts in the vertical direction and provides a low impedance path to connect between the DUT leads and the PC board pad. DIP pattern boards use Augat sockets soldered flush with the PC board surface. This effectively eliminates any inductance due to a socket. The trade-off is decreased insertions on the surface mount boards. In order to align an SMT device to the required DUT pads alignment blocks and alignment guides are required (See Appendix I for dimensions). They are machined from a phenolic material for over temperature operation and electrical isolation. The block is designed to align the DUT to the pads, allow circulation for a temperature stream and on gull-wing devices, to provide mechanical

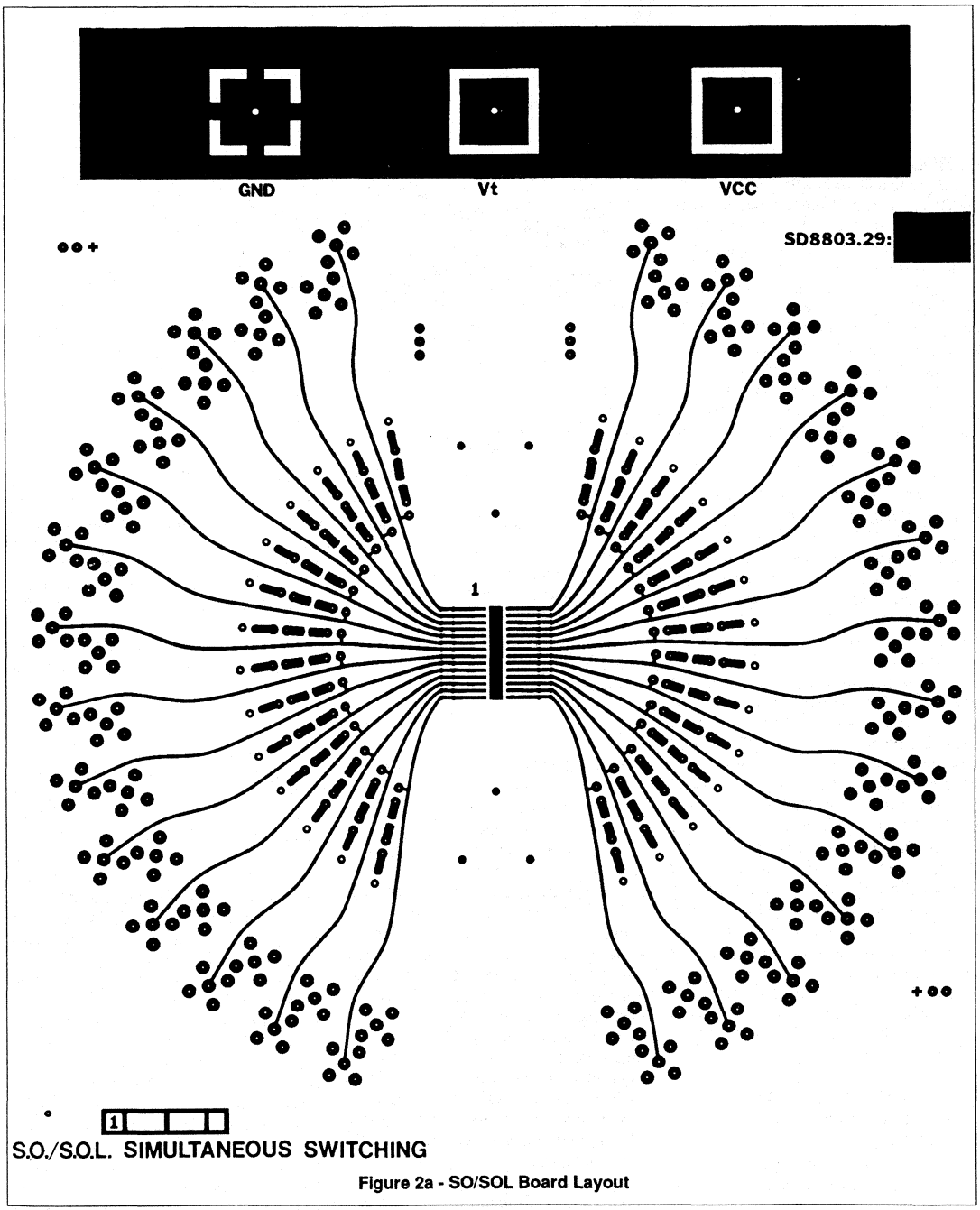


Figure 2a - SO/SOL Board Layout

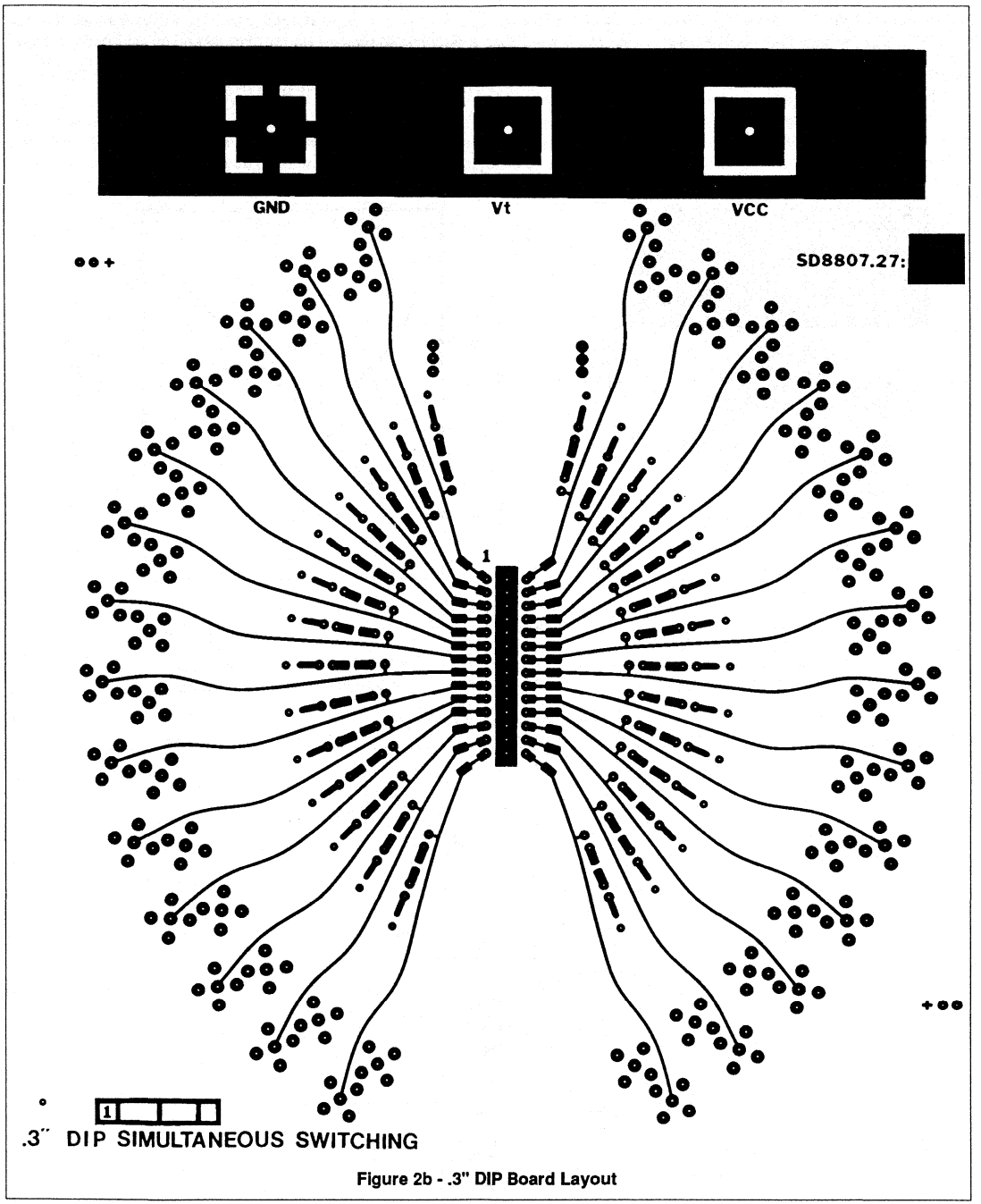


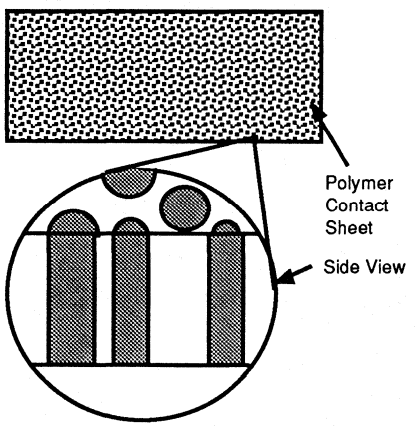
Figure 2b - .3" DIP Board Layout

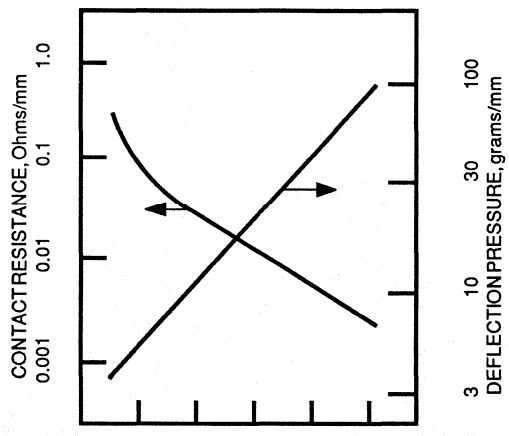
pressure to the leads to ensure contact with the conductive polymer. The top hole in the block also doubles as the vacuum wand access to change devices. The boards are also designed to use the alignment guides to provide a mechanical clamp and hold the polymer in place and allow easy replacement. See Figure #4.

SIGNAL LINES

All signal lines have a 50Ω impedance, determined by the microstrip layout method. The 50Ω value was selected to allow easy termination for input signal generators and a 10:1 divider for outputs. The inputs are also terminated into a 10:1 divider, 50Ω terminator. This allows the boards to be built with very small stubs for signal integrity and all oscilloscope channels can be set up to the same vertical amplification.

On the top of the PC board is a trace running straight from the SMB connector to the DUT pad. The only connection to





MAF 0.4 mm thick

Current carrying capacity amps/mm:	5.0
Number of conductors/mm:	7.3
Contact resistance milli-Ohms/mm:	4.8
Minimum contact area, mm:	0.287

Sample connector: 0.4mm thick
Electrode: 1.2mm (gold plated)

Figure 3 - Shin-Etsu Polymer

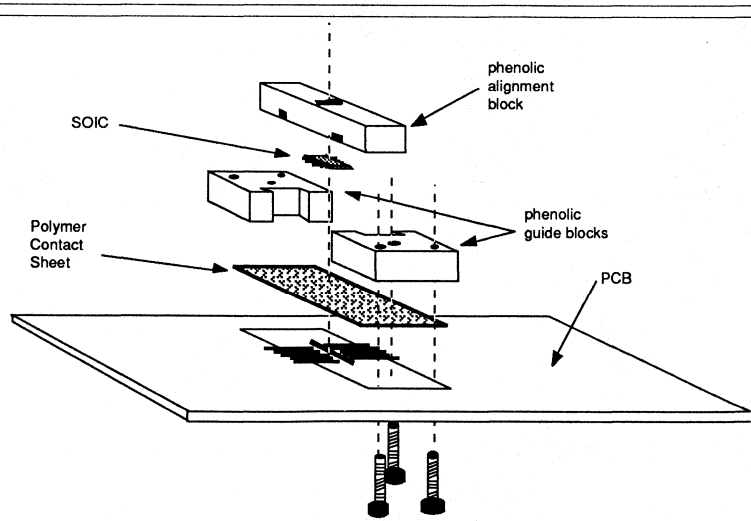


Figure #4. Illustrated Parts Breakout of SO Device Assembly

this line is a jumper allowing connection of a pull-up resistor for TTL 3-S or open-collector outputs. On the bottom of the PC board the trace has a break in it to allow mounting a 453Ω resistor (R1) for the 10:1 divider network. Since the worst case load in simultaneous switching conditions is to mount a lumped capacitance directly on the DUT pin, a direct connection to the internal GND plane is in the center of the DUT pads to allow soldering on load capacitors. For input pins it is also used for mounting termination resistors directly beneath the device. Therefor the PC boards must be assembled for a particular I/O pin combination.

If a DUT pin is an input the board is configured in a loop through mode. The outer circle of SMB connectors is con-

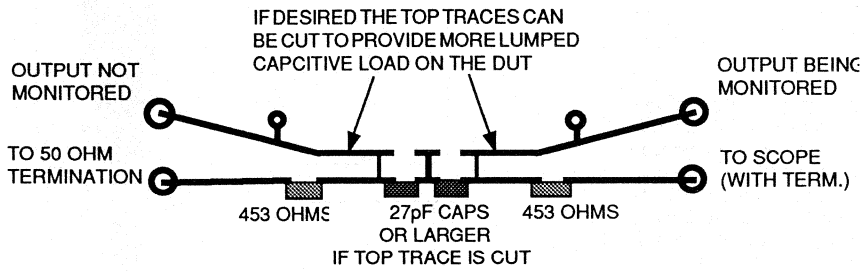


Figure 5a - SSE PC Board Input Schematics

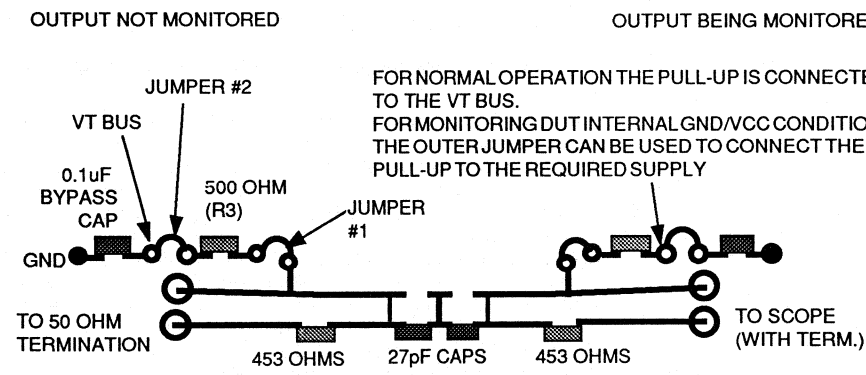


Figure 5b - SSE PC Board 2-S Output Schematics

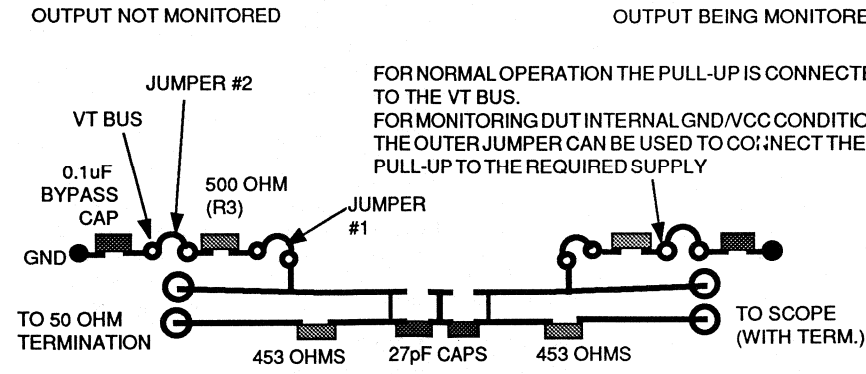


Figure 5c - SSE PC Board 3-S/O.C. Output Schematics

nected to the signal source. On the bottom side of the PC board a 56.2Ω (R2) resistor is soldered between the DUT pad and the GND. Across the break in the bottom trace a 453Ω resistor is soldered. In combination with a 50Ω o-scope termination or a 50Ω SMB terminator the 450 + 50Ω in parallel with the 56.2Ω provides the proper 50Ω termination for signals and a monitoring capability (See Figure 5a).

For an output pin the outer ring of SMB's is not used. The same 453Ω/50Ω pair is used as a 10:1 divider into the o-scope and still provide the specified 500Ω pull-down resistor. A chip capacitor of sufficient capacitance to bring the total to 50pF is soldered between the bottom DUT pad and the GND (See Figure 5b). For 3-S or open collector devices the 500Ω pull-up resistor (R3) on the top trace is jumpered in with a .1" jumper (#1). The outside of the pull-up resistor also has a .1" jumper (#2) to allow connection to the internal V_T bus or some other termination voltage as needed for any particular test (See Figure 5c).

The bottom trace SMB connector is always connected either to an SMB 50Ω terminator or the 50Ω terminated input of the scope to complete the load. See Figure 6 for a 50Ω terminator example.

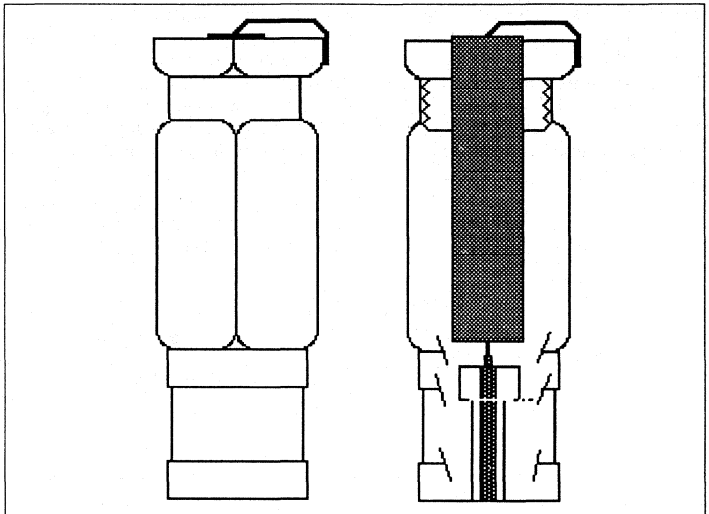


Figure 6 - Resistive Load Used on Non-monitored SMB Connectors

INPUT STIMULUS AND MEASUREMENT

As stated previously, the measurements are made with 50Ω sampling systems. The connections to these systems are made via SMB connectors. This was chosen since it is a standard connector, available from several sources, uses push-on operation, is small for easy configuration and is capable of high bandwidth operation. Figure 8 shows where the connections are made and also where the pulse generators connect to the input, also an SMB connector. Since the 450Ω resistor, R1, is soldered directly to the pin of the device, see Figure 6, the actual probe tip is at that point. This has the advantage of eliminating any distance from the device to the probe tip, thus guaranteeing accurate results.

INSERTING DEVICES

To hold surface mount devices in place the alignment block is clipped down to the PC board with brass clips mounted to the alignment guides. This provided the simplest solution to several conflicting demands. The device had to have good contact with the Shin-Etsu polymer to function. There needed to be some method of allowing a temperature stream flow around the device, and the devices needed to be changed. For SO devices the edges of the package cutout provide enough pressure to the top of the DUT leads to make good contact with the polymer, for PLCC the top of the cutout provides the same function. The hole through the middle of the alignment block allows a vacuum wand to be inserted and hold the device and block together until they are clipped to the PC board. Several models of wands are available from H-Square Company for handling devices, including one with a built in static dissipation resistor and lead for ESD protection. They also have designed a custom tip to mate with the top hole of the alignment blocks and prevent the block from bouncing up the wand tube prior to clipping it to the PC board. Cutouts around the device allow exit for the temperature stream.

VERSATILITY AND COST

At some point, there is a choice between the most technically attractive options and the cost of such options. This fixture has been designed to optimize its technical effectiveness. This was dictated by the test requirements of the ACL logic family, specifically the simultaneous switch specifications. It is also suitable for testing FAST, ALS and ECL product devices if the existing series of boards do not provide the needed environment to get accurate, repeatable results.

For the user the only connections being made to the fixture are:

- V_{CC} (banana jack) This is the positive DUT voltage supply.
- GND (banana jack) This is the common ground of all input supplies.
- V_T supply (banana jack) This is the 3-state/O.C. pull-up voltage and is jumpered to each pin as needed.
- V_{GND} supply (banana jack) This is the DUT GND layer used for ECL which requires a +2V offset for proper termination on the output pins when using oscilloscope input termination.

- V_{EE} supply (banana jack) This is the negative DUT power supply layer used for ECL devices
- Input Stimulus (outside SMB connectors) This is found on every input/output pin. More than one pin may be used in this manner.
- Output Measurement or Scope Connection (inside SMB connectors). More than one pin may be used in this manner. *Remember*, if this pin is not connected to a scope, a 50Ω resistor must be connected here to ground to complete the 500Ω resistive load or input termination network. Signetics has constructed their own 50Ω load by soldering a high quality (high frequency) 50Ω resistor inside a female SMB cable connector. See Figure 6.

With these seven connection types, the fixture is capable of testing the product lines mentioned.

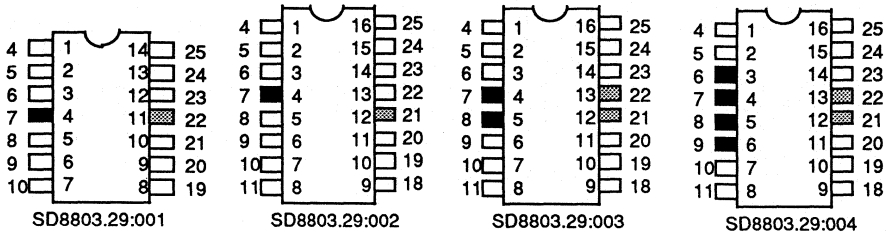
Included in Appendix I are the internal GND/V_{CC} connections of the existing defined layers.

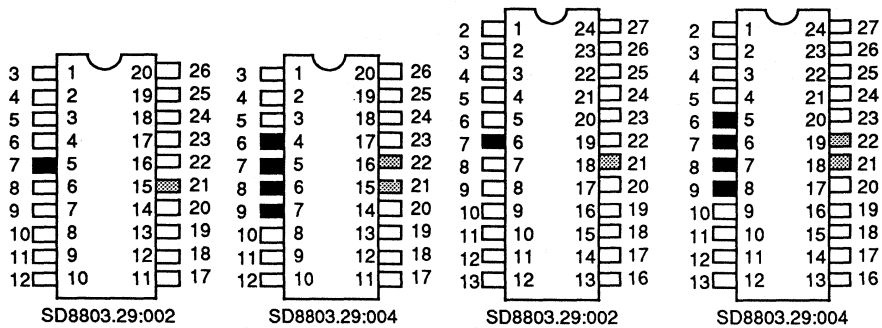
In Appendix II are the dimensions of the alignment blocks and guides for the SMT packages.

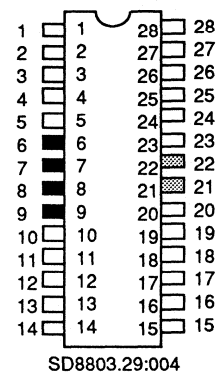
In Appendix III is the parts list for these fixtures and the supplies used by Signetics.

This in no way constitutes Signetics endorsements of these suppliers and the customer may select their own supplier if they so desire. This fixture is offered to the public to duplicate and use within their own environments. Signetics will not provide any materials but will allow the manufacturers of the board and materials to build and/or supply for any requesting party. Pricing and availability are left to the vendors and Signetics has no control over those issues. The intent is to provide something for users of ACL, and other advanced logic family devices, that has been proven and tested in use, namely the characterization of these products prior to the introduction to the market place.

Appendix I - Internal GND/V_{CC} Connections



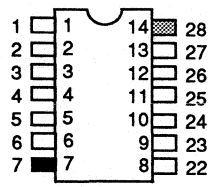




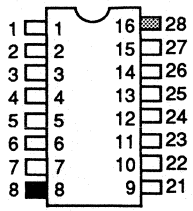
VCC ▩
GND ■

(On each package outline the outer numbers refer to the PCB footprint and the inner numbers refer to the DUT pins.)

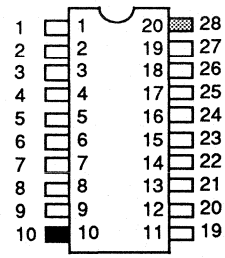
For .3" DIP boards, substitute SD8807.27:nnn for SD8803.29:nnn



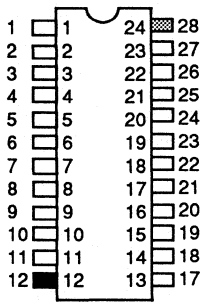
SD8803.29:005



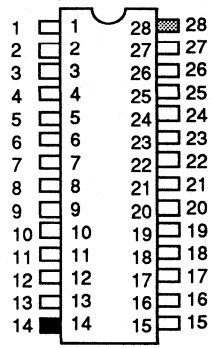
SD8803.29:006



SD8803.29:007



SD8803.29:008



SD8803.29:009

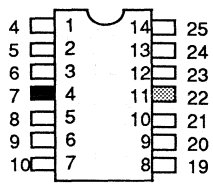
VCC GND

NOTE: The PC board/package configurations shown above require the use of the SO alignment blocks with offset package cutouts.

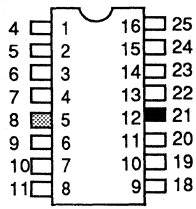
Defined layers and their connections for SO (SD8803.29:nnn) and .3" DIP (SD8807.27:nnn) boards are:

GROUND LAYER (2.x)	
2.1 =	7
2.2 =	7, 8
2.3 =	10
2.4 =	6, 7, 8, 9
2.5 =	21, 22
2.6 =	21
2.7 =	8
2.8 =	12
2.9 =	14
2.A =	4, 8, 11, 18, 22, 25

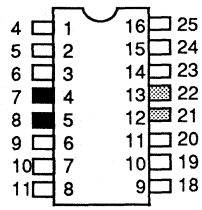
V_{CC} LAYER (3.y)	
3.1 =	22
3.2 =	21, 22
3.3 =	28
3.4 =	21
3.5 =	8
3.6 =	7
3.7 =	1



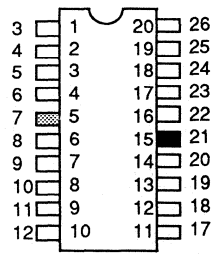
SD8803.29:001
(74F779)



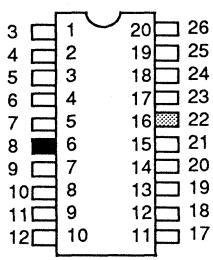
SD8803.29:010
(74F83)



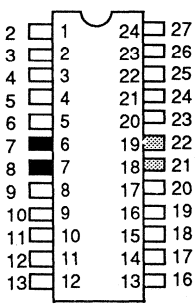
SD8803.29:003
(74F3037,38,40)



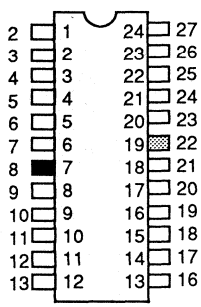
SD8803.29:011
(74F1804,1805
74F1808,1832)



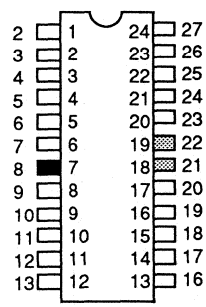
SD8803.29:012
(74F579)



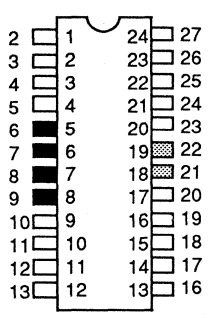
SD8803.29:003
(74F723,725)



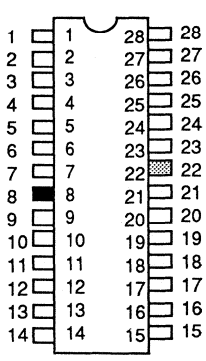
SD8803.29:012
(74F269)



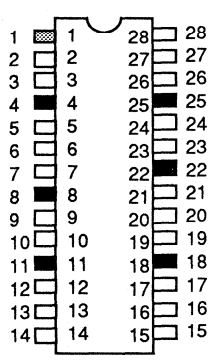
SD8803.29:013
(74F455,456
74F657)



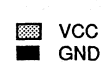
SD8803.29:004
(74F30240,30244,
74F30245,30640)



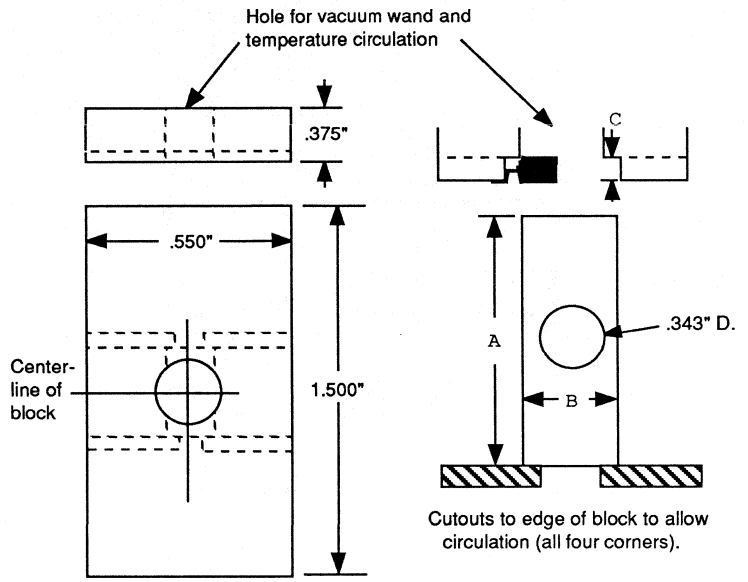
SD8803.29:012
(74F550,551,552)



SD8803.29:014
(74F776
74F8960
74F8961)



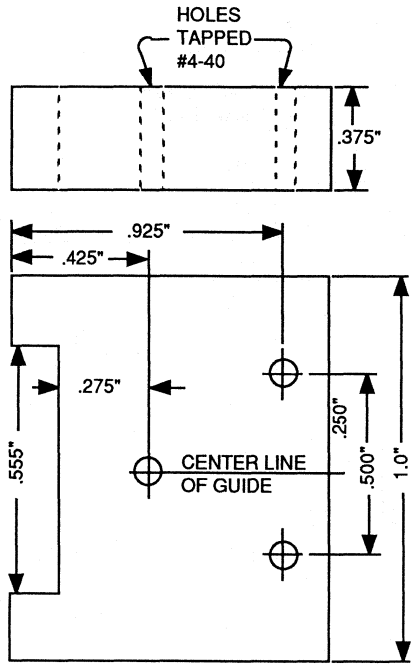
APPENDIX II - SMT Alignment Blocks and Guides



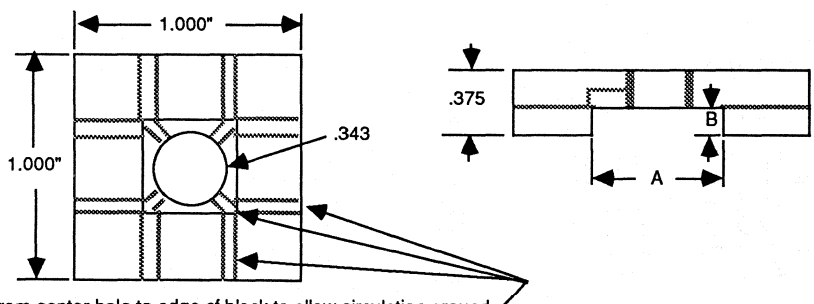
Material phenolic or other insulator able to withstand 155 degrees C.

DIMENSIONS FOR VARIOUS PACKAGES

PACKAGE		A	B	C	OFFSET FROM CENTERLINE
JEDEC	14 PIN .150"	.346 +-.001	.205	.055+-.001	.025
JEDEC	14 PIN .150"	.346 +-.001	.205	.055+-.001	.175
EIAJ II	14 PIN .210"	.405 +-.001	.265	.075+-.001	.025
EIAJ II	14 PIN .210"	.405 +-.001	.265	.075+-.001	.175
JEDEC	16 PIN .150"	.400 +-.001	.200	.050+-.001	.000
JEDEC	16 PIN .150"	.400 +-.001	.200	.050+-.001	.150
EIAJ II	16 PIN .210"	.405 +-.001	.265	.070+-.001	.000
EIAJ II	16 PIN .210"	.405 +-.001	.265	.070+-.001	.150
JEDEC	16 PIN .300"	.406 +-.001	.360	.090+-.003	.000
JEDEC	16 PIN .300"	.406 +-.001	.360	.090+-.003	.150
EIAJ II	20 PIN .210"	.505 +-.001	.265	.075+-.001	.000
EIAJ II	20 PIN .210"	.505 +-.001	.265	.075+-.001	.100
JEDEC	20 PIN .300"	.510 +-.001	.365	.095+-.003	.000
JEDEC	20 PIN .300"	.510 +-.001	.365	.095+-.003	.100
JEDEC	24 PIN .300"	.605 +-.001	.365	.095+-.003	.000
JEDEC	24 PIN .300"	.605 +-.001	.365	.095+-.003	.050
JEDEC	28 PIN .300"	.710 +-.001	.365	.090+-.003	.000



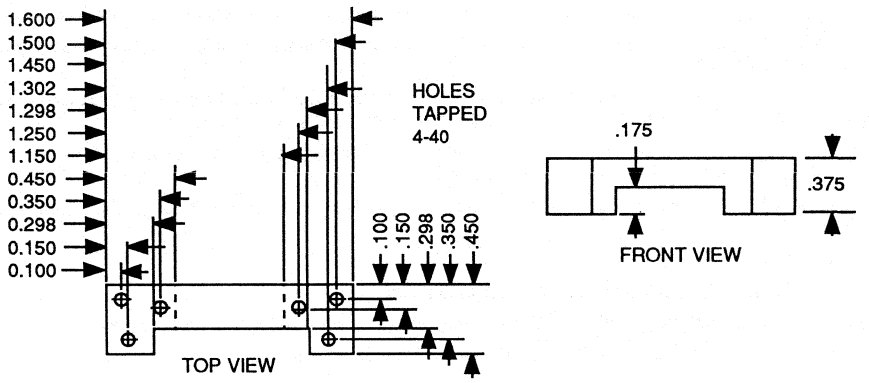
SO Alignment Guides



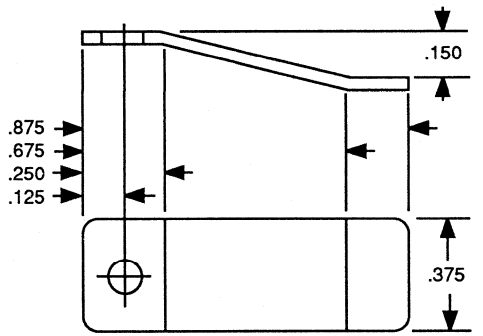
Cutouts from center hole to edge of block to allow circulation around device when forcing temperature (all four corners).

PACKAGE TYPE	A	B
20 PIN PLCC	.390"	.160"
20 PIN LCC	.350"	.060"
28 PIN PLCC	.494"	.160"
28 PIN LCC	.450"	.060"

Figure 12 - PLCC/LCC Alignment Block and Package Cutout Dimensions



PLCC/LCC Alignment Guide



Hole .116 +- .003" diameter.
.020" Brass shim stock
Edges deburred
Corners radiused .050"

All other dimensions +- .025"

Alignment Block Retainer Clip

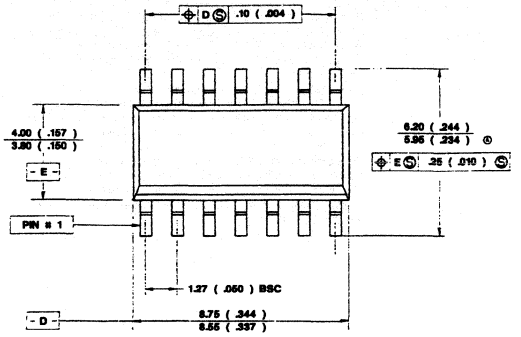
Construction Hints:
A suggested order of assembly is as follows:

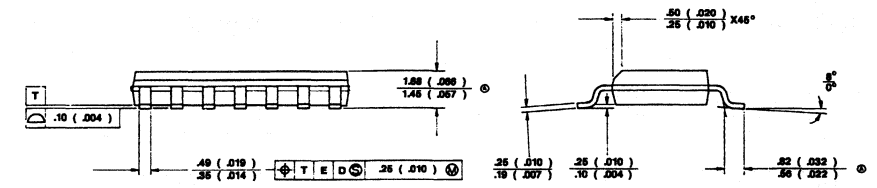
1. Install SMB Connectors. Elevate base from board .05" (this can be done with a shim or the posts can be soldered flush with the bottom side of the PC board).
2. Install Augat pin-sockets (3-S or DIP boards only, use a device inserted into the sockets on the DIP boards to hold them steady or tape over the open end of the socket with masking tape and remove after soldering).
3. Install 453 Ohm load/termination resistors (for surface mount components apply a drop of solder to one pad then reflow and mount the component, then solder the other side to its pad).
4. Install the 56.2 Ohm load/termination resistors and load caps (solder the ends on the individual lines and then the common GND connections).
5. Install banana jacks.
6. Connect V_{CC}, GND, and V_T supplies from banana jacks to board.
7. Attach alignment blocks and guides with 4-40 Phillips pan head machine screws (SMT boards only).
8. Remove all remaining flux. Keep "flux-off" or other solvent from banana jacks.

Section 7
Packaging Information

Packaging Information

14–PIN PLASTIC SMALL OUTLINE (SO)



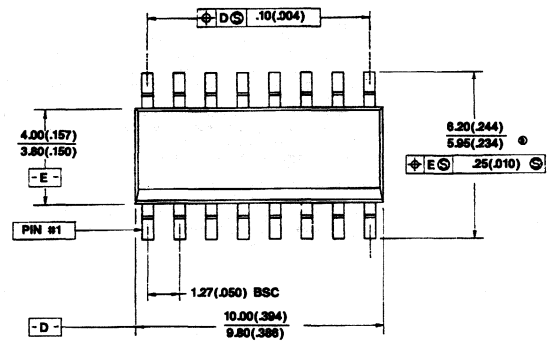


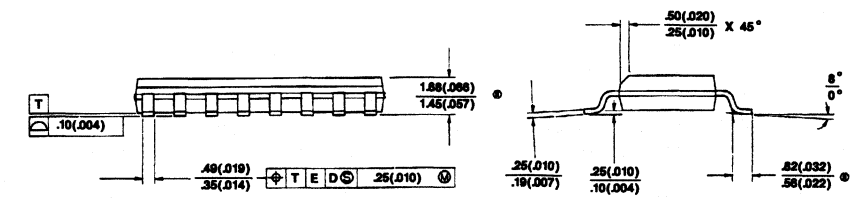
DH1 853-0175 91504

PO02270S

NOTES:
1. Package dimensions conform to JEDEC specification MS-012-AB for standard small outline (SO) package, 14 leads, 3.75mm (.150") body width (issue A, June 1985).
2. Controlling dimensions are in mm. Inch dimensions in parentheses.
3. Dimensioning and tolerancing per ANSI Y14.5M- 1982.
4. "T", "D" and "E" are reference datums on the molded body and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .15mm (.006") on any side.
5. Pin numbers start with pin #1 and continue counterclockwise to pin #14 when viewed from top.
6. Signetics ordering code for a product packaged in a plastic small outline (SO) package is the suffix D after the product number.

16–PIN PLASTIC SMALL OUTLINE (SO)





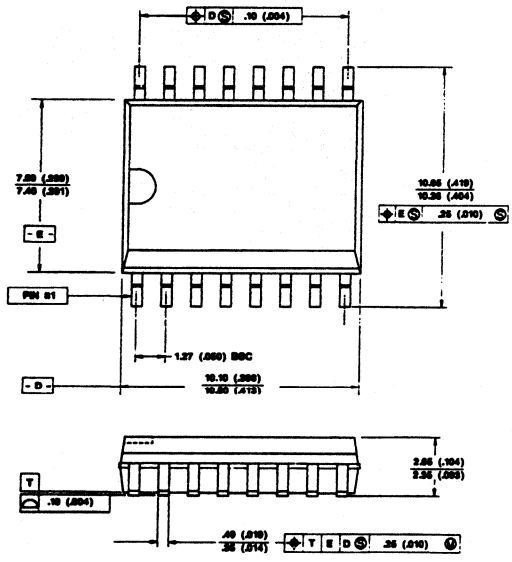
DJ1 853-0005 91504

PO01830S

NOTES:
1. Package dimensions conform to JEDEC specification MS-012-AC for standard small outline (SO) package, 16 leads, 3.75mm (.150") body width (issue A, June 1985).
2. Controlling dimensions are mm. Inch dimensions in parentheses.
3. Dimensioning and tolerancing per ANSI Y14.5M-1982.
4. "T", "D" and "E" are reference Datums on the molded body and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .15 mm (.006") on any side.
5. Pin numbers start with pin #1 and continue counterclockwise to pin #16 when viewed from top.
6. Signetics ordering code for a product packaged in a plastic small outline (SO) package is the suffix "D" after the product number.

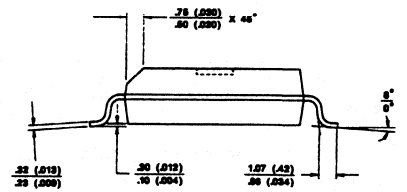
Packaging Information

16–PIN PLASTIC SMALL OUTLINE (SOL)



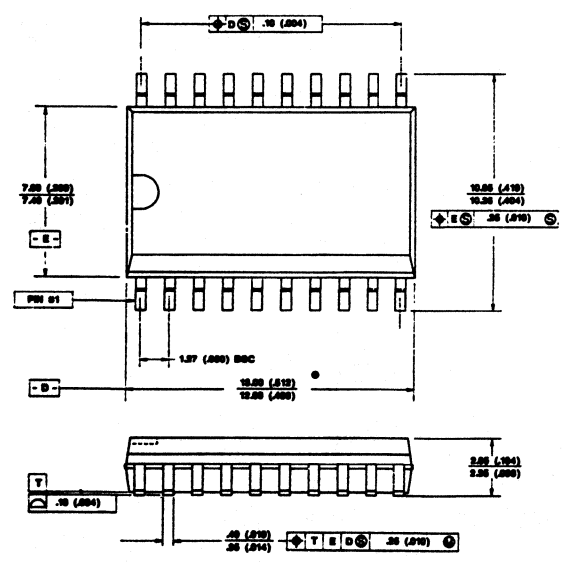
DJ2 853-0171 81218

NOTES:
1. Package dimensions conform to JEDEC specification MS-013-AA for standard small outline (SO) package, 16 leads, 7.50mm (.300") body width (issue A, June 1985).
2. Controlling dimensions are in mm. Inch dimensions in parentheses.
3. Dimensioning and tolerancing per ANSI Y14.5M- 1982.
4. "T", "D" and "E" are reference datums on the molded body and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .15mm (.006") on any side.
5. Pin numbers start with pin #1 and continue counterclockwise to pin #16 when viewed from top.
6. Signetics ordering code for a product packaged in a plastic small outline (SO) package is the suffix D after the product number.



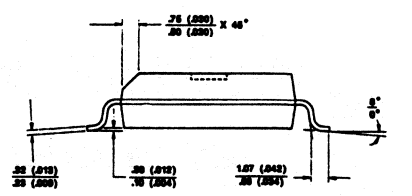
PO02290S

20–PIN PLASTIC SMALL OUTLINE (SOL)



DL2 853-0172 82948

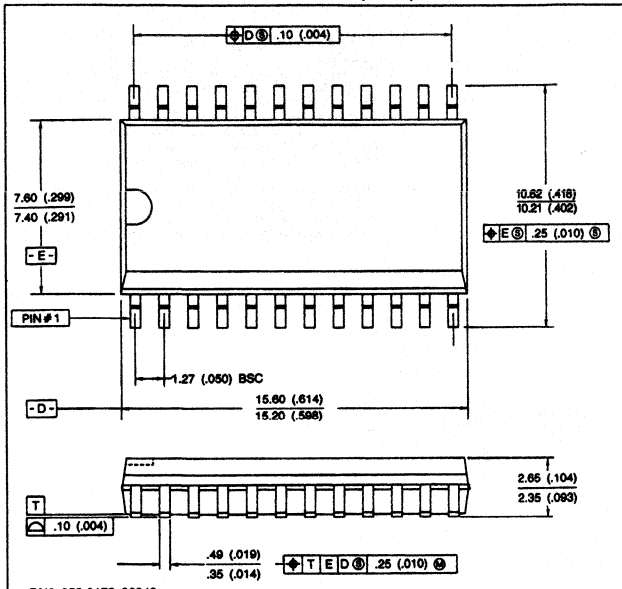
NOTES:
1. Package dimensions conform to JEDEC specification MS-013-AC for standard small outline (SO) package, 20 leads, 7.50mm (.300") body width (issue A, June 1985).
2. Controlling dimensions are in mm. Inch dimensions in parentheses.
3. Dimensioning and tolerancing per ANSI Y14.5M- 1982.
4. "T", "D" and "E" are reference datums on the molded body and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .15mm (.006") on any side.
5. Pin numbers start with pin #1 and continue counterclockwise to pin #20 when viewed from top.
6. Signetics ordering code for a product packaged in a plastic small outline (SO) package is the suffix D after the product number.

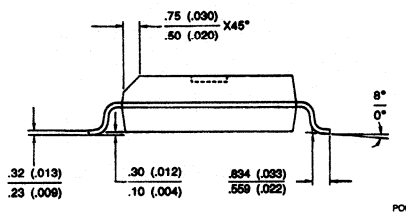


PO02360S

Packaging Information

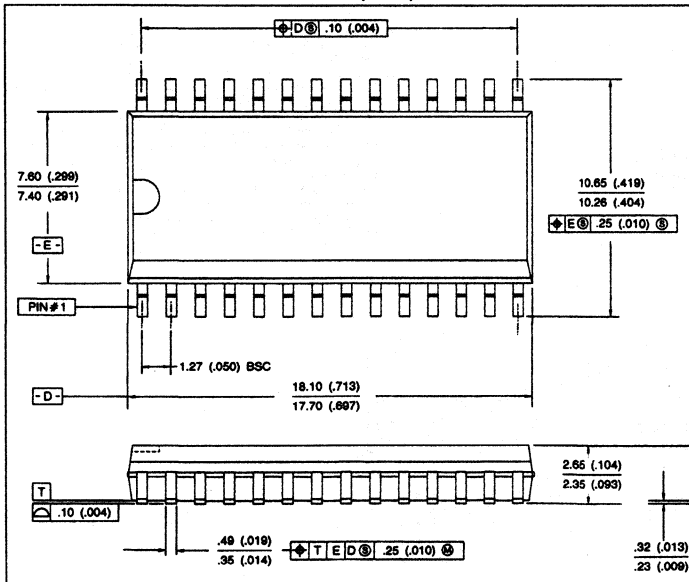
24–PIN PLASTIC SMALL OUTLINE (SOL)

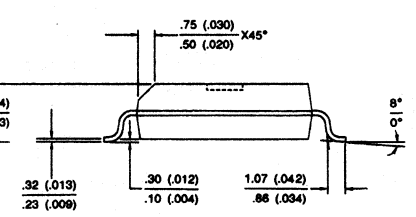




NOTES:
1. Package dimensions conform to JEDEC specification MS-013-AD for standard small outline (SO) package, 24 leads, 7.50mm (.300") body width (Issue A, June 1985).
2. Controlling dimensions are in mm. Inch dimensions in parentheses.
3. Dimensions and tolerancing per ANSI Y14.5M- 1982.
4. "T", "D" and "E" are reference datums on the molded body and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .15mm (.006") on any side.
5. Pin numbers start with pin #1 and continue counterclockwise to pin #24 when viewed from top.
6. Signetics ordering code for a product packaged in a plastic small outline (SO) package is the suffix D after the product number.

28–PIN PLASTIC SMALL OUTLINE (SOL)

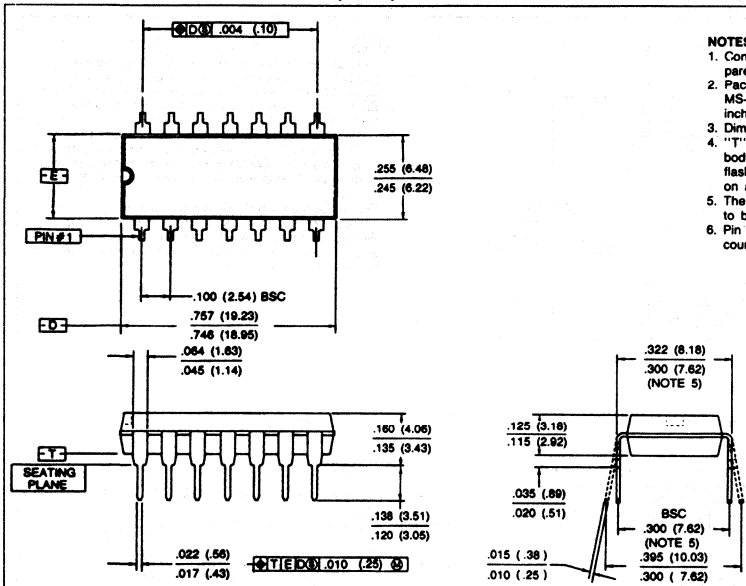




NOTES:
1. Package dimensions conform to JEDEC specification MS-013-AE for standard small outline (SO) package, 28 leads, 7.50mm (.300") body width (issue A, June 1985).
2. Controlling dimensions are in mm. Inch dimensions in parentheses.
3. Dimensions and tolerancing per ANSI Y14.5M- 1982.
4. "T", "D" and "E" are reference datums on the molded body and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .15mm (.006") on any side.
5. Pin numbers start with pin #1 and continue counterclockwise to pin #28 when viewed from top.
6. Signetics ordering code for a product packaged in a plastic small outline (SO) package is the suffix D after the product number.

Packaging Information

14–PIN PLASTIC DUAL IN–LINE (PDIP)

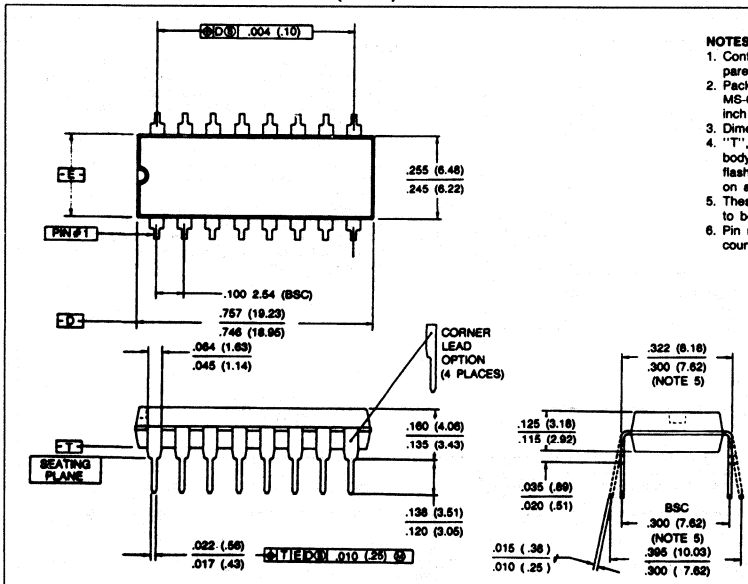


NH1 853-0405 81231

PC000330S

NOTES:
1. Controlling dimension: inches. Metric are shown in parentheses.
2. Package dimensions conform to JEDEC specification MS-001-AC for standard dual in-line (DIP) package .300 inch row spacing (PLASTIC) 14 leads (issue B. 7/85)
3. Dimensions and tolerancing per ANSI Y14. 5M-1982.
4. "T", "D" and "E" are reference datums on the molded body and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010 inch (.25mm) on any side.
5. These dimensions measured with the leads constrained to be perpendicular to plane T.
6. Pin numbers start with pin #1 and continue counterclockwise to pin #14 when viewed from the top.

16–PIN PLASTIC DUAL IN–LINE (PDIP)



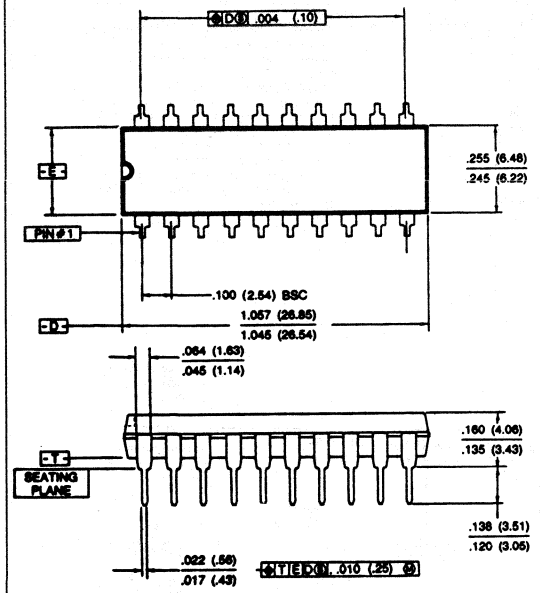
NJ1 853-0406 81232

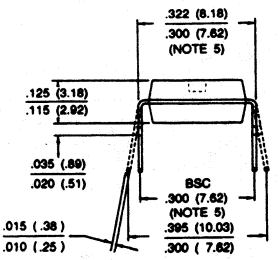
PC002806

NOTES:
1. Controlling dimension: inches. Metric are shown in parentheses.
2. Package dimensions conform to JEDEC specification MS-001-AA for standard dual in-line (DIP) package .300 inch row spacing (PLASTIC) 16 leads (issue B. 7/85)
3. Dimensions and tolerancing per ANSI Y14. 5M-1982.
4. "T", "D" and "E" are reference datums on the molded body and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010 inch (.25mm) on any side.
5. These dimensions measured with the leads constrained to be perpendicular to plane T.
6. Pin numbers start with pin #1 and continue counterclockwise to pin #16 when viewed from the top.

Packaging Information

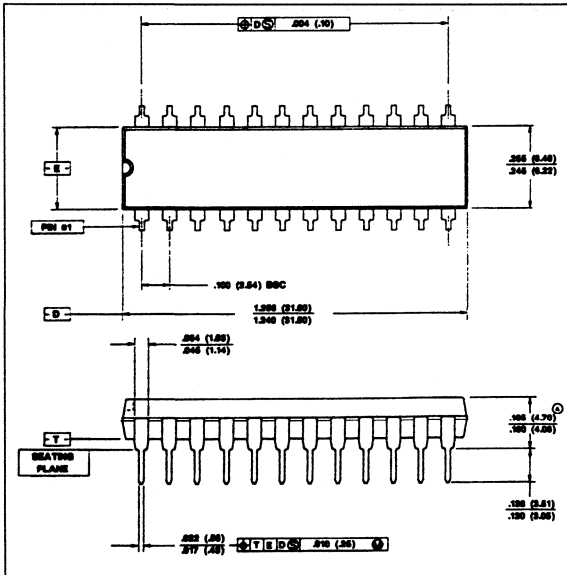
20–PIN PLASTIC DUAL IN–LINE (PDIP)

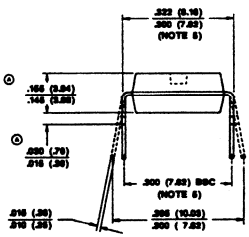




NOTES:
1. Controlling dimension: inches. Metric are shown in parentheses.
2. Package dimensions conform to JEDEC specification MS-001-AE for standard dual in-line (DIP) package .300 inch row spacing (PLASTIC) 20 leads (issue B, 7/85)
3. Dimensions and tolerancing per ANSI Y14. 5M-1982.
4. "T", "D" and "E" are reference datums on the molded body and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010 inch (.25mm) on any side.
5. These dimensions measured with the leads constrained to be perpendicular to plane T.
6. Pin numbers start with pin #1 and continue counterclockwise to pin #20 when viewed from the top.

24–PIN PLASTIC DUAL IN–LINE (PDIP)

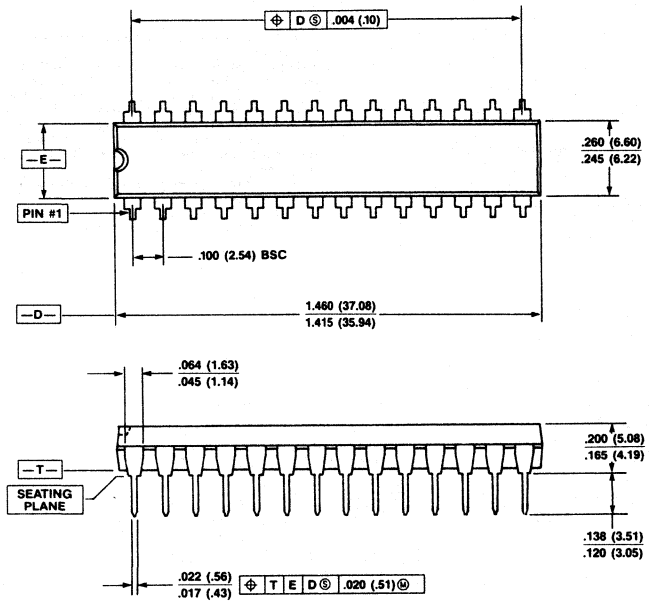




NOTES:
1. Controlling dimension: inches. Metric are shown in parentheses.
2. Package dimensions conform to JEDEC specification MS-001-AF for standard dual in-line (DIP) package .300 inch row spacing (PLASTIC) 24 leads (issue B, 7/85)
3. Dimension and tolerancing per ANSI Y14. 5M-1982.
4. "T", "D" and "E" are reference datums on the molded body and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010 inch (.25mm) on any side.
5. These dimensions measured with the leads constrained to be perpendicular to plane T.
6. Pin numbers start with pin #1 and continue counterclockwise to pin #24 when viewed from the top.

Packaging Information

28–PIN PLASTIC DUAL IN–LINE (PDIP) (300–mil–wide)



NOTES:

1. Controlling dimensions: inches. Metric are shown in parentheses.
2. Dimensions are tolerancing per ANSI Y14.5M-1982.
3. "T", "D", and "E" are reference datums on the molded body and do not include mold-flash or protrusions which shall not exceed .010 inch (.25 mm) on any side.
4. These dimensions measured with the leads constrained to be perpendicular to plane "T".
5. Pin numbers start with #1 and continue counterclockwise to pin #28 when viewed from the top.

853-0864 89398

NQ1

DATA HANDBOOK SYSTEM

DATA HANDBOOK SYSTEM

Our Data Handbook System comprises more than 60 books with specifications on electronic components, subassemblies and materials. It is made up of six series of handbooks:

INTEGRATED CIRCUITS

DISCRETE SEMICONDUCTORS

DISPLAY COMPONENTS

PASSIVE COMPONENTS*

PROFESSIONAL COMPONENTS**

MATERIALS*

The contents of each series are listed on pages III to VIII.

The data handbooks contain all pertinent data available at the time of publication, and each is revised and reissued periodically.

When ratings or specifications differ from those published in the preceding edition they are indicated with arrows in the page margin. Where application is given it is advisory and does not form part of the product specification.

Condensed data on the preferred products of Philips Components is given in our Preferred Type Range catalogue (issued annually).

Information on current Data Handbooks and how to obtain a subscription for future issues is available from any of the Organizations listed on the back cover.
Product specialists are at your service and enquiries will be answered promptly.

* Will replace the Components and materials (green) series of handbooks.
** Will replace the Electron tubes (blue) series of handbooks.

INTEGRATED CIRCUITS

This series of handbooks comprises:

code	handbook title
IC01	**Radio, audio and associated systems** Bipolar, MOS
IC02a/b	**Video and associated systems** Bipolar, MOS
IC03	**ICs for Telecom** Bipolar, MOS Subscriber sets, Cordless Telephones
IC04	**HE4000B logic family** CMOS
IC05	**Advanced Low-power Schottky (ALS) Logic Series**
IC06	**High-speed CMOS; PC74HC/HCT/HCU** Logic family
IC07	**Advanced CMOS logic (ACL)**
IC08	**ECL 10K and 100K logic families**
IC09N	**TTL logic series**
IC10	**Memories** MOS, TTL, ECL
IC11	**Linear Products**
IC12	**I^2C-bus compatible ICs**
IC13	**Semi-custom** Programmable Logic Devices (PLD)
IC14	**Microcontrollers** NMOS, CMOS
IC15	**FAST TTL logic series**
IC16	**CMOS integrated circuits for clocks and watches**
IC17	**ICs for Telecom** Bipolar, MOS Radio pagers Mobile telephones ISDN
IC18	**Microprocessors and peripherals**
IC19	**Data communication products**

DISCRETE SEMICONDUCTORS

This series of data handbooks comprises:

current code	new code	handbook title
S1	**SC01**	**Diodes** High-voltage tripler units
S2a	**SC02**	**Power diodes**
S2b	**SC03***	**Thyristors and triacs**
S3	**SC04**	**Small-signal transistors**
S4a	**SC05**	**Low-frequency power transistors and hybrid IC power modules**
S4b	**SC06**	**High-voltage and switching power transistors**
S5	**SC07**	**Small-signal field-effect transistors**
S6	**SC08** **SC09**	**RF power transistors** **RF power modules**
S7	**SC10**	**Surface mounted semiconductors**
S8a	**SC11***	**Light emitting diodes**
S8b	**SC12**	**Optocouplers**
S9	**SC13***	**PowerMOS transistors**
S10	**SC14**	**Wideband transistors and wideband hybrid IC modules**
S11	**SC15**	**Microwave transistors**
S15**	**SC16**	**Laser diodes**
S13	**SC17**	**Semiconductor sensors**
S14	**SC18***	**Liquid crystal displays and driver ICs for LCDs**

* Not yet issued with the new code in this series of handbooks.
** New handbook in this series; will be issued shortly.

DISPLAY COMPONENTS

This series of data handbooks comprises:

current code	new code	handbook title
T8	**DC01**	**Colour display components**
T16	**DC02**	**Monochrome monitor tubes and deflection units**
C2	**DC03**	**Television tuners, coaxial aerial input assemblies**
C3	**DC04***	**Loudspeakers**
C20	**DC05**	**Flyback transformers, mains transformers and general-purpose FXC assemblies**

* These handbooks are currently issued in another series; they are not yet issued in the Display Components series of handbooks.

PASSIVE COMPONENTS

This series of data handbooks comprises:

current code	new code	handbook title
C14	**PA01**	**Electrolytic capacitors; solid and non-solid**
C11	**PA02**	**Varistors, thermistors and sensors**
C12	**PA03**	**Potentiometers and switches**
C7	**PA04**	**Variable capacitors**
C22	**PA05***	**Film capacitors**
C15	**PA06***	**Ceramic capacitors**
C9	**PA07***	**Piezoelectric quartz devices**
C13	**PA08**	**Fixed resistors**

* Not yet issued with the new code in this series of handbooks.

PROFESSIONAL COMPONENTS

This series of data handbooks comprises:

current code	new code	handbook title
T1	*	**Power tubes for RF heating and communications**
T2a	*	**Transmitting tubes for communications, glass types**
T2b	*	**Transmitting tubes for communications, ceramic types**
T3	**PC01****	**High-power klystrons**
T4	*	**Magnetrons for microwave heating**
T5	**PC02****	**Cathode-ray tubes**
T6	**PC03****	**Geiger-Müller tubes**
T9	**PC04****	**Photo and electron multipliers**
T10	**PC05**	**Plumbicon camera tubes and accessories**
T11	**PC06**	**Circulators and Isolators**
T12	**PC07**	**Vidicon and Newvicon camera tubes and deflection units**
T13	**PC08**	**Image intensifiers**
T15	**PC09****	**Dry reed switches**
C8	**PC10**	**Variable mains transformers; annular fixed transformers**
	PC11	**Solid state image sensors and peripheral integrated circuits**

* These handbooks will not be reissued.
** Not yet issued with the new code in this series of handbooks.

MATERIALS

This series of data handbooks comprises:

current code	new code	handbook title
C4 } C5 }	MA01*	**Soft Ferrites**
C16	MA02**	**Permanent magnet materials**
C19	MA03**	**Piezoelectric ceramics**

* Handbooks C4 and C5 will be reissued as one handbook having the new code MA01.

** Not yet issued with the new code in this series of handbooks.

Philips Components – a worldwide company

Argentina: PHILIPS ARGENTINA S.A., Div. Philips Components, Vedia 3892, 1430 BUENOS AIRES, Tel. (01) 541-4261.
Australia: PHILIPS COMPONENTS PTY Ltd, 11 Waltham Street, ARTARMON, N.S.W. 2064, Tel. (02) 439 3322.
Austria: ÖSTERREICHISCHE PHILIPS INDUSTRIE G.m.b.H., UB Bauelemente, Triester Str. 64, 1101 WIEN, Tel. (0222) 60 101-820.
Belgium: N.V PHILIPS PROF. SYSTEMS – Components Div., 80 Rue Des Deux Gares, B-1070 BRUXELLES, Tel. (02) 52 56 111.
Brazil: PHILIPS COMPONENTS (Active Devices) Av. Brigadeiro Faria Lima, 1735-SAO PAULO-SP, Tel. (011) 211-2600.
PHILIPS COMPONENTS (Passive Devices & Materials) Av. Francisco Monteiro, 702-RIBEIRO PIRES-SP, Tel. (011) 459-8211.
Canada: PHILIPS ELECTRONICS LTD., Philips Components, 601 Milner Ave., SCARBOROUGH, Ontario, M1B 1M8, Tel. (416) 292-5161.
Chile: PHILIPS CHILENA S.A., Av. Santa Maria 0760, SANTIAGO, Tel. (02) 77 38 16.
Colombia: IPRELENSO LTDA., Carrera 21 No. 56-17, BOGOTA, D.E., P.O. Box 77621, Tel. (01) 249 76 24.
Denmark: PHILIPS COMPONENTS A/S, Prags Boulevard 80, PB1919, DK-2300 COPENHAGEN S, Tel. 01-54 11 33.
Finland: PHILIPS COMPONENTS, Sinikalliontie 3, SF-2630 ESPOO HELSINKI 10, Tel. 358-0-50 261.
France: PHILIPS COMPOSANTS RTC-COMPELEC, 117 Quai du Président Roosevelt, 92134 ISSY-LES-MOULINEAUX Cedex, Tel. (01) 40 93 80 00.
Germany (Fed. Republic): VALVO, UB Bauelemente der Philips G.m.b.H., Valvo Haus, Burchardstrasse 19, D-2 HAMBURG 1, Tel. (040) 3296-0.
Greece: PHILIPS HELLENIQUE S.A., Components Division, No. 15, 25th March Street, GR 17778 TAVROS, Tel. (01) 489 4 339/489 4 911.
Hong Kong: PHILIPS HONG KONG LTD., Components Div., 15/F Philips Ind. Bldg., 24-28 Kung Yip St., KWAI CHUNG, Tel. (0-42 45 121.
India: PEICO ELECTRONICS & ELECTRICALS LTD., Components Dept., Band Box Building, 254-D Dr. Annie Besant Rd., BOMBAY – 400 025, Tel. (022) 493 0311/493 0590.
Indonesia: P.T. PHILIPS-RALIN ELECTRONICS, Components Div., Setiabudi II Building, 6th Fl., Jalan H.R. Rasuna Said (P.O. Box 223/KBY) Kuningan, JAKARTA 12910, Tel. (021) 51 79 95.
Ireland: PHILIPS ELECTRONICS (IRELAND) LTD., Components Division, Newstead, Clonskeagh, DUBLIN 14, Tel. (01) 693355.
Italy: PHILIPS S.p.A., Philips Components, Piazza IV Novembre 3, I-20124 MILANO, Tel. (02) 6752.1.
Japan: PHILIPS K.K. Philips Components Division, Philips Bldg 13-37, Kohnan 2-chome, Minato-ku, TOKYO (108), Tel. (03) 740 5028.
Korea (Republic of): PHILIPS ELECTRONICS (KOREA) LTD. Components Division, Philips House, 260-199 Itaewon-dong, Yongsan-ku, SEOUL, Tel. (02) 794-5011.
Malaysia: PHILIPS MALAYSIA SDN BHD, Components Div., 3 Jalan SS15/2A SUBANG, 47500 PETALING JAYA, Tel. (03) 73 45 511.
Mexico: PHILIPS COMPONENTS, Paseo Triunfo de la Republica, No 215 Local 5, Cd Juarez CHI HUA HUA 32340 MEXICO Tel. (16) 18-67-01/02.
Netherlands: PHILIPS NEDERLAND, Marktgroep Philips Components, Postbus 90050, 5600 PB EINDHOVEN, Tel. (040) 78 37 49.
New Zealand: PHILIPS NEW ZEALAND LTD., Components Division, 110 Mt. Eden Road, C.P.O. Box 1041, AUCKLAND, Tel. (09) 605-914.
Norway: NORSK A/S PHILIPS, Philips Components, Box 1, Manglerud 0612, OSLO, Tel. (02) 68 02 00.
Pakistan: PHILIPS ELECTRICAL CO. OF PAKISTAN LTD., Philips Markaz, M.A. Jinnah Rd., KARACHI-3, Tel. (021) 72 57 72.
Peru: CADESA, Av. Pardo y Aliaga No. 695, 6th Floor, San Isidro, LIMA 100, PO. Box 5612, Tel. (014) 70 70 80.
Philippines: PHILIPS INDUSTRIAL DEV. INC., 2246 Pasong Tamo, P.O. Box 911, Makati Comm. Centre, MAKATI-RIZAL 3116, Tel. (02) 868 951 to 59.
Portugal: PHILIPS PORTUGUESA S.A.R.L., Av. Eng. Duarte Pacheco 6, 1009 LISBOA Codex, Tel. (019) 68 31 21.
Singapore: PHILIPS SINGAPORE, PTE LTD., Components Div., Lorong 1, Toa Payoh, SINGAPORE 1231, Tel. 350 2000.
South Africa: S.A. PHILIPS PTY LTD., Components Division, JOHANNESBURG 2000, P.O. Box 7430.
Spain: PHILIPS COMPONENTS, Balmes 22, 08007 BARCELONA, Tel. (03) 301 63 12.
Sweden: PHILIPS COMPONENTS, A.B., Tegeluddsvägen 1, S-11584 STOCKHOLM, Tel. (0)8-782 1 000.
Switzerland: PHILIPS A.G., Components Dept., Allmendstrasse 140-142, CH-8027 ZÜRICH, Tel. (01) 488 22 11.
Taiwan: PHILIPS TAIWAN LTD., 150 Tun Hua North Road, P.O. Box 22978, TAIPEI, Taiwan, Tel. (02) 71 20 500.
Thailand: PHILIPS ELECTRICAL CO. OF THAILAND LTD., 283 Silom Road, P.0. Box 961, BANGKOK, Tel. (02) 233-6330-9.
Turkey: TÜRK PHILIPS TICARET A.S., Philips Components, Talatpasa Cad. No. 5, 80640 LEVENT/ISTANBUL, Tel. (01) 179 27 70.
United Kingdom: PHILIPS COMPONENTS LTD., Mullard House, Torrington Place, LONDON WC1E 7HD, Tel. (01) 580 6633.
United States: (Colour picture tubes – Monochrome & Colour Display Tubes) PHILIPS DISPLAY COMPONENTS COMPANY, 1600 Huron Parkway, P.O. Box 963, ANN ARBOR, Michigan 48106, Tel. 313/996-9400.
(IC Products) SIGNETICS CORPORATION, 811 East Arques Avenue, SUNNYVALE, CA 94088-3409, Tel. (408) 991-2000.
(Passive Components, Discrete Semiconductors, Materials and Professional Components) PHILIPS COMPONENTS, Discrete Products Division, 2001 West Blue Heron Blvd., P.O. Box 10330, RIVIERA BEACH, Florida 33404, Tel. (407) 881-3200.
Uruguay: PHILIPS COMPONENTS, Coronel Mora 433, MONTEVIDEO, Tel. (02) 70-40 44.
Venezuela: MAGNETICA S.A., Calle 6, Ed. Las Tres Jotas, CARACAS 1074A, App. Post. 78117, Tel. (02) 241 75 09.
Zimbabwe: PHILIPS ELECTRICAL (PVT) LTD., 62 Mutare Road, HARARE, P.O. Box 994, Tel. 47211.

For all other countries apply to: Philips Components Division, Strategic Accounts and International Sales, P.O. Box 218, 5600 MD EINDHOVEN, The Netherlands, Telex 35000 phtcnl, Fax. 23753

AS75

Printed in The Netherlands 9398 170 400 11

Philips Components

PHILIPS

PHILIPS